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Design and Measurements of 64-channel ASIC for Neural Signal Recording

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Abstract—**This paper presents the design and measurements of a low noise multi-channel front-end electronics for recording extra-cellular neuronal signals using microelectrode arrays. The integrated circuit contains 64 readout channels and was fabricated in CMOS 0.18 μm technology. A single readout channel is built of an AC coupling circuit at the input, a low noise preamplifier, a band-pass filter and a second amplifier. In order to reduce the number of output lines, the 64 analog signals from readout channels are multiplexed to a single output by an analog multiplexer. The chip is optimized for low noise and matching performance with the possibility of cut-off frequencies tuning. The low cut-off frequency can be tuned in the 1 Hz - 60 Hz range and the high cut-off frequency can be tuned in the 3.5 kHz - 15 kHz range. For the nominal gain setting at 44 dB and power dissipation per single channel of 220 μW the equivalent input noise is in the range from 6 μV - 11 μV rms depending on the band-pass filter settings. The chip has good uniformity concerning the spread of its electrical parameters from channel to channel. The spread of gain calculated as standard deviation to mean value is about 4.4% and the spread of the low cut-off frequency is on the same level. The chip occupies 5×2.3 mm^2 of silicon area.**

I. Introduction

FRONTIERS of neurobiological and pharmacological experiments need multi-channel readout systems for simultaneous recording of extra-cellular signals from many neuronal cells. These experiments develop in two directions. The first one aims to find answers to principal questions: how complicated neuronal system like retina or brain code and process information. In this case recording the neuronal signals is performed both in vivo and in vitro experiments [1, 2, 3]. The other direction is connected with cultured neuronal networks, which emerged as a powerful tool in the assessment of acute neuropharmacological effects of both known and unknown agents [4].

For simultaneous recording of neuronal signals from many cells one needs both a high density multi-electrode array and a multi-channel readout electronic system. Multi-channel readout systems are offered commercially as up to 128-channel readout modules. Further increase of the number of channels becomes very unpractical because of the large volume occupied by the electronics (which is connected to high density microelectrode arrays) and because of high cost. An obvious solution to overcome these problems is to use the VLSI technology in order to develop an Application Specific Integrated Circuit (ASIC), which is suitable for these purposes.

In the references pertaining to the subject there are several examples of ASICs dedicated to extra-cellular recording like [5-9]. Based on our experience in design and practical applications of such kind of ASICs for recording system comprising of hundreds of electrodes [10, 11, 12], we propose a novel 64-channel ASIC, which meets requirements for a low power and small silicon area, a good matching of analog parameters from channel to channel, a low frequency range operation and a low noise performance.

The paper is organized as follows. Section II describes the ASIC architecture. The measurements of the multi-channel ASIC are presented in Section III. Section IV contains a summary.

II. Chip Architecture

The ASIC comprises three basic blocks: 64 AC coupling circuits at the inputs, 64 analog channels with amplifiers and filters and an analog 64:1 multiplexer (see Fig. 1). It was fabricated in CMOS 0.18 μm technology.

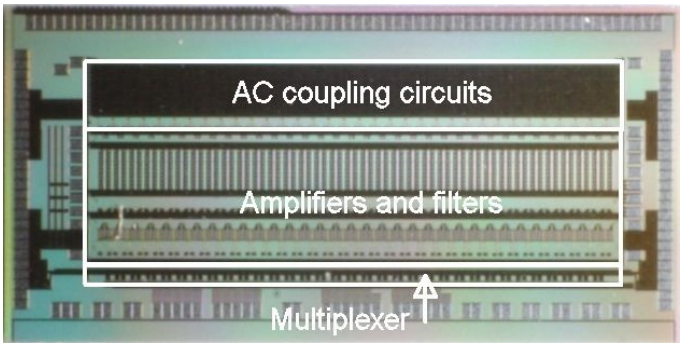

Fig. 1. Photo of 64-channel chip: input pads are at the top side, control and output pads are at the bottom side, power supply and test pads are on the left and right side.

The 64 analog channels amplify and filter small amplitude neuronal signals, which are typically in the range from tens to hundreds of μV with the frequency spectrum from a few Hz to a few kHz [7]. The signals are recorded with respect to common reference electrode INREF immersed in

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physiological saline solution. The low and the high cut-off frequencies of the channel are controlled by external signals. The signals from the 64 channels are sampled at the same moment and subsequently multiplexed through the analog multiplexer to the output buffer.

A. Architecture of the analog readout channel

Since the readout channel is a part of the multi-channel system and records small amplitude input signals, one has to take into account requirements concerning low noise performance, uniformity of analog parameters in all 64 channels and power limitation. The proposed architecture of single readout channel is shown in Fig. 2. It consists of three main sections: AC coupled input preamplifier, band-pass filter stage with AC coupled output and second amplifier.

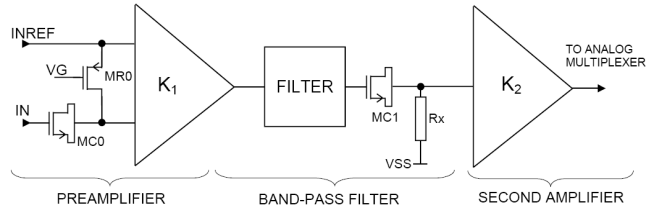


Fig. 2. Simplified block diagram of single readout channel.

B. AC coupling circuits

Using the AC coupling in the readout channel suppresses the DC offset propagation through the entire signal path (in our case the total gain is about 44 dB) and improves the uniformity of the analog parameters in the multi-channel system. Additionally the AC coupling circuits work as high-pass filters and suppress the low frequency 1/f noise generated in MOS transistors.

The AC coupling circuits are used twice in the readout channel:

- at the input of the preamplifier (transistors MC0-MR0) to cut off the offsets generated by the interface between electrodes and biological cells,
- at the output of filter stage (elements MC1-Rx) to cut off the offsets generated by the preamplifier and filter.

The high value input capacitors MC0 (with effective capacitance C_{g0} = 80 pF) is realised using MOS transistors of W_{C0}/L_{C0} = 400µm/50µm biased in the strong inversion region [6]. The MR0 is formed as the array of six PMOS transistors with W_{R0}/L_{R0} = 0.4µm/50µm each connected in series and working in linear region. Changing the gate voltage VG of transistor MR0 (see Fig. 2) one controls the low cut-off frequency at the preamplifier input.

The second AC coupling has also MOS capacitor MC1 (with a much lower area W_{C1}/L_{C1} = 60µm/29.5µm) and the effective resistance Rx based on two current sources as it is described in our previous papers [10]. The low cut-off frequency of this circuit is much below a single Hz.

C. Low noise preamplifier

The scheme of low noise preamplifier is shown in Fig. 3. The preamplifier design is optimised for low noise performance. The total noise of the preamplifier is a sum of three main components:

- noise of the differential amplifier M1-M5:
- noise of the AC coupling circuit MC0-MR0,
- noise of the source follower input transistors MSF, which ensures the bias of MC0 transistor in strong inversion region.

The current consumption in this stage is 95 µA and its gain is 38 dB. The feedback capacitance of C0 limits the preamplifier bandwidth to 440 kHz.

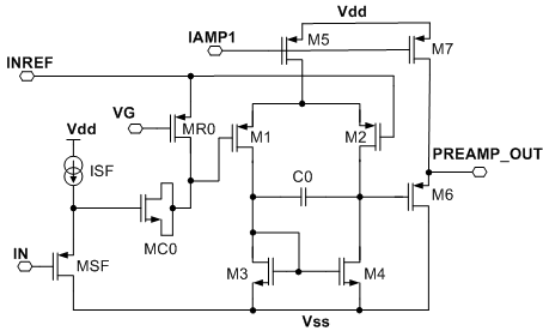


Fig. 3. Simplified scheme of the preamplifier.

D. Pass-band filter with frequency tuning

The scheme of the filter core is shown in Fig. 4. The band-pass filter is obtained as a combination of two RC low-pass filters with the cut-off frequencies corresponding to the required low and high cut-off frequency, and of a differential amplifier MF1-MF5 [10].

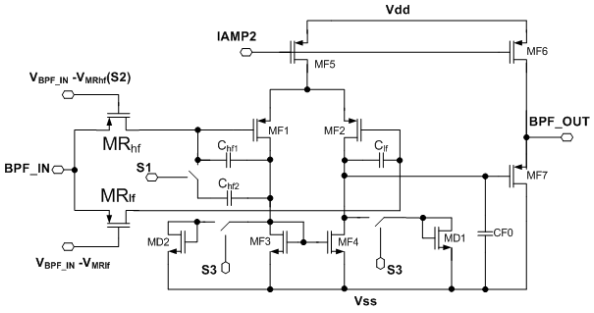


Fig. 4. Simplified scheme of the filter.

The resistors of the RC filters are built of transistor MR_{hf} of W_{Rhf}/L_{Rhf} = 10µm/30µm and transistor MR_{lf} of W_{Rlf}/L_{Rlf} = 1µm/150µm which are biased in the linear region. The input signal is applied simultaneously to the sources of these transistors and with a DC offset to their gates. The effective capacitances are formed by the metal-metal capacitor C_{hf1} = 0.52 pF and C_{hf2} = 3.15 pF for the high cut-off frequency and by the metal-metal capacitor C_{lf} = 7.98 pF for the low cut-off frequency (multiplied due to the Miller effect by the gain of differential stage MF1-MF5).

There are three different switches to control the cut-off frequencies in the filters stage:

- S1 to modify the effective value of C_{hf} capacitance,
- S2 to change the small signal resistance of MR_{lf},
- S3 to change the effective gain of differential amplifier MF1-MF5 and in this way the multiplication factor for the Miller effect.

The band pass filter consumes 20 µW of power and its gain is 0.7 dB.

E. Analog multiplexer and crosstalk minimization

In order to reduce the number of output lines, the 64 analog signals from the 64 front-end channels on the chip are multiplexed to a single output by an analog multiplexer. The block diagram of the multiplexer is presented in Fig. 5. Multiplexer is built of 64 channels consisting of sample and hold circuit with input buffers. Signal from each channel (IN0-IN63) is subtracted from the signal from the dummy channel (IN_ DUMMY) with use of the differential amplifier stage (DIFF). This operation minimizes the effect of substrate noise introduced by the digital part of the chip.

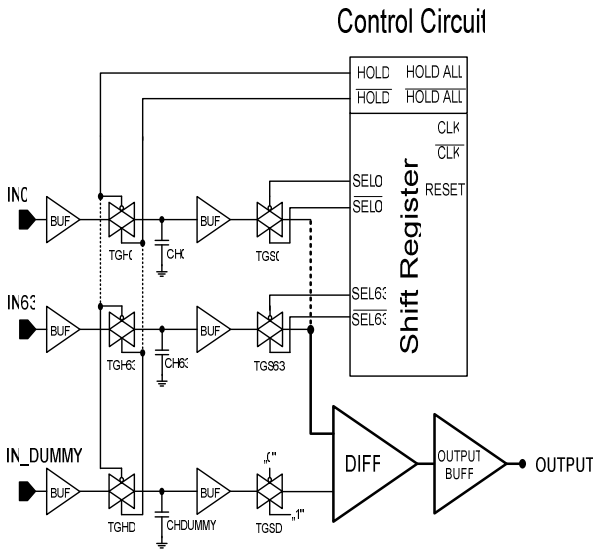


Fig. 5. Simplified scheme of the multiplexer.

The bandwidth of single channel is limited to 15 kHz. The nominal frequency of multiplexer operation is 5 MHz. This results in about 75 kHz sampling frequency per single channel and it is enough to avoid aliasing problem.

For test purposes the readout of the multiplexer can be performed in two ways, either all channels are read sequentially or only one channel is read.

III. TEST RESULTS

A. Pass-band settings

The pass-band of the single channel can be changed by tuning of time constant in the AC coupling input stage and by the switches in the filter stage (S1, S2, S3). Using the analog control at the input (VG voltage - see Fig. 3) the low cut-off frequency can be tuned continuously from 1 Hz to 60 Hz as it is shown in Fig. 6(a). The high cut-off frequency can be changed only by switches in the filter stage, setting its value in steps around 3.5 kHz, 9 kHz or 15 kHz (see Fig. 6 (b)). The frequency tuning allows to find the best settings for given neurobiological tests, however the pass-band of the analog channel influences the noise performance and signal to noise ratio in our system.

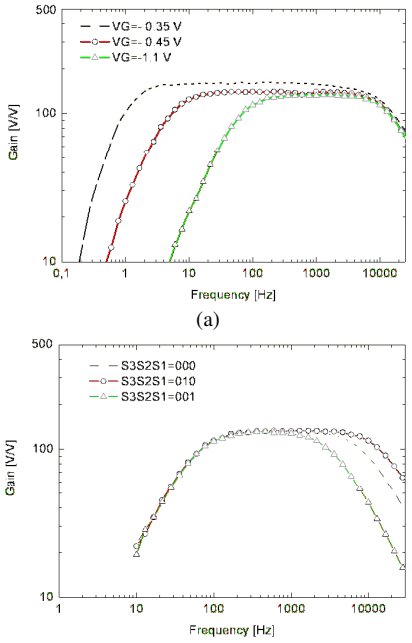


Fig.6. Frequency response of single channel for: a) tuning the time constant of the input AC coupling circuit, b) different values of switches S1, S2, S3 to change the high cut-off frequency.

B. Channel-to-channel uniformity

The ASIC consists of 64 identical channels with the bias and control currents common for all the channels. Therefore the spreads of the basic parameters from channel to channel, like gain, output offsets, cut-off frequencies, are important having in mind single ASIC applications and also future large multi-chip systems. Typical distributions of these parameters measured for the ASIC are shown in Fig. 7 and Fig. 8. The spread of the gain defined as as standard deviation to mean value (sd/mean) is equal to 4.4%. The low offset spread at the multiplexer outputs (standard derivation is equal to 3.5 mV) makes the future operation with external ADC much easier.

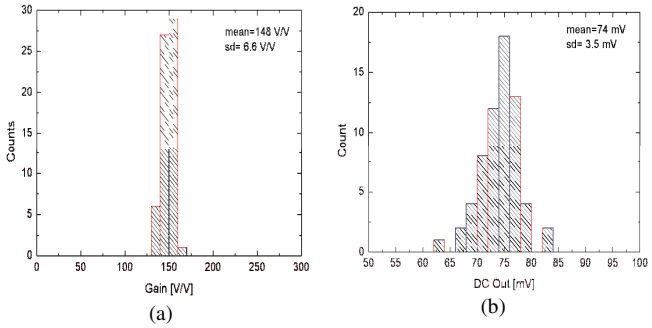
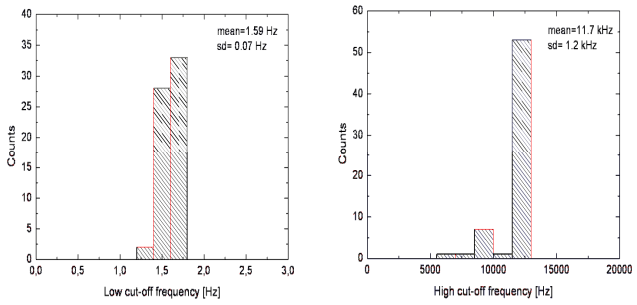


Fig.7. Spread of analog parameters in 64-channel ASIC: (a) gain, (b) offset.

Probably the most difficult parameter in many of the multi-channel ASIC designs for neurobiology experiments is the small spread of the low cut of frequency from channel to channel. For our design this spread is on the level of 4.4% - see Fig. 8(a). The spread of the high cut-off frequency is about 10.2% - see Fig. 8(b).



(a) (b)

Fig. 8. Spread of analog parameters in 64-channel ASIC: (a) low cut-off frequency, (b) high cut-off frequency .

C. *Preliminary noise measurements*

We measured the noise of the ASIC for different values of cut-off frequencies in the filter stage and different time constants of the input AC coupling circuit. The examples of measured Power Spectral Density (PSD) of noise for two different pass-band settings are shown in Fig. 9:

- setting I: pass-band 20 Hz - 6.5 kHz, gain 42 dB,
- setting II: pass-band 1 Hz - 13 kHz, gain 44 dB.

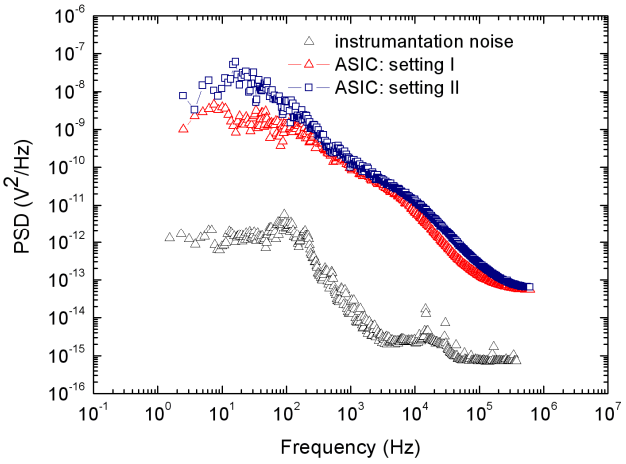


Fig.9. Power spectral density of output noise of ASIC for two different settings of band-pass and instrumentation noise.

Taking the square root of integrals from plots in Fig. 9 and dividing these results by the gain of the circuit, one can obtain rms value of equivalent input noise which are equal to 6 µV rms and 11 µV rms respectively. The noise are enough low for most of neurobiology experiments, however the noise are three times higher than we expected from earlier circuit simulations. Thanks to different test structures implemented in our ASIC, the effect of higher noise is the subject our intensive investigations.

IV. SUMMARY

We have shown a novel circuit solutions of a low noise multi-channel integrated circuit working in the low frequency range and realized in CMOS 0.18 µm technology. The essential parameters of the presented ASIC are summarized in table 1. The low noise performance of the IC, implemented AC coupling at the inputs and good channel-to-channel matching make the ASIC a universal multi-channel readout ASIC for experiments with alive neuronal cells. This ASIC can be used in systems comprising of several hundreds/thousands of readout channels for both in vivo and in vitro experiments.

TABLE I
SUMMARY OF BASIC PARAMETERS OF ASIC

Parameter	Value
Gain	44 dB
Tuning range for low cut-off frequency	1 - 60 Hz
Tuning range for high cut-off frequency	3.5 - 15 kHz
Equivalent input noise	6 - 11 µV
Power per channel	220 µW
Linearity for input signals	2 mV
Spread of gain and low cut-off frequency	4.4 %
Power supply voltage	±1.1

REFERENCES

[1] A.M. Litke, E.J. Chichilnisky, W. Dąbrowski, A. Grillo, P. Gryboś, S. Kachiguine, M. Rahman, G. Taylor, "Large scale imaging of retinal output activity." *Nucl. Instr. and Meth.,* vol. 501, 2002, pp. 298-307.

[2] H. Oka, K. Shimono, R. Ogawa, H. Sugihara, M. Takateni, "A new planar multielectrode array for extracellular recording application to hippocampal acute slice." *J. Neurosci. Meth.,* vol. 93, 1999, pp. 61–67.

[3] Y. Jimbo, H.P.C. Robinson, "Propagation of spontaneous synchronized activity in cortical slice cultures recorded by planar electrode arrays." *Bioelectrochemistry*, vol. 51, 2000, pp. 107–115.

[4] J.J. Pancrazio, R.P. Bey, Jr., A. Loloee , S. Manne, H-C. Chao, L.L. Howard, W. Milton Gosney , D.A. Borkholder, G.T.A. Kovacs, P. Manos, D.S. Cuttino, D.A. Stenger, "Description and demonstration of a CMOS amplifier-based-system with measurement and stimulation capability for bioelectrical signal transduction." *Biosensors & Bioelectronics*, vol. 13, 1998, pp. 971–979.

[5] R. R. Harrison, "A versatile integrated circuit for the acquisition of biopotentials." Custom Integrated Circuits Conference, 2007, CICC '07, pp. 115-122.

[6] R. R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, B. Greger, F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system." Solid-State Circuits, IEEE Journal of Solid-State Circuits, vol. 42, 2007, pp. 123–133.

[7] R. F. Yazicioglu, P. Merken, R. Puers, C. Van Hoof "A 60µW 60nV/√Hz readout front-end for portable biopotential acquisition systems." IEEE Journal of Solid-State Circuits, vol. 42, 2007, pp. 1100-1110.

[8] P. Mohseni, K. Najafi, "A low power fully integrated bandpass operational amplifier for biomedical neural recording applications", Engineering in Medicine and Biology, EMBS/BMES Conference, vol. 3, 2002, pp. 2111-2112.

[9] M. Roham, P. Mosheni, "A reconfigurable IC for wireless monitoring of chemical or electrical neural activity." Circuits and Systems, ISCAS 2008, pp. 1978-1981.

[10] P. Gryboś, *Low Noise Multichannel Integrated Circuits in CMOS Technology for Physics and Biology Applications.* Monography 117, AGH Uczelniane Wydawnictwa Naukowo-Dydaktyczne, Kraków 2002, available at: www.kmet.agh.edu.pl/www/asics

[11] P. Grybos, W. Dabrowski, P. Hottowy, T. Fiutowski, "Low noise multichannel front-end electronics for recording signals from alive neuronal cells." Mixed Design of Integrated Circuits and Systems, MIXDES 2004, pp. 214-219

[12] A. Litke, N. Bezayiff, E. Chichilinsky, W. Cunnigham, W. Dabrowski, A. Grillo, M. Grivich, P. Grybos, P. Hottowy, S. Kachiguine, R. Kalmar, K. Mathieson, D. Petrusca, M. Rahman, A. Sher, "What does the eye tell the brain?: Development of system for the large-scale recording of retinal output activity." IEEE Transactions on Nuclear Scienc, vol. 51, 2004, pp. 1434-1440.