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Efficient Algorithm development of CIS Speech Processing Strategy for Cochlear Implants

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Abstract— **Continuous Interleaved Sampling (CIS) is one of the most useful and famous speech processing strategies used in Cochlear Implant speech processors. However, algorithm realization in hardware is a laborious task due to high computation cost of the algorithm. Real-time issues and low-power design demands an optimized realization of algorithm. This paper proposes two techniques to cut the computation cost of CIS by using polyphase filters and by implementing the complete algorithm in frequency domain. About 70% reduction in computation cost can be achieved by using multi-rate, multi-stage filters; whereas computation cost decreases by a factor of five when the whole algorithm is implemented in frequency domain. Evaluation of the algorithm is done by a laboratory designed algorithm development and evaluation platform. Algorithm flow diagrams and their computation details have been given for comparison. Utilizing the given techniques can remarkably reduce the processor load without any compromise on quality.**

I. Introduction

Cochlear Implant (CI) is an electronic prosthetic device surgically implanted into the inner ear that restores partial hearing to the profoundly deaf [1]. Unlike commercial hearing aids which benefit patients with conductive hearing loss, cochlear implant, on the other hand, also benefits patients with sensory-neural hearing impairment. It bypasses the normal hearing mechanism and directly stimulates the inner ear sensory cells of the auditory nerve by delivering electrical signals to an electrode array implanted inside the cochlea. These electrical signals are derived from the external sound acquired from a microphone. Sound signals are first manipulated by an external speech processor and then transmitted via transcutaneous link in the form of electromagnetic waves to the inner ear where they are finally converted into electrical pulses. With high success rates and increasing demand of implants worldwide, a substantial growth and progress is seen in the cochlear implant research in the last two decades.

A speech processing strategy or speech coding strategy is one of the key features which affect the overall performance of the device [1]. Speech Processing may be regarded as a functional space composed of a series of nonlinear functions which maps acoustic signals to the electrical domain such that the final electrical impulses mimic the actual impulses delivered by a healthy cochlea. Depending upon the speech processing strategy, the speech processor extracts various parameters from the acoustic signals and converts them into electrical signals. Various speech processing strategies have been developed and reported in literature [2-4] over time for cochlear prosthesis which include Continuous Interleaved Sampling (CIS), Spectral Peak (SPEAK), Advanced Combination Encoder (ACE), Spectral Maxima Sound Processor (SMSP), Simultaneous Analog Strategy (SAS), Paired Pulsatile Sampler (PPS), Quadruple Pulsatile Sampler (QPS) and various Formant based Strategies. Numerous algorithms based on Wavelet Transform [5], Wavelet Packets [6], Bionic Wavelet Transform [7] and Auditory Models [8] are also found in literature. In contrast to traditional approaches, various algorithms especially for tonal languages have been developed, which emphasize on the extraction of maximum tonal and pitch information from speech [9].

Although performance of different speech processing strategies is variable from patients to patient but CIS generally achieves better performance on considerably large percentage of implanted patients [10]. This is the reason it is included in all currently available implant systems (Nucleus 24, Med-El and Clarion). CIS is also very easy to implement and adjust, and most importantly, it is computationally efficient due to the parallel nature of algorithm in which different processes may be pipelined and multithreaded as compare to the other strategies which are computationally more demanding.

This paper addresses the need for efficient hardware implementation of CIS in terms of computation and performance. Computation cost is a challenging bottleneck for low-power, real-time processing applications such as a cochlear implant speech processor and therefore requires critical optimization. A low-cost, customized laboratory made simplified speech processing module is used for the implementation and evaluation of the algorithms [11]. Paper is organized as follows: First of all an overview of the evaluation module is given. Then in Section III, CIS algorithm is discussed in detail along with the improvements made in the implementation of these algorithms. A comprehensive comparison in terms of performance and computation cost is given in the end followed by the conclusion.

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II. Evaluation Module

As the name suggests, Speech Processing Evaluation Module is a laboratory made algorithm development, analysis and evaluation platform to design algorithms and test their performance. It is based on a commercially available floating point DSP Starter kit (DSK TMS320C6713). DSK was used for the research module because it provides an efficient and stable DSP development environment and can better mimic the actual low power processor found in any cochlear implant device. It is also a robust, low-cost and easily available DSK in both universities and industry.

Evaluation is carried out by three sub-modules: i) Software Evaluation Module, ii) Hardware Evaluation Module and iii) Real-time Patient Evaluation Module as shown in Figure 1.

A. Software Evaluation Module

Software Evaluation Module is a graphical environment developed in MATLAB for the algorithm development, assessment and to study the effect of different parameters on overall performance of the algorithm. Figure 2 shows a snapshot of the graphical user interface (GUI) for an eight channel CIS algorithm. It has a waveform analyzer which enables visual representation of waveforms at different channels. Moreover, it has capability to reconstruct multichannel signals in the form of synthesized sound for the evaluation of speech quality.

B. Hardware Evaluation Module

Hardware Evaluation Module is a software utility to test the CIS performance when it is realized in the hardware domain. Hardware Evaluation Module evaluates the real time operational performance of the CIS in DSP environment as well as the final speech recognition ability in real-time. Hardware Evaluation Module was developed using SIMULINK and TMS320C6713 DSK and it is capable of revealing the actual hardware issues pertinent to the algorithm design such as computation cost of an algorithm, data rates and real-time issues which are bottleneck performance parameters of any implantable medical device.

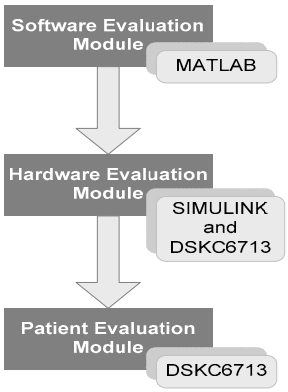

Fig. 1. Evaluation Module

Fig. 1. GUI: Software Evaluation Module

C. Real-time Patient Evaluation Module

Finally, Real-Time Patient Evaluation Module is used for laboratory testing of the developed and optimized CIS algorithm with actual Cochlear Implant patients. It is essentially a digital signal processing board directly linked with Software Evaluation and Hardware Evaluation Modules. Software routines of CIS are coded in C. It enables final evaluation of patient's response to any particular speech processing strategy as well his/her response to parametric variations of the strategy.

III. Continuous Interleaved Sampling

Continuous Interleaved Sampling or CIS is one of the most famous and commonly used speech processing strategies. It is a type of Pulsatile Waveform strategy. Figure 3 depicts the algorithm flow of CIS. The input signal is first pre emphasized and then passed through a filter bank. For an n-channel CIS algorithm, the filter bank consists of n bandpass filters with nonlinear band widths. Usual choice for n is eight. After passing through filter bank, envelopes of the filtered signals are computed via full wave rectification followed by a lowpass filter with a typical cutoff of 200Hz. In conversational speech, the acoustic amplitudes may vary over a range of 30 dB. Implant listeners, however, may have a dynamic range as small as 5 dB. Therefore, envelope compression is done by mapping acoustic amplitudes to electrical amplitudes using nonlinear mapping functions. These mapping functions map the acoustic amplitudes to the electrical dynamic range of the patient. Two most popular

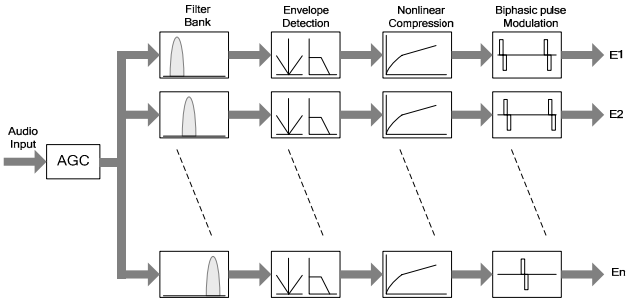

Fig. 3. Algorithm flow: Continuous Interleaved Sampling

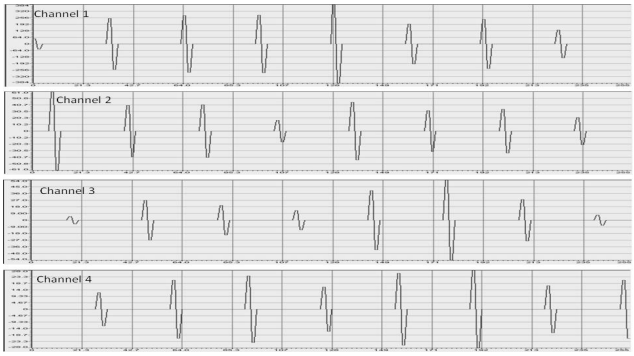

Fig.4. Interleaved Biphasic pulses for four consecutive channels

compression functions are i) Logarithmic Compression Function; ii) Power Law Compression Function. Mathematically, Logarithmic Compression function may be stated as:

$$Y = Alog(x) + B$$

while Power law compression function may be stated as:

$$Y = Ax^p + B$$

where x is the acoustic amplitude (output of the envelope detector), A and B are constants and Y is the (compressed) electrical amplitude. For Power Law $p < 1$. Values for A and B depend on two electrical dynamic range parameters commonly known as Threshold Level (THL) and Most Comfortable Level (MCL) and they can be mathematically expressed as:

$$A = \frac{MCL - THL}{x_{max} - x_{min}}$$

$$B = THL - Ax_{min}$$

Variables MCL and THL may vary from patient to patient and channel to channel as well. Final stage of the algorithm is to modulate it with biphasic pulses in such a way that all channels are time multiplexed with each other i.e. only one channel is active at a time. Biphasic pulses are used to modulate the envelope in order to preserve the charge balance inside the cochlea whereas time multiplexing is done in order to avoid inter-channel interaction. Channel interaction is a major problem and CIS solves this problem by providing signals in the form of biphasic pulses interleaved in time. However, time multiplexing calls for the need for higher data rates for effective speech comprehension. Figure 4 illustrates pulsatile biphasic pulses interleaved in time suitable for cochlear stimulation.

IV. Cost Reduction

Need for higher data rates and low power design demands optimization in the way CIS is implemented in DSP. Following techniques can considerably reduce the computation cost without any compromise on performance.

A. Multi-rate, Multi-stage Filters

The filter Bank is the most complex component of CIS and it takes about 60% execution time of the CIS algorithm. Since frequency mapping inside the cochlea is nonlinear and most information of acoustic signals lie in the low frequency

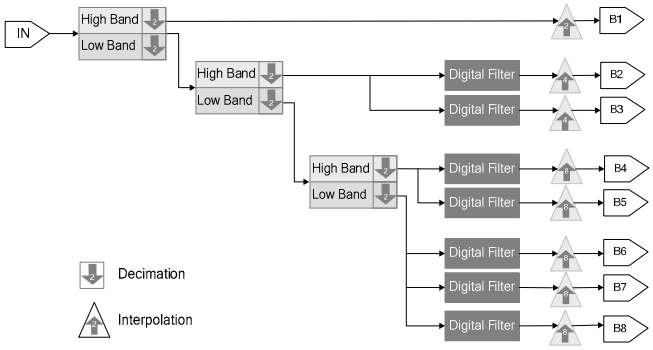

Fig. 5. A Multi-rate Multi-stage System

region; therefore, bandwidth of the filter banks is distributed in such a way that narrow bands are set for lower frequencies while relatively wider bands are set for higher frequencies. However, narrow bandwidths give rise to narrow transition widths which implies high computation cost for a single filter. To solve the problem of narrow transition width and high computation cost, the concept of multirate, multistage filtering can be used.

A multirate filter decreases or increases the input sample rate, resulting in an output rate different from the input rate. Higher frequencies imply evaluation of more samples/unit time which results in higher load on the filter implying a higher cost and vice versa for low frequencies. A multistage filter, on the other hand, consists of several filters connected in series. Together they can solve problem of narrow transition width and considerably reduce the filter cost. Figure 5 shows a bank of bandpass filters implemented from a multirate, multistage system.

To evaluate the effectiveness of the concept, a computation comparison between the filter bank implemented by FIR filters and multirate, multistage filters is made as shown in Table 1, and nearly 70% decrease in computation was observed in case of Multirate, Multistage filters.

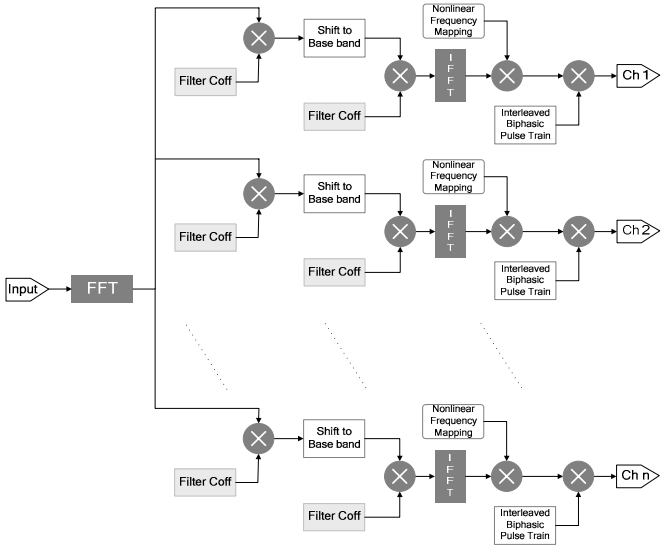

Fig. 6. Frequency Implementation of CIS

TABLE I
COMPARISON OF COMPUTATION COST OF BANDPASS FILTERS IMPLEMENTED BY 8 FIR FILTERS AND BY A MULTIRATE MULTISTAGE SYSTEM

Computation Details	8 FIR Filters	Multirate, Multistage
Number of Multipliers	257 × 8 = 2056	(65 × 6) + (37 × 7) = 621
Number of Adders	256 × 8 = 2048	(64 × 6) + (37 × 7) = 615
Number of States	256 × 8 = 2048	(64 × 6) + (37 × 7) = 615
Multiplications/ Input Sample	257 × 8 = 2056	(32 × 6) + (37 × 7) = 416
Additions/ Input Sample	256 × 8 = 2048	(32 × 6) + (37 × 7) = 416

B. *Frequency Domain Implementation*

Further improvement in cost reduction can be achieved if the complete CIS algorithm is implemented in frequency domain rather than time-domain. Essence of this methodology is the famous DSP axiom: "Convolution in Time domain is Multiplication in Frequency Domain". Computation of CIS algorithm is a multi-threaded process in hardware; about 48 simultaneous filter convolutions are under operation when CIS is implemented in time-domain. Since these filter coefficients are constant, 48 simultaneous convolutions can be bypassed by 48 multiplication operations which results in extreme reduction of cost resulting in a robust and energy efficient system. Figure 6 depicts the algorithm flow of CIS when implemented in frequency domain. Computation comparison of CIS implementation in time domain and frequency domain is given in Table 2 and 3. Number of computations per sample decrease from 3504 to 732 machine cycles.

TABLE II
COMPUTATION COST WHEN IMPLEMENTING CIS IN TIME DOMAIN

Computation Detail	Total Number of Computations
Multistage Filter/Input Sample	2120 Cycles
Envelope Detection	1384 Cycles
Total	3504 Cycles

TABLE III
COMPUTATION COST WHEN IMPLEMENTING CIS IN FREQUENCY DOMAIN

Computation Detail	Total Number of Computations
FFT/Input Sample	25 Cycles
Multistage Filter/Input Sample	286 Cycles
Envelope Detection/Input Sample	176 Cycles
IFFT/Input Sample	245 Cycles
Total	732 Cycles

V. CONCLUSION

An overview of CIS followed by simple techniques to reduce the computation cost of algorithm when implemented in software and hardware is provided here. The cost reduction techniques include implementation of filter banks through polyphase filters and programming the algorithm in frequency domain rather than time-domain. A detailed comparison accounting the total number of machine cycles for different techniques is tabulated. Evaluation of the algorithm is done by a laboratory based DSK Speech Processing Evaluation Module for Cochlear Implant Research.

REFERENCES

[1] P.C. Loizou, "Mimicking The Human Ear," *IEEE Signal Process. Mag*, *Vol. 15,* Sep. 1998, pp. 101-130.

[2] B.S. Wilson, C.C. Finley, D.T. Lawson, R.D. Wolford, D.K. Eddington and W.M. Rabinowitz, "Better speech recognition with cochlear implants," *Nature, Vol. 352,* Jul. 1991, pp. 236-238.

[3] P.C. Loizou, "Signal-processing techniques for cochlear implants," *IEEE EMBS*, vol.18, no.3, May-June 1999, pp. 34-46.

[4] P.C. Loizou, G. Stickney, L. Mishra, and P. Assmann, "Comparison of Speech Processing Strategies Used in the Clarion Implant Processor," *Ear and hearing, vol. 24,* 2003, pp. 12-19.

[5] A. Paglialonga, G. Tognola, G. Baselli, M. Parazzini, P. Ravazzani, F. Grandori, "Speech Processing for Cochlear Implants with the Discrete Wavelet Transform: Feasibility Study and Performance Evaluation", *IEEE EMBS*, Sep 2006, pp. 3763-3766.

[6] W. Nogueira, A. Giese, B. Edler, A. Buchner, "Wavelet Packet Filterbank for Speech Processing Strategies in Cochlear Implants," *IEEE ICASSP*, vol.5, May 2006, pp. V121-V124.

[7] J. Yao, Y. Zhang, "The Application of Bionic Wavelet Transform to Speech Signal Processing in Cochlear Implants Using Neural Network Simulations", *IEEE Transactions On Biomedical Engineering*, Vol. 49, No. 11, Nov 2002, pp. 1299-1309.

[8] D.B. Grayden, A.N. Burkitt, O.P. Kenny, J.C. Clarey, A.G. Paolini, G.M. Clark, "A Cochlear Implant Speech Processing Strategy Based On An Auditory Model", *IEEE ISSNIP*, 2004, pp. 491-496.

[9] N. Lan, K.B. Nie, S.K. Gao, F.G. Zeng, "A Novel Speech-Processing Strategy Incorporating Tonal Information for Cochlear Implants", *IEEE Transactions On Biomedical Engineering*, *Vol. 51,* No. 5, May 2004, pp. 752-760.

[10] Skinner MW, Holden LK, Whitford LA, Plant KL, Psarros C and Holden TA, "Speech Recognition with the Nucleus 24 SPEAK, ACE, And CIS Speech Coding Strategies in newly Implanted Adults," *Ear And Hearing*, Vol. 23, No. 3, 2002, pp. 207-223.

[11] T. J. Ahmad, H. Ali, M.A. Ijaz, S.A. Khan, "A DSK based simplified Speech processing module for Cochlear Implant Research", *IEEE ICASSP*, 2009, pp. 269-272.