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Highly Programmable Digital Controller for High-Density Epi-Retinal Prosthesis

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Abstract—**This paper presents the analysis and circuit design of a digital controller supporting up to 1024-pixel epi-retinal prosthesis. High programmability of each stimulation pixel is desirable to support various physiological conditions. The goal of this design is to achieve high programmability with limited wireless transmission bandwidth. Two-tier architecture is adopted to reduce chip area. Several circuit blocks are developed in this design: on-chip address generator (OCAG) and configuration mode reduce the data bandwidth requirement by 54.7%; flexible data parser enables the optimization between data discard rate and maximum frame rate; delay timer makes any scanning pattern possible. Multi-clock domain and data gating design are used to reduce power. A prototype 256 pixels epi-retinal prosthesis controlled by the proposed digital controller is fabricated in a 0.18μm CMOS HV technology. This digital controller can be used in other implantable multi-channel stimulation systems.**

I. Introduction

Reserach on prostheses using functional electrical stimulation (FES) has made great progress in many different applications, including cochlear implants [1], bladder controllers [2], and retinal prostheses [3] – [5]. Patients suffering from incurable blindness diseases lose their vision due to degeneration of the light sensing photoreceptor cells. Retinal prostheses induce artificial visual perception by applying electrical pulses on the retina through hundreds of electrodes.

Epi-retinal prosthesis is composed of external and internal units. The camera at the external unit captures the image and transmits it to the internal unit through wireless data telemetry. The stimulator integrated circuit (IC) implanted in the eyeball receives power and data wirelessly, and translates the image data into electrical current stimuli. The quality of the artificial visual perception is determined by both the stimulation frequency (frame rate) and the number of stimulation pixels. The research in [6] showed that at least 1000 pixels are required to restore important visual functions, such as face recognition and reading. Also, the minimum refresh rate for a steady and flicker-free vision is 60 frame-per-second (fps) [7].

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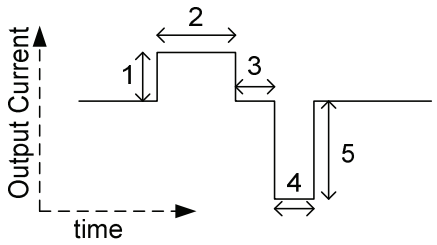

Fig. 1 Current-based bi-phasic stimulation waveform. Independently programmable parameters are labeled with numbers.

Consequently, our design is targeting at 1000-pixel, 60fps.

The paper is organized as follows: digital controller requirements are analyzed in Section II. Architecture and circuit design of the digital controller are presented in Section III, followed by the chip implementation and testing results in Section IV. Section V concludes this work.

II. Digital Controller Requirements

For an epi-retinal prosthesis interfacing with human tissues, high programmability is important to adapt to each individual, which leads to a high data bandwidth requirement. Reducing the data bandwidth requirement can lower system power and the design complexity of wireless data link. To prevent any potential errant stimulation, error detection mechanisms are essential for safety consideration.

A. Programmability and Flexibility

There are two levels of programmability in epi-retinal prosthesis system: pixel level and frame level. The former decides the stimulation waveform and the later provides different scanning patterns. Fig. 1 illustrates some stimulation parameters of an output bi-phasic pulse, including pulse width, pulse amplitude, and inter-phase delay. Pixel level programming bits also includes other information, such as leading pulse polarity, charge cancellation enabling bit, and current mirror gain control. In this design, the resolution of the stimulation parameters is defined based on the information collected from experiments by Dr. James Weiland and Second Sight Inc. The parameters of each pixel are defined 32-bit long.

Frame level programming bits set the relative activation timing of all pixels. Activating all pixels simultaneously

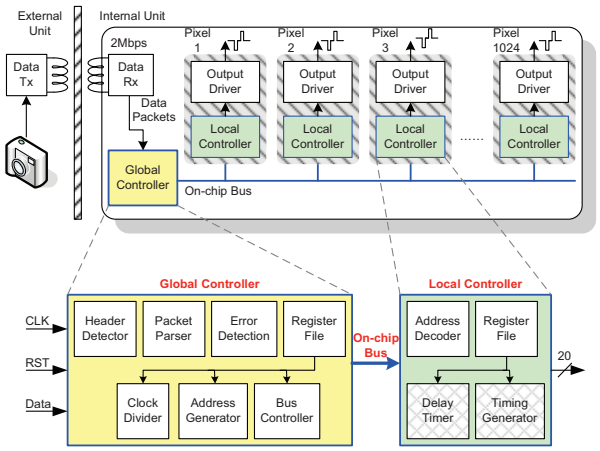

Fig. 2 Upper: data path of the epi-retinal prosthesis; lower: block diagram of the two-tier (global and local) digital controller. The meshed functional blocks in the local controller is operating at lower frequency to reduce power consumption.

causes a power surge. Because big storage capacitance is unavailable due to limited space in epi-retinal prostheses, the power surge may result in system failure in extreme cases. By sequentially activating all pixels over the entire frame cycle in a specific pattern, we can reduce the strong instantaneous peak current. Two dedicated pattern matrices are used in [5] to support two activation sequences, or scanning patterns. Delay timers are used in this work to support various scanning patterns.

B. *Minimize Data Bandwidth Requirement*

High programmability implies more stimulation parameter bits for each pixel. Supporting a high-density stimulator by simply increasing the data telemetry bandwidth can be both area- and power-consuming. A stimulator having 1024 pixels requires 10-bit address to identify each pixel, so the data amount for each pixel per frame is 42 bits (32 for stimulation parameters; 10 for address). To support 60 frame-per-second (fps) in this system, the minimal data bandwidth is 42(bits) x 1024(pixels) x 60(fps) = 2.58Mbps. On-chip address generation (OCAG) and configuration mode are developed in this work to support high programmability and minimize the data bandwidth by 54.7%.

C. *Data Integrity to Guarantee Safety*

Safety is crucial for all implantable devices. For epi-retinal prosthesis implanted in the eye, data error during transmission can cause errant stimulations and damage the delicate retinal cells. However, data error is inevitable in wireless transmission. Error detection methods are hence essential to prevent any unexpected operation. Error detection codes should be attached to each data packet, and the entire data packet is discarded if any bit in the packet is corrupted.

Though error detection codes can prevent errant stimulation, a significant amount of data may be discarded if the bit error ratio (BER) of the wireless transmission channel is high. Since a single bit error in a data packet corrupts the entire packet, the longer data packet it is, the higher discard rate there will be. Therefore, the system should be able to adjust the data packet length according to the BER condition in order to achieve a low data discard rate.

III. Architecture and Circuit Design

The data path of the retinal prosthesis is shown in Fig. 2. Image from the external camera is processed, packed, and wirelessly transmitted. After the internal unit receives the data packets, a global controller decodes them and distributes the stimulation parameters through an on-chip bus. Similar to the Ethernet, every local controller is assigned a unique address, and each set of stimulation parameters running on the bus comes with an address. Local controllers catch the parameters from the bus when two addresses match. Timing generator in the local controller produces control signals for output current driver based on the stimulation parameters. Bi-phasic electrical pulses from the current drivers stimulate the retina and elicit artificial vision. The detail implementation is explained below.

A. *Two-tier Architecture and In-pixel Delay Timer for High Programmability*

A global controller and numerous local controllers compose the two-tier architecture in this work as shown in Fig. 2. Every pixel has its own register file and dedicated timing generator, so it can be independently programmed to produce different current pulses. Since there are one thousand pixels on the IC, reducing the area of the local controller greatly decreases the overall chip size as well as the power consumption. Therefore, global functions, such as packet header detection, packet parsing, error detection, and clock division, are implemented in a global controller. An on-chip bus connects the global controller and pixels. In addition to area reduction, the two-tier architecture also enables the on-chip address generation (OCAG). This will be discussed in

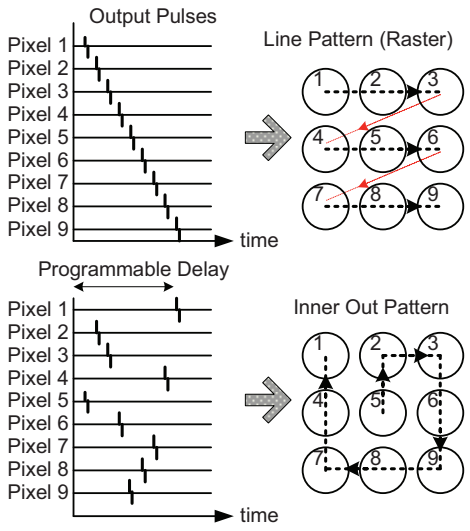

Fig. 3 Various scanning patterns can be realized by programming the delay timer in each pixel.

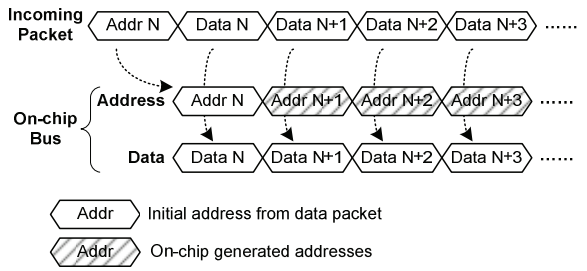

Fig. 4 On-chip address generation reduces the data bandwidth requirement for the wireless data telemetry.

the next subsection.

A delay timer is developed in each pixel, which generates a programmable delay on the stimulation pulses output. This timer enables flexible scanning patterns. The concept of the delay function is illustrated in Fig. 3. By adjusting the delay timer of each pixel, any scanning pattern can be achieved. This delay function also helps disperse the stimulation output to reduce instantaneous peak current and thus eases the design of wireless power telemetry system.

B. On-chip Address Generation for Bandwidth Reduction

On-chip address generator (OCAG) and configuration mode are applied in this system to reduce the data bandwidth/power requirement. The concept of the OCAG is shown in Fig. 4. Originally, a bandwidth of 614.4Kbps is used for pixel addressing (10(bits) x 1024(pixels) x 60(fps)). However, in most operation conditions, the data are transmitted pixel-by-pixel in the simple raster- or line-interleaving scanning order. For OCAG, only the initial address (10 bits) and an address generation mode selection (3 bits) of each data packet are transmitted. All other addresses can be generated on-chip. Rule of address generation can be programmed. For the data packets containing 1024 pixels, the bandwidth requirement for addressing is 13(bit) x 60(fps) = 0.78Kbps, which is a 99.87% reduction compared with 614.4Kbps.

To further reduce the data bandwidth, stimulation parameters are categorized into two groups: real-time and configuration parameters. While real-time parameters are transmitted every frame, configuration parameters, *e.g.* inter-phase delay and amplitude resolution, are transmitted only when needed. By applying the configuration mode, the data bandwidth required for stimulation parameters can be reduced from 1.97Mbps (32(bits) x 1024(pixels) x 60(fps)) to 1.17Mbps (19(bits) x 1024(pixels) x 60(fps)), or 40.6% reduction. After applying both methods, the total bandwidth requirement is reduced by 54.7%, as shown in Fig. 5. The term "pixel data" will be used in the rest of this paper to express 19-bit data for one pixel.

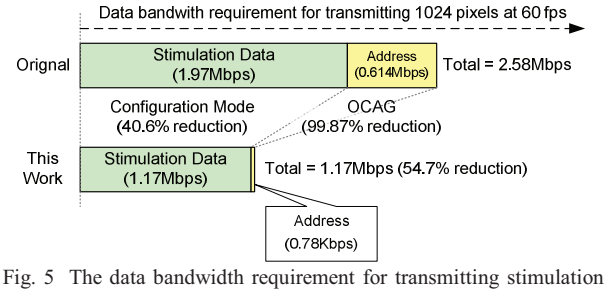

Fig. 5 The data bandwidth requirement for transmitting stimulation data for 1024 pixels at 60 fps is reduced from 2.58Mbps to 1.17Mbps.

C. Flexible Packet Length Enabling Tradeoff between Frame Rate/Pixel Discard Rate

Unexpected operation due to data transmission error can be prevented by the error detection methods implemented in this work. The packet parser in the global controller performs checksum and cyclic redundancy check (CRC) on every incoming data packet, and the entire data packet will be discarded if any bit in the data packet is corrupted.

Data discard rate due to transmission error is proportional to the data packet length as discussed in Section II.C. Analysis in Fig. 6 (right axis) shows that for a given BER, the average number of pixel data discarded per frame is much smaller for short packets than long packets. The short packets, however, increases the total data amount due to the overheads of each data packets, such as header marker and error detection codes. There is a tradeoff between the data amount per frame and the data discard rate for a given BER. Since the BER varies from the eyeball thickness, noise, and interference, a pre-defined packet size during circuit development may not be suitable for all circumstance.

Flexible data packet length is supported in the work. The data packet parser is developed to support any data packet size which is the power of 2 between 1 to 1024. Therefore, doctors can determine the optimal packet size based on the real BER after the system is implanted. Small data packets, although providing better data protection, increase the data amount of each frame, and the maximum frame rate for a given data bandwidth is hence lowered. The relationship between maximum frame rate and packet size is shown in Fig. 6 (left axis). For BER=10^{-6}, changing the data packet size from 1024 to 4 pixel data per packet lowers the frame rate from 102 fps to

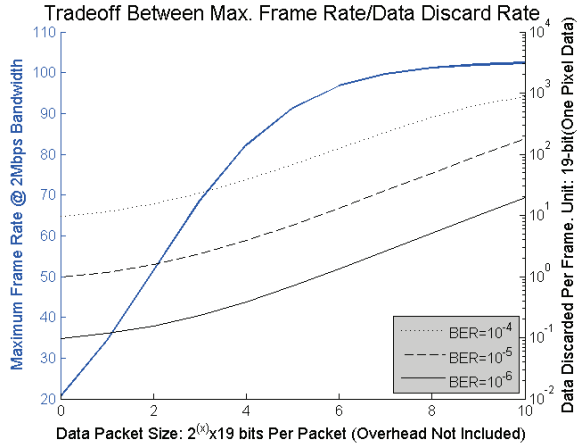

Fig. 6 For a given BER, the pixel discard rate can be lowered by reducing the data packet size. The tradeoff is lower maximum frame rate.

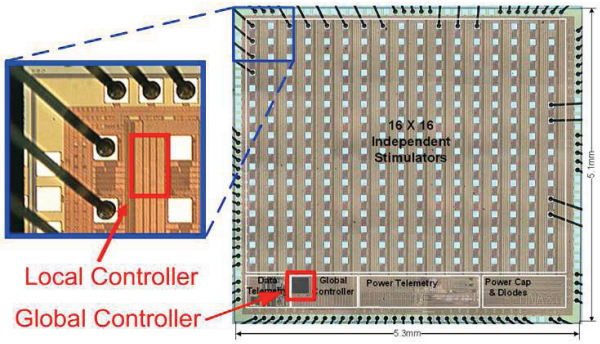

Fig. 7 The digital controller in the micrograph of the 256-pixel retinal prosthetic IC. The local controller in the inset is underneath the top metal layers, so the detail cannot be seen.

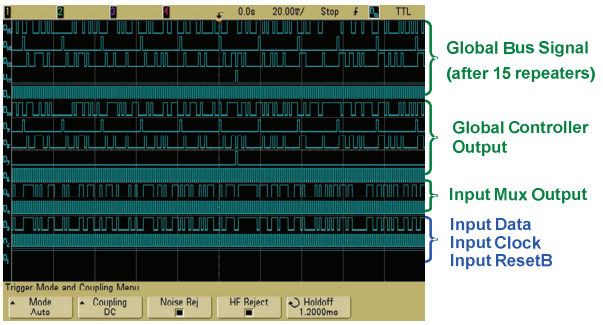

Fig. 8 The measurement results from the prototype IC. Input test signals (D1~D3) are sent to the digital controller directly, bypassing the data demodulator. Global controller output signals (D6~D10) and global bus signals (D11~D15) are recorded through test pins.

51 fps, but reduces the data discard rate by ~99% (from 19.81 to 0.156 pixel data per frame). Doctors can find an optimal point for low data discard rate and minimal image flickering.

IV. Implementation and Testing

Multi-clock domain and data gating design techniques are employed in this work to reduce the power consumption. Due to the physiological nature of retina, a temporal resolution of the output stimulation pulses as fine as the data clock period, *i.e.* 0.5 microsecond, is less meaningful. Therefore, a slow clock domain is used in the circuit blocks related to the output timing generation, including the delay timer and the timing generator. A programmable clock divider in the global controller produces the slow clock from the 2MHz data clock. For testing consideration, ad hoc test pins are added into this design for direct test pattern feeding and intermediate signal observation.

This controller is designed and synthesized using 1.8V, 0.18µm digital cell library. The core area of the global controller is 262x287µm^2; the core area of the local controller is 84x221µm^2. Since the controller is designed using Verilog HDL, it can be easily synthesized into 90nm technology to further reduce the area by three times.

A prototype IC with 256 pixels, each of which contains a local controller and a current driver, is fabricated using TSMC 0.18µm CMOS HV process as shown in Fig. 7. HV process is chosen because the high voltage transistors are required to achieve high compliance voltage at the output current drivers, which has been discussed in [4]. The digital controller in this IC has been bench top tested. Input test patterns are generated from a National Instrument data acquisition device (NI USB-6259) and fed into the digital controller through test pins. The output signals of each functional block are recorded using an Agilent logic analyzer (MSO6054A). The measurement result is shown in Fig. 8. A thorough test has verified that every block of the digital controller on the Retina8.0 chip works correctly.

V. Conclusion

The requirement analysis for digital controller based on the characteristics of the high-density epi-retinal prosthesis has been discussed in this paper. Detailed circuit design for global and local controllers has also been presented. This modular design supports up to 1024-pixel stimulation system. A prototype 256-pixel epi-retinal prosthetic IC has been fabricated and tested. This work can be transferred into more advanced technology for area reduction and/or applying clock gating for further power reduction in the future versions. The analysis and circuit design described in this work can also be applied to other implantable multi-channel stimulation systems requiring wireless data telemetry.

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