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Six-Channel Neural Signal Regeneration Integrated Circuit

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***Abstract*—A six-channel neural signal regeneration integrated circuit (IC) was designed and fabricated in CSMC's 0.5-μm CMOS technology. The circuit consists of a low-noise and high common mode rejection ratio (CMRR) instrument amplifier, an inverted operational amplifier (OPA) and a buffer. The six-channel IC occupies a die area of 1.9mm×1.6mm. The testing result shows that the consumption of a single channel is less than 5 mW, and the output voltage swing reaches 5 V under ±2.5V power supply，the gain can be adjusted from 60dB to 110dB. The circuit has been used for in-vivo experiments on toad's nerve with electrodes to regenerate neural signals. Different neural signals have been successfully regenerated on toad's nerve and corresponding actions have been observed.**

I. Introduction

After nerve bundles are injured, the organism has lost the related motorial and sensory function, since neural signal channels are interrupted. There are two biological methods utilized for this purpose: to replant cells and organs and to lead the growth orientation of nerves by nutrition. But these methods have been proved helpless for most spinal cords injuries.

An idea for recovering the function of an injured spinal cord is using microelectronic techniques to create an in-body embedded circuit module to regenerate the interrupted signal channels of the spinal cord [1]. In last years, several modules have been designed by using commercial ICs and discrete devices, which are already used for in-vitro animal experiment.

The module includes two electrode arrays and a neural signal regeneration circuit which realize neural signal detecting and functional electrical stimulation (FES) [2]. The neural signal detecting microelectrode arrays detect neural signal on damaged end of nerve, and send them to the neural signal regeneration circuit. In there, the neural signal is amplified to appropriate amplitude, and then applies it to neural stimulating microelectrode array which linked to the other end of the damaged nerve. So that neural signal can be transfer by the electronic signal channel [3-4].

Using the circuit principle as discrete devices, a neural signal regeneration IC has been designed and fabricated in the CSMC's 0.5-μm CMOS technology.

In this paper, a six-channel low-noise, low-power CMOS neural signal regeneration IC with adjustable gain is presented.

II. Circuit Design

Between micro-electrode array and neural interface there is a voltage offset which amplitude is about 1~2 V [5]. There is also a strong animal electromyography (EMG) signal, biological background noise, thermal noise of neural electrode. However, the neural signal from extracellular recording is very weak. The signal noise ratio (SNR) is about -60 dB [6]. Therefore, it is essential for neural signal detecting circuit to eliminate outside interference and improve SNR.

The structure of a single channel IC is shown in Fig. 1. It contains two parts: detecting circuit and FES circuit [3, 6]

An RC network and a low-noise high CMRR instrument amplifier constitute the detecting circuit which receives the neural signal from the electrode on the upper end of injured nerve. The off-chip RC network is the first stage and made up of two capacitances and four resistances,which realizes the AC coupling for differential signal and provides a DC bias for the next amplifier at the same time. The second stage is an instrument amplifier which is composed of three the same OPAs A1. The neural signal has an amplitude in the range of 10 μV to 1 mV, and a spectrum from 100 Hz to 4 kHz. So the detecting circuit should meet the adjustable gain and its 3dB bandwidth is larger than 4KHz. Rg is an off-chip resistor which used to adjust the amplifying factor.

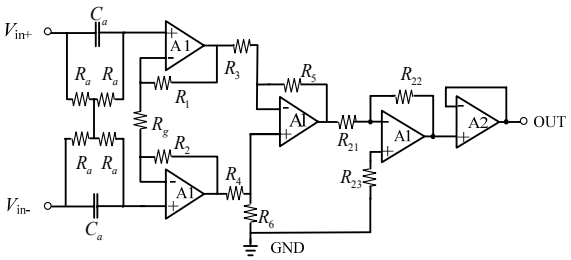

Fig.1 Neural signal regeneration circuit

An inverter-configurated OPA and a voltage buffer constitute the FES circuit. The OPA amplifies the detected signal further and transmits the simulated signal to the lower end of injured nerve by the buffer. According to different demands of detecting and stimulation circuit, two kinds of OPA have been designed to realize the respective function.

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A. Operational Amplifier A1

The instrument amplifier used to achieve the biological signal detection. Its most important features include noise, power, and common-mode rejection. The input stage is very important owing to the noise performance. Due to the lower noise coefficient than that of NMOS, PMOS transistors were used as input transistors. Input differential pair in weak inversion is also beneficial to the noise performance besides the advantage of minimizing the overall offset. In the first stage, a telescopic cascode OPA was chosen for the OPA, since a telescopic one has a higher gain, a lower power and a lower noise than a folded cascade one[6]. The disadvantage of lower output swing of a telescopic OPA is offset by using a second stage with a larger output swing. The schematic for the 2-stage telescopic cascode OPA is shown in Fig. 2.

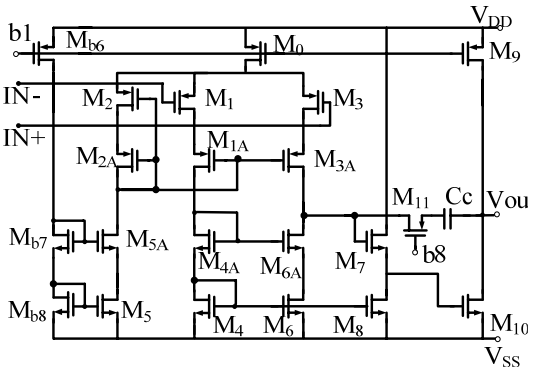


Fig.2 Schematic of the operational amplifier A1

Compared with the first stage, the input-referred noise of the second stage of OPA1 can be omitted. The noise in cascode transistors typically contributes little to the overall noise in OPA, so M1, M3, M4 and M6 are the main noise sources. The simulation results indicate that in the frequency range from 100 Hz to 4 kHz , the equivalent input noise of opa A1 is 18.5nV/sqrt(Hz) (not contain 1/f noise for the technology does not provide 1/f noise model), and the gain of A1 can reach 102.4 dB, CMRR reaches 134 dB, the power consumption of the system is 0.72 mW with the power supply of ±2.5 V.

B. Operational Amplifier A2

In the buffer stage, taking the requirements of larger input common-mode (CM) range and low output resistor into account, we designed a rail-to-rail input stage, constant-gm OPA to be a unity-gain buffer. A typical constant-gm input stage for a rail-to-rail OPA consists of a PMOS differential pair and an NMOS differential pair as shown in Fig. 3. To obtain a constant-gm over the whole CM input range, an electronic zener diode (constituted by the transistors MZ1~MZ5 in the dashed area of Fig. 3) is inserted between the tails of the complementary input pairs [7-8].

The total transconductance gmtol is given by

$$g_{mtol} = g_{mn1} + g_{mp1} = K(V_{OVn1} + KV_{OVp1}) \quad (1)$$

$$V_{OV} = \sqrt{I/K} \quad (2)$$

where Vov is the effective gate-source voltage of an input transistor, the factor K is the transconductance parameter of the input transistors and equal to

$$K = \frac{1}{2}\mu_N C_{OX}\left(\frac{W}{L}\right)_N = \frac{1}{2}\mu_P C_{OX}\left(\frac{W}{L}\right)_P \quad (3)$$

Vcon is the sum of gate-source voltages of input pairs, which is given by

$$V_{CON} = -V_{TP} + V_{TN} + KV_{OV} \quad (4)$$

The electronic zener diode keeps Vcon constant, and therefore, the total gm of input stage is constant.

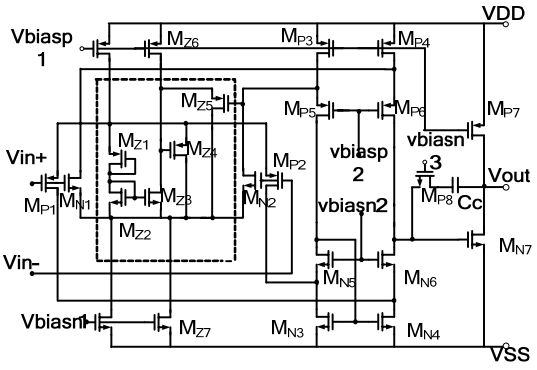


Fig. 3 Schematic of the operational amplifier A2

Two complementary diode-connected transistors MZ1 and MZ2 form a reference chain. The current through this chain is set by W/L of MZ1, MZ2 and the voltage across the chain. MZ3 and MZ4 form two transistor gain stages. MZ5 controls the tail currents and the gate-source voltages of input pairs. The total transconductance gmtol versus the CM input voltage is shown in Fig. 4. From this figure we can be concluded that gmtol varies only 7.8% over the entire CM input voltage range. The variation of gmtol is caused by the fact that the voltage across the electronic zener is slightly of current dependent. The main advantage of this constant-gm rail-to-rail input stage is very power-efficient compared to other methods.

III. RESULTS AND ANALYSIS

Since neural signals exist in many neural channels, the chip must be a multi-channel neural signal regeneration

circuit. Therefore, six copies of the same circuit described above are integrated on one chip. The whole six-channel IC occupies a die area of 1.9mm×1.6mm. The photomicrograph of the chip is shown in Fig. 5.

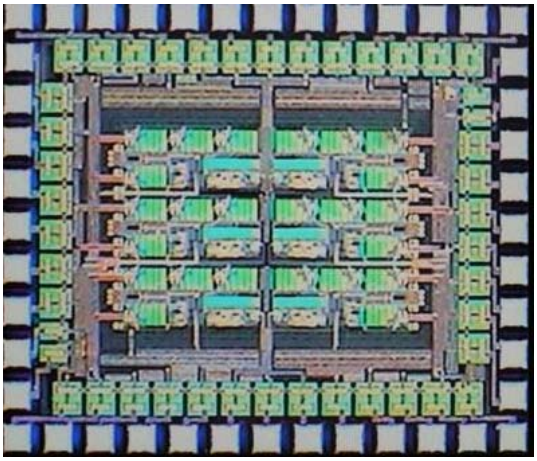


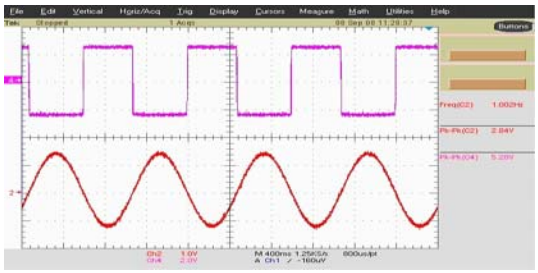
Fig.5 Photomicrograph of the chip

All circuits are simulated in Synopsys Star Hspice and Cadence Spectre. The test results indicate that a signal channel power consumption is less than 5 mW, the output swing is about 5 V with the power supply of ±2.5V. Table 1 gives simulation and neural signal regeneration circuit test results.

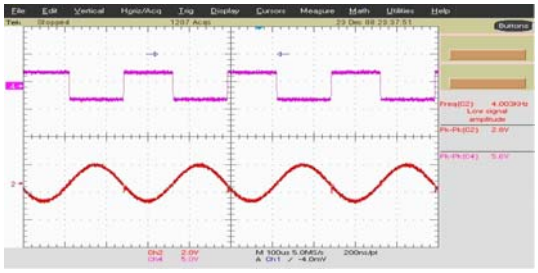
Table 1 Results of the neural signal regeneration circuit

Parameters	Simulation results	test results
power voltage (V)	±2.5	±2.5
Output range (V)	-2.5~+2.5	-2.5~+2.5
gain (dB)	58~111	58~109
GBW (MHz)	7.68	>5
3dB Bandwidth (kHz)	>8	>4
Power (mW)	3.62	<5
Input offset voltage (mv)	<0.01	<2

The output waveform of neural signal regeneration IC is shown in Fig. 6, input signal is sinusoidal signal from 1Hz ~ 4kHz, VINp-p = 25 mV, The gain of the detecting circuit can be modified through changing the off-chip resistor Rg. when Rg=4kΩ, the gain of the entire circuit is 114 × 106, the amplitude of output waveform will be limited.



(a) f =1Hz



(b) f =4 kHz

Fig. 6 Output signal waveforms at different frequencies of input signal

IV. ANIMAL EXPERIMENT

After packaging, the circuit has been used for in-vivo experiments on toad's nerve with electrodes to regenerate neural signals.

Neural signal regeneration experiments were carried out in the Institute of RF- & OE-ICs of Southeast University. Two pair of acupuncture electrodes was inserted into the left leg nerve of one toad to detecting the neural signal. One was connected with oscillograph to monitor the neural signal of the toad; the other was connected with the neural signal regeneration IC. The IC connected with a stimulating electrode which was a pair of acupuncture electrodes inserted into anther toad's left leg nerve. After dropping 1% sulfuric-acid on the left foot of the first toad, the left leg of the toad moved flinching due to conditioned reflex. The neural signal was detected and displayed on the oscillograph. The neural signal regenerated by the neural signal regeneration IC was sent to the second toad's left leg nerve through the stimulating electrode. The left leg of the second toad made the similar action like to the first toad. The neural signal of the left foot of second toad also monitored with the oscillograph. Now the circuit achieves the goal of neural signal regeneration.

V. CONCLUSION

A six-channel low-noise, low-power CMOS neural signal regeneration IC with adjustable gain for biomedical applications is presented. The circuit is designed and fabricated in CSMC's 0.5-μm CMOS process. The test results meet the demands of micro-electronic-aided neural signal regeneration system. In the animal experiment, the neural signal is successfully regenerated.

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