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A 1μW 85nV/√Hz Pseudo Open-Loop Preamplifier with Programmable Band-Pass Filter for Neural Interface System

Sun-Il Chang and Euisik Yoon

Abstract—**We report an energy efficient pseudo open-loop amplifier with programmable band-pass filter developed for neural interface systems. The proposed amplifier consumes 400nA at 2.5V power supply. The measured thermal noise level is 85nV/√Hz and input-referred noise is 1.69 μV_{rms} from 0.3Hz to 1 kHz. The amplifier has a noise efficiency factor of 2.43, the lowest in the differential topologies reported up to date to our knowledge. By programming the switched-capacitor frequency and bias current, we could control the bandwidth of the preamplifier from 138 mHz to 2.2 kHz to meet various application requirements. The entire preamplifier including band-pass filters has been realized in a small area of 0.043mm^2 using a 0.25μm CMOS technology.**

I. Introduction

With advances in CMOS technology, there has been a significant progress in implementing multichannel implantable neural systems which will potentially enable us to diagnose disease and establish a direct interface between brain and external electronic devices [1,2]. However, chronic monitoring of the brain activities, such as neural spikes, EEG, ECoG, etc., is still a challenge, especially, in the wireless ambulatory systems due to stringent constraints in power, noise and area for hardware implementation.

Typically, field potentials (in EEG, ECoG) contain most of important information in the bandwidth between 0.5Hz and 300Hz with amplitude ranges from 1μV to 100μV, where thermal and 1/f noise can severely interfere with the signal. To establish the reliable monitoring of vulnerable neural signals, front-end preamplifier is one of the most critical components which determine the signal-to-noise ratio of the entire system. Preamplifiers should meet the stringent requirements of low noise (<100nV/√Hz) for reliable measurement of weak signals, low-power consumption (<2μW) for chronic operation, and small area (<0.1mm^2) for multichannel systems. Furthermore, the interference at the electrode interface induces a huge DC offset and drift which can be easily up to 1~2V and changes over time at very slow frequency (<0.1Hz). This huge offset must be suppressed to prevent the saturation of the amplifier.

Previously, many preamplifier circuit techniques have been reported in the literature [3-10]. In order to achieve high noise-power efficiency, most amplifiers utilize closed-loop topologies with input transistors operated in subthreshold region where the g_m/I_d can be maximized [3-6]. However, these closed-loop amplifiers impose the stability constraint which results in the limit to the power-noise efficiency. The low-power open-loop amplifier has been proposed by Holleman [10]; however, single-ended output is susceptible to common mode noise and supply fluctuation.

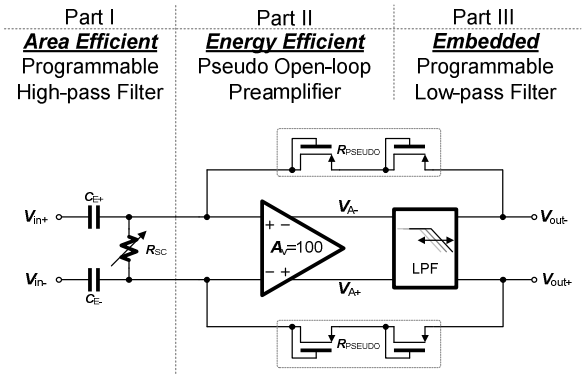

Fig. 1: The overall structure of the preamplifier

To suppress the electrode interface interferences, a simple passive high-pass filter (HPF) is widely utilized using a large input capacitor (10~20pF) which occupies most areas in the preamplifier. To address this, several other low-frequency suppression techniques have been introduced [7-9]. However, the low-frequency corners of these amplifiers are not controllable. Parthasarathy *et al* reported the feed-forward method by implementing a high-pass filter (HPF) with a low cut-off frequency (~0.5Hz) in a small area [8]. However, the cut-off frequency is difficult to control and vulnerable to process variations.

In this paper, we propose a low-power pseudo open-loop preamplifier combined with an on-chip programmable BPF in a small area. The proposed pseudo open-loop preamplifier can retain a high linearity and stable operation over process and bias variations. We have implemented the programmable BPF composed of a switched-capacitor (*S-C*) HPF and an embedded g_m-*C* low-pass filter (LPF). In the HPF filter we can significantly reduce the area by utilizing the intrinsic parasitic capacitance in the electrode. The cut-off frequency is programmed by changing *S-C* frequency (F_{SC}). In the g_m-*C* LPF, the high cut-off frequency can be tuned by the transconductance gain (g_m) in the output stage.

II. The Proposed Pseudo Open-loop Preamplifier

A. Overall Preamplifier Scheme

The proposed preamplifier consists of three parts as shown in Fig. 1. In part I, an area-efficient programmable *S-C* HPF utilizes the parasitic capacitance of the electrode (C_E) as well as the *S-C* resistor (R_{SC}). The *S-C* HPF can provide a

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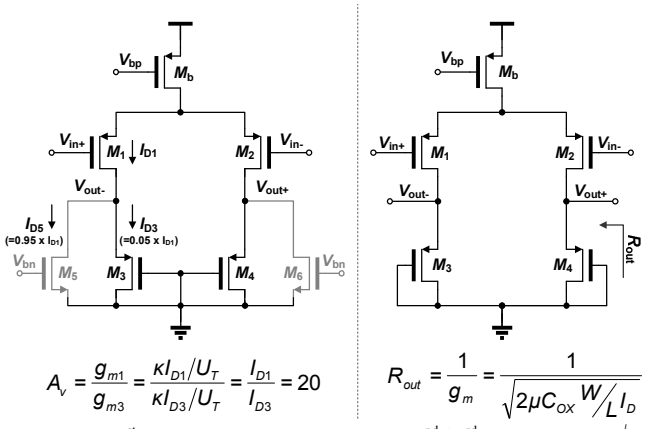


(a) 1st Stage (Gain = 20) (b) 2nd / 3rd Stages (Gain = √5)

Fig. 2: Schematics of each stage in diode-connected load configuration.
(a) 1st Stage: weak inversion operation (Current-ratio Gain),
(b) 2nd/3rd Stages: strong inversion operation (Dimension-ratio Gain)

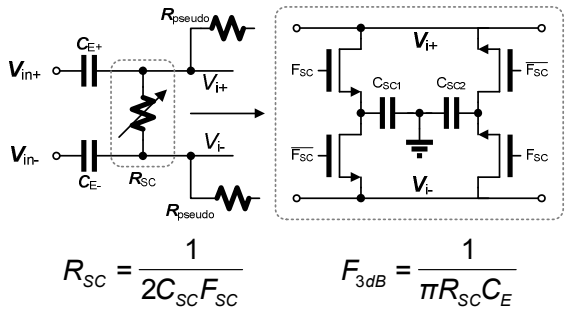


Fig. 3: Schematic of the implemented high-pass filter with a controllable cut-off frequency below 1Hz using electrode capacitor (C_E) and switched-capacitor resistor (R_{SC})

relatively accurate frequency response because R_{SC} can be easily controlled by *S-C* frequency (F_{SC}). Large parasitic electrode capacitance (C_E) is used to cut off the DC interference at the electrode-tissue interface. In part II, a fully-differential pseudo open-loop preamplifier is realized to amplify weak brain signals. As shown in Fig 2, the overall amplifier has three stages to provide the total gain of 100: the gain of 20 from the first stage and another 5 from the second and third stages. It should be noted that the feedback path through the R_{pseudo} (shown in Fig. 1) acts as a unit gain feedback only in the very low frequency range because it forms a low-pass filter with C_E. The feedback factor, β, can be given as $1/(1+sR_{pseudo}C_E)$). As a result, the proposed preamplifier operates as a simple open-loop amplifier above $\omega=1/R_{pseudo}C_E$. In part III, output impedance ($=1/g_m$) of the third stage forms an embedded g_m-*C* LPF. By adjusting the bias current of the third stage (thus changing g_m), the preamplifier can eliminate any undesirable noise signals above the cut-off frequency.

B. High Linearity Design

Linearity is one of the main concerns in open-loop topology. To provide high linearity while maintaining the same power-noise efficiency, we utilized the diode-connected load transistors operating in weak inversion region at the first stage (Fig. 2). In the following stages, the transistors are operating in strong inversion to minimize any noise

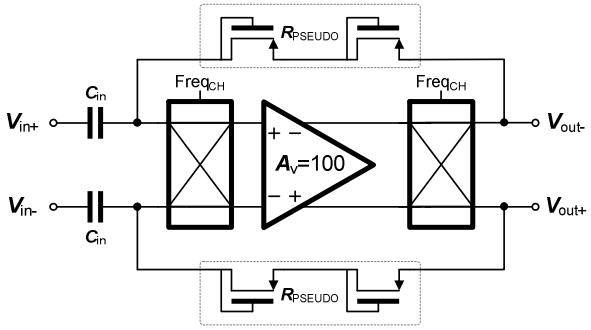


Fig. 4: Chopper stabilized preamplifier to suppress 1/f noise

contribution. Because the gain of the first stage is set by the current ratio between the input and load transistors, we utilize the current-steering sources ($M_{5,6}$) to accurately set the gain:

$$A_v = \frac{g_{m1}}{g_{m3}} = \frac{\kappa I_{D1}/U_T}{\kappa I_{D3}/U_T} = \frac{I_{D1}}{I_{D3}} = 20,$$

where $I_{D1}=I_{D3}+I_{D5}$. The first stage consumes the most of the supply current (I_{D1}:$I_{D7,11}$ =10:1) to give high power-noise performance. To minimize any possible process mismatches, we used PMOS transistors for both input (M_1, M_2) and load (M_3, M_4) transistors. Long-channel transistors (L=100μm) are used for current-steering sources ($M_{5,6}$) to reduce gain offsets, which will be explained in the next section. The measured frequency responses show a very stable mid-band gain for various supply current variations.

C. Energy Efficient Design

The power-noise efficiency can be analyzed by input-referred noise in the first stage since the noise contributed from the following stages is negligible due to the high gain of the first stage. Here, the input-referred noise can be given by the EKV model [1] as

$$\overline{v_n^2} = \frac{4kT}{\kappa \cdot g_{m1}}\left(1+\alpha_3\frac{I_{D3}}{I_{D1}}+\frac{4\kappa}{3}\alpha_5\frac{I_{D5}}{I_{D1}}\right) \approx \frac{4kT}{\kappa \cdot g_{m1}}\left(1+\frac{1}{A_{V1}}+\frac{4\kappa}{3}\frac{1}{\sqrt{IC_5}}\right)$$

where $\alpha_n=2/(1+\sqrt{(1+4*IC_n)})$, κ is the subthreshold gate coupling coefficient, and IC is inversion coefficient which is inversely proportional to the W/L ratio of transistors. In this analysis, we do not include 1/f noise because 1/f noise can be suppressed by other techniques using a chopper. We can draw useful design criteria from the equation given above. In order to minimize the input-referred noise, the gain in the first stage should be maximized, and the W/L ratio of M_5 and the g_m of the rest of transistors be minimized to reduce their noise contribution. In our design, we adopt a pseudo open-loop topology to meet all the design criteria without introducing instability. We set the gain of the first stage to be 20 and the W/L of M_5 to be 1/100. We design all the rest of transistors operating in strong inversion except for the first stage. The simulation results show that the input-referred noise of the proposed preamplifier is 78.4nV/√Hz with a noise efficiency factor (NEF) of 2.3 for I_{total}=400nA.

D. Programmable Band-pass Filter

In neural signal monitoring we should cut off low frequency signals to suppress the electrode offset voltage and

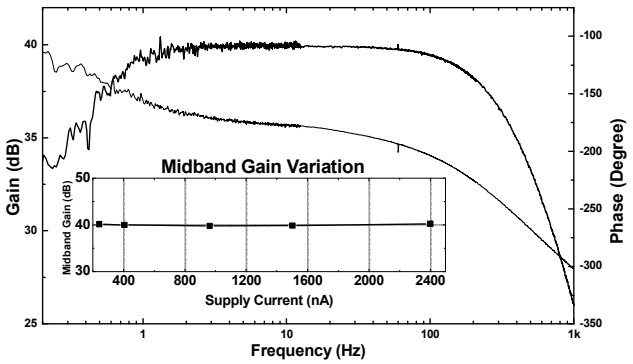
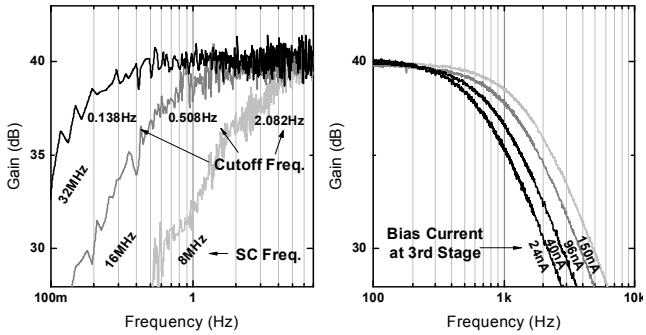


Fig. 5: Frequency response of the pseudo open-loop preamplifier with a bandwidth from 0.5 Hz to 292 Hz for EEG application. The mid-band gain variation is also negligible for supply current ranging from 240nA to 2.4μA



(a) S-C HPF (b) g_m-C LPF

Fig. 6: Frequency response of the programmable HPF and LPF.

drift. Fig. 3 shows the *S-C* HPF that we implemented by utilizing the electrode capacitance (C_E). The electrode capacitance is relatively large (> 5 nF), therefore, we can easily implement a low cut-off frequency (<0.1 Hz) without using an external capacitor. The cut-off frequency can be controlled by a RC network formed by C_E and R_{SC} where the *S-C* resistance (R_{SC}) is determined by F_{SC} and C_{SC}. To minimize the impedance mismatch and charge injection in the differential signal lines, we implemented the paired R_{SC} switched by quadrature phases. The cur-off frequency can be programmed by adjusting the *S-C* frequency, F_{SC}. Combined with the embedded g_m-C LPF at the third gain stage (explained in *section II-A*), we can form a complete band-pass filter. This bandwidth programmability allows the proposed amplifier to be applied for various neural interface applications, such as EEG, ECoG, local field potential, neuroprostheses, BCI, etc.

E. 1/f Noise Reduction by Chopper Stabilization

In addition to thermal noise, 1/f (or flicker) noise severely interferes with the low-frequency neural signals in EEG and ECoG applications. To reduce the 1/f noise, we used the large PMOS transistors (W/L=200 μm/1μm) in the first stage. PMOS transistors typically show better noise performance than NMOS counterparts. However, we still have relatively large 1/f noise from $M_{3,4}$ which is designed to be relatively small in order to optimize the gain and bandwidth. To suppress the 1/f noise furthermore, we have implemented a chopper as shown in Fig 4.

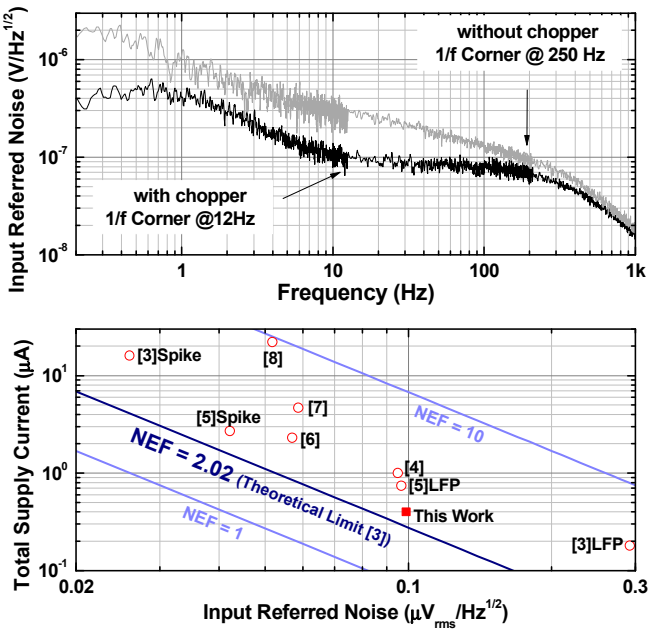


Fig. 7: Measured input-referred noise with and without chopper operation and noise efficiency factor (NEF) comparison graph with previous approaches reported in the literatures.

III. Measurement Results

A. Test Bench Measurement

The proposed preamplifier is fabricated using 0.25μm 1P5M CMOS process. The overall power consumption is 1μW (400nA at 2.5V supply). Fig. 5 shows the measured frequency response of the fabricated pseudo open-loop preamplifier. It shows a stable mid-band gain of 40.01±0.2dB for various supply currents from 240nA to 2400nA. To verify the process variation, the gain variation was measured from twenty chips and we observed a variation of 39.95±0.53dB. These results show the proposed preamplifier has a stable gain over the bias and process variation. Fig. 6 (a) shows the frequency response of the *S-C* HPF. To verify the operation, we assume the electrode capacitance (C_E) is 10μF in 20mm^2 and *S-C* capacitance (C_{SC}) is 1pF. By changing the *S-C* frequency of 8, 16, and 32 MHz, we could modulate the cut-off frequency to 0.13, 0.598, and 2.082 Hz, respectively. Fig 6 (b) shows the frequency response of the programmable g_m-C filter for various bias currents in the third stage from 24 nA to 150nA. In Fig 7 shows the noise performance of the proposed amplifier compared with the previous literatures. By enabling the chopper, 1/f corner frequency is reduced by twenty times from 250Hz to 12Hz. Performance of the preamplifier is summarized in Table 1. The measured thermal noise level is 85nV/√Hz and the input-referred noise is 1.69μVrms from 0.3Hz to 1 kHz. The fabricated preamplifier has achieved the best NEF value of 2.43 among the differential topologies reported up to date to our knowledge. The total harmonic distortion (THD) is measured below 1% when the input signal of 2.25mV @ 100 Hz is applied. The measured CMRR and PSRR are 79 dB and 82 dB, respectively, and the dynamic range is 53.5 dB. The fabricated preamplifier occupies the small area of 0.043mm^2.

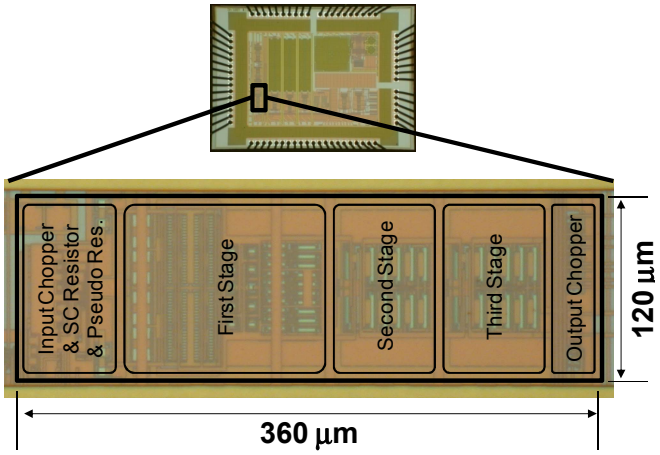


Fig. 8: Microphotograph of the fabricated preamplifier in a test chip.

Parameter	Measured
Technology	0.25µm 1P5M CMOS
Supply Voltage	2.5 V
Total Current	0.4µA
Gain (Average±σ, 20 chips)	39.95 ± 0.53 dB
Bandwidth	0.51 ~ 292 Hz
Input-referred Noise	1.69 µVrms
Noise Efficiency Factor	2.43
THD	< 1 % (2.25mVpp @ 100 Hz)
Dynamic Range	53.5 dB
CMRR	79 dB
PSRR	82 dB
Area	0.043 mm²

Table 1. Performance Summary Table

The microphotograph of the fabricated preamplifier is shown in Fig. 8.

B. In-vivo EEG Measurement

To evaluate the performance of the fabricated preamplifier, *in-vivo* EEG signals of a human subject have been measured. Fig. 9 shows the recorded waveform and its spectrogram of a subject while blinking the eyes. During eye-closed periods, we observed α-waves in 8–12 Hz bandwidth which is a typical brain activity in the absence of visual stimulus [10]. Eye lid motion artifact can be distinctly shown during the recording session indicated by the red arrows in Fig. 9.

IV. Conclusion

We have proposed, designed, fabricated and fully characterized a low-power pseudo open-loop preamplifier with a programmable band-pass filter for neural interface systems. The proposed amplifier consumes 400nA at 2.5V power supply and the total chip area is 0.043mm^2. The measured thermal noise is 85nV/√Hz and input-referred noise is 1.69 μ V_{rms} from 0.3Hz to 1 kHz when using a chopper stabilization technique to suppress 1/f noise. The fabricated preamplifier shows the lowest noise efficiency factor of 2.43

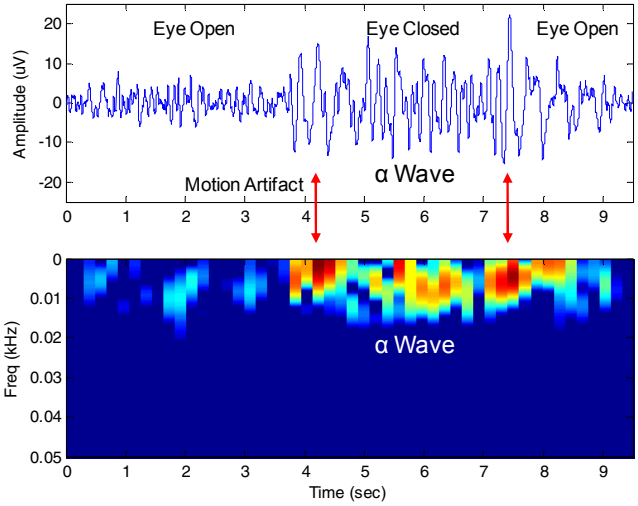


Fig. 9: *In-vivo* EEG measurement: waveform and its spectrogram

in the differential topologies reported up to date to our knowledge. We have implemented the programmable BPF by adjusting a low cut-off frequency of the switched-capacitor resistance in the input node and a high cut-off frequency in the g_m-C filter at the output stage. The bandwidth of the preamplifier can be adaptively programmed from 138 mHz to 2.2 kHz, applicable for various neural interface systems from non-invasive EEG to fully-invasive single neuron activity monitoring.

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