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Integrated Electronics for Peripheral Nerve Recording and Signal Processing

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***Abstract*—This paper describes the integrated circuit implementation of an electronic system for peripheral nerve recording and signal processing. Specifically, the system aims to record and condition neural activity from the phrenic nerve as a good indicator for breathing, and generate a stimulus trigger signal for a laryngeal pacemaker device to reanimate a paralyzed muscle with electrical stimulation paced with respiration. The 2.2 × 2.2-mm^2 integrated circuit is fabricated using the AMI 1.5 µm 2P/2M n-well CMOS process, and consumes 1 mW from ±1.5 V. System architecture, circuit design, simulation results, and measurement data in benchtop experiments are presented.**

I. Introduction

Neural activity from the phrenic nerve is often considered to be an optimal indicator for inspiratory drive, and could be used to control a laryngeal pacemaker device [1] in patients with bilateral vocal fold paralysis to reanimate paralyzed muscle via electrical stimulation controlled by a trigger signal from the sensing circuitry. In such a closed-loop operation, interface electronics have to be developed to record neural activity from the phrenic nerve, process the recorded signal, and generate an activity-dependent trigger signal for stimulator control. Such a closed-loop system has been previously proposed in [2], [3], but it is not implantable due to its discrete implementation with commercial off-the-shelf components and benchtop equipment.

Some of the most important issues in peripheral nerve recording are related to the signal itself. Peripheral nerve signal characteristics depend on the electrode type, electrode contact distance, and signal distribution rate on the nerve. In general, peripheral nerve signals are on the order of a few µV, and have significant frequency components extended to a few kHz. Given such low-level amplitudes, noise is typically a major concern in recording and, therefore, both device and ambient noise should be minimized.

Since peripheral nerve recording is typically performed close to other functioning organs such as the muscles or heart, large-amplitude biopotential artifacts such as the electromyogram (EMG) or the electrocardiogram (EKG) as well as low-frequency motion artifacts are also major sources of concern. Good electrode design practices in addition to signal filtering can reduce the effect of these artifacts on recording quality. In addition, over the past few years, researchers have utilized recording architectures such as quasi-tripole (QT) [4]-[6], true-tripole (TT) [6], and adaptive-tripole (AT) [7] to alleviate the artifact problem with varying degrees of success. In our design, a QT front-end architecture has been used as a tradeoff between its moderate artifact rejection capability and minimal recording circuit complexity [8].

In this paper, we report on the design, implementation, and benchtop measurement results from an integrated electronic system that aims to generate an activity-dependent stimulus trigger signal from bursts of neural activity on the phrenic nerve, which is theoretically a good indicator for breathing since it slightly precedes diaphragm activation. Section II describes the system architecture for phrenic nerve recording and signal processing. Section III describes the integrated circuit architecture of some of the major building blocks. Section IV presents our circuit- and system-level measurement results at the benchtop level. Finally, Section V draws some conclusions from this work.

II. System Architecture

Given that the majority of peripheral nerve signal power lies within 1-2 kHz with a peak around 1.5 kHz [3], Fig. 1 shows the proposed integrated system architecture for phrenic nerve recording and signal processing. The input signal is amplified with a low-noise neural recording amplifier with a gain of 40 dB and bandpass filtered up to 6 kHz. The amplified signal is then highpass filtered with a cutoff frequency of 300 Hz using a 2nd-order operational transconductance amplifier-capacitor (OTA-C) filter, additionally amplified by 20 dB with a resistive feedback amplifier, full-wave rectified using a current-mode rectifier, and then lowpass filtered with a cutoff frequency of 10 Hz. Off-chip RC highpass filters are also used in between stages for further dc removal. A third amplification stage with variable gain is used just before feeding the signal to a comparator with hysteresis to generate the trigger signal at the output.

III. Integrated Circuit Architecture

A. Neural Recording Amplifier

Since extracellular neural activity has amplitude levels on the order of a few tens of µVs, it is necessary to amplify the weak neural signal before any further signal processing can be performed. Neural recording amplifiers in general have to

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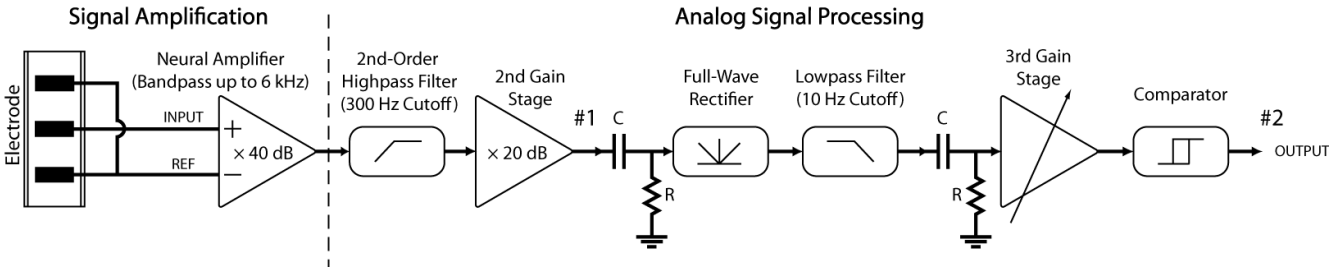

Fig. 1. Schematic block diagram of the neural recording and signal processing system.

be low-noise, and should provide adequate ac amplification and dc rejection. The front-end neural recording amplifier used in this work is a low-noise CMOS amplifier based on the design in [9]. This ac-coupled amplifier can reject dc frequency components at the interface, and amplify only the ac components in the mHz to kHz frequency range.

B. Highpass and Lowpass Filters

A 2nd-order Butterworth highpass filter has been implemented based on the design in [10], [11] with a standard transfer function as given by:

$$H(s) = \frac{s^2}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2} \tag{1}$$

where ω_p and Q_p are the pole frequency and quality factor of the highpass filter, respectively. The basic architecture for an OTA-C highpass filter is shown in Fig. 2 where G_{mi} (i = 1-4) is the transconductance of the i^{th} OTA. Filter design is guided by the following equations [11]:

$$C_1 = \frac{G_{m1}}{Q_p \times \omega_p} \tag{2}$$

$$C_2 = \frac{G_{m2} \times Q_p}{\omega_p} \tag{3}$$

$$G_{m3} = G_{m4}. \tag{4}$$

In this work, the highpass filter cutoff frequency is chosen to be around 300 Hz. Given that the quality factor of a 2nd-order Butterworth filter is 0.707 and that on-chip capacitors should be in the range of a few pF for a practical silicon implementation, OTA stages with very low transconductance values ($G_{m1,2}$) are needed.

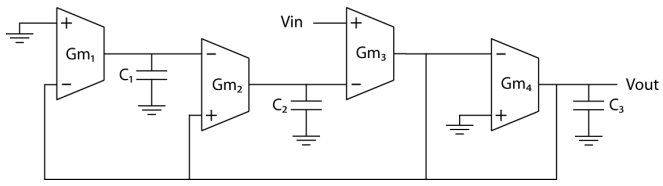

Fig. 2. Schematic block diagram of the 2nd-order OTA-C highpass filter.

Using the series-parallel current division technique, an OTA stage having very low transconductance with extended linear range is designed based on [12]. Compensation capacitor (C_3) has been used to ensure stability. An OTA-C lowpass filter with a target cutoff frequency of 10 Hz is also designed on-chip using the same technique.

C. Precision Full-Wave Rectifier

Fig. 3 shows the transistor-level circuit schematic of the precision full-wave rectifier that has been implemented in this work based on [13]. Full-wave rectification is performed in the current domain by the CMOS rectifier that comprises two transistors (M_n and M_p) and two wide-swing NMOS-PMOS current mirrors [14]. The rectifier is placed within the feedback loop of a high-gain operational amplifier [15], and its operation is best described based on the current flow, I_{in}, through MOS resistor string M_{11}-M_{12}.

During the positive cycle, M_n is turned on and M_p is turned off. Therefore, the drain current of M_n will be equal to I_{in}. This current is then mirrored by the wide-swing PMOS current mirror, and produces a positive output voltage V_{out} across MOS resistor string M_{13}-M_{14}. On the other hand, during the negative cycle, M_p is turned on and M_n is turned off. Therefore, the drain current of M_p will be equal to I_{in}. This current is then mirrored twice, first by the NMOS and next by the PMOS current mirror, to generate a positive output voltage across MOS resistors M_{13}-M_{14}.

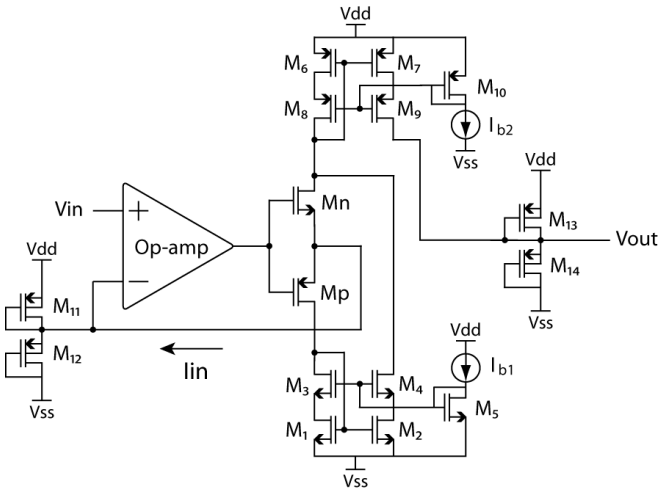

Fig. 3. Circuit schematic of the precision full-wave rectifier.

IV. Measurement Results

A prototype integrated circuit was fabricated using the AMI 1.5 µm double-poly double-metal n-well CMOS process. Fig. 4 shows a microphotograph of the fabricated chip (2.2 mm × 2.2 mm). A custom-designed printed-circuit board (PCB), as shown in Fig. 5, was used to house the microchip and evaluate the circuit- and system-level performance at the benchtop level.

The front-end neural recording amplifier had a measured mid-band ac gain of 39.39 dB and a 3-dB bandwidth of approximately 3 mHz to 6 kHz. The input-referred noise voltage over the frequency range of 290 Hz to 6 kHz was measured to be 1.95 μV_{rms}.

The 2nd-order Butterworth highpass filter was implemented with nominal design parameters of $G_{m1,2}$ = 10 nS, $G_{m3,4}$ = 14 µS, C_1 = 7 pF, C_2 = 3.5 pF, Q_p = 0.707, for a nominal cutoff frequency of 300 Hz. Fig. 6 shows the simulated (dashed line) and measured (solid line) frequency response of the Butterworth highpass filter with a cutoff frequency of 320 Hz and 290 Hz, respectively. Moreover, the simulated and measured in-band gain was -0.89 dB and -0.68 dB, respectively. The slight discrepancy (<10%) in cutoff frequency was attributed to post-fabrication variations in the value of capacitive components, $C_{1,2}$.

The full-wave rectifier gain was measured to be 1.28 and -1.36 for positive and negative cycles, respectively. Gain deviations from the nominal value of unity were mainly caused by device mismatches in implementing MOS resistors and current mirrors as well as the finite output impedance of the current mirrors. During the negative cycle, rectifier gain is more adversely impacted than in the positive cycle, because the output current is mirrored twice, first by the NMOS and then by the PMOS current mirror [13].

For on-chip implementation of the lowpass filter, nominal capacitor and transconductance values of 20 pF and 1.25 nS were selected for a cutoff frequency of 10 Hz. The measured cutoff frequency was found to be approximately 8.75 Hz due to post-fabrication variations in the capacitor value.

Table I summarizes the measured performance characteristics of major circuitry in the system. The total system power consumption was 1 mW from ±1.5V.

TABLE I
Summary of Measured Chip Performance

Circuit Block	*Parameter*	*Measured Value*
Front-End Amplifier	Gain @ 1 kHz	39.39 dB
	Bandwidth	3 mHz – 6 kHz
	Input-Referred Noise (290 Hz – 6 kHz)	1.95 μV_{rms}
2nd-Order Highpass Filter	Cutoff Frequency	290 Hz
Full-Wave Rectifier	Positive Cycle Gain: 1.28 (2.1 dB) Negative Cycle Gain: -1.36 (2.7 dB)	
Lowpass Filter	Cutoff Frequency	8.75 Hz
Comparator	Hysteresis Loop	200 mV

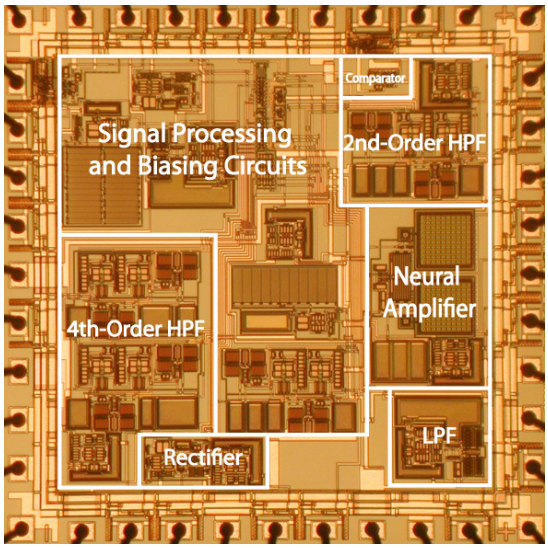

Fig. 4. Microphotograph of the 2.2 × 2.2-mm^2 IC fabricated using AMI 1.5 µm 2P/2M n-well CMOS process.

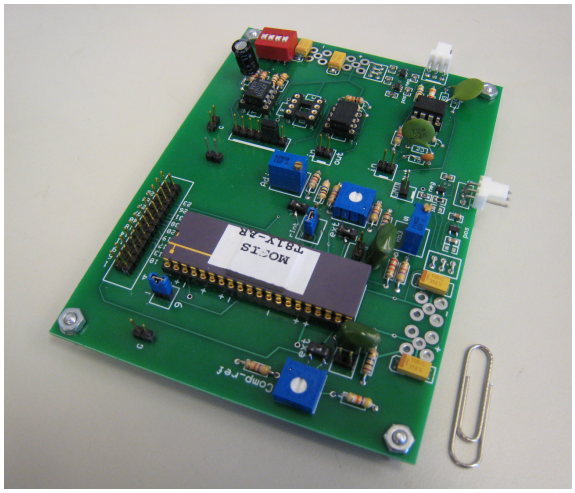

Fig. 5. A photograph of the custom-designed PCB housing the microchip.

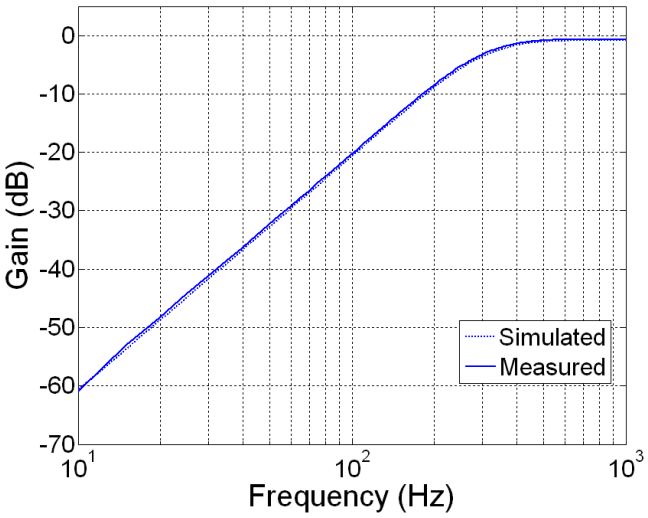

Fig. 6. Simulated (dashed line) and measured (solid line) frequency response of the 2nd-order Butterworth highpass filter.

To verify the system-level functionality of the integrated electronics, a benchtop experiment was performed using a 1-kHz, 60-μV_{pp}, amplitude-modulated, sinusoidal signal as the system input. The amplitude modulation profile was the temporal profile of a surface EMG signal as described in [16]. Fig. 7 shows the measured system-level waveforms. The top trace depicts the amplitude-modulated signal with maximum amplitude of 60 mV_{pp} before being attenuated by 60 dB and fed to the system input. The middle trace shows the measured waveform corresponding to node 1 in Fig. 1 after two stages of amplification and highpass filtering. The bottom trace depicts the measured trigger signal at the output of the system, corresponding to node 2 in Fig. 1.

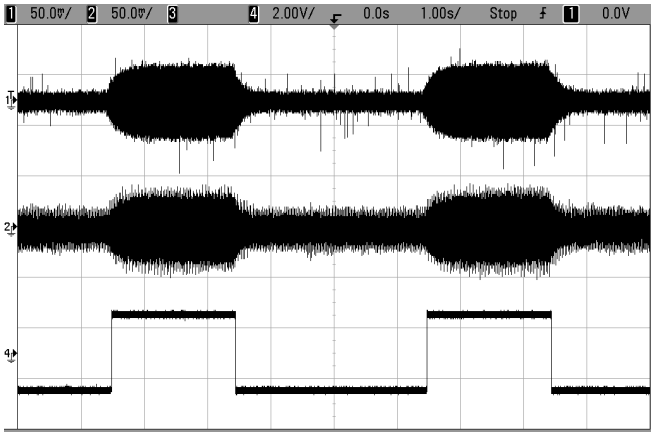

Fig. 7. Measured system-level waveforms. The top trace is a 1-kHz, amplitude-modulated, sinusoidal signal with maximum amplitude of 60 mV_{pp}. The amplitude modulation profile is the temporal profile of a surface EMG signal as described in [16]. This signal is then attenuated by 60 dB before being fed into the system, corresponding to an input signal for the system with maximum amplitude of 60 μV_{pp}. The middle trace depicts the waveform after two amplification stages and highpass filtering, corresponding to node #1 in Fig. 1. The bottom trace depicts the trigger signal at the system output that corresponds to node #2 in Fig. 1.

V. Conclusion

We presented an integrated implementation of interface electronics for phrenic nerve recording and signal processing in order to generate a trigger signal from bursts of neural activity. The system is envisioned to be used as part of a "smart" laryngeal pacemaker device to reanimate a paralyzed muscle by electrical stimulation paced with respiration. Overall system architecture as well as that of major building blocks, such as filtering and rectification stages, were presented along with simulation and measured results from a fabricated prototype. The system consumes 1 mW from a 3-V power supply. Efforts are currently underway to miniaturize the PCB and interface the system with a flat interface nerve electrode (FINE) [17] for future *in vivo* experiments in the canine.

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