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A Low-Power Area-Efficient 8 bit SAR ADC Using Dual Capacitor Arrays for Neural Microsystems

Sun-Il Chang and Euisik Yoon

Abstract— **We report an area-efficient 8bit SAR ADC using dual capacitor array banks for brain signal interface microsystems. The proposed ADC consumes 680nW and the total chip area is 0.035 mm^2. We reduced the area and power by a factor of eight when compared with conventional approaches. If we increase the resolution, the area and power reduction factor exponentially increases in our architecture (e.g., a factor of 16 for 10 bit resolution). The measured SNDR, SFDR, THD, and ENOB are 42.82 ± 0.47 dB, 57.90 ± 2.82dB, -53.58 ± 2.15 dB, and 6.65 ± 0.07 bits, respectively.**

I. Introduction

Recently, multichannel neural interface systems have been implemented to monitor neural activities [1-2]. For the comprehensive analysis of neural activities, it is essential to realize simultaneous real-time monitoring of multiple sites in 3D electrode arrays with 64 channels or more. Typically, neural activities such as spike contain most of information in the bandwidth below 10 kHz with maximum amplitude of ±500 μV [3]. In these microsystems, the neural signals should be amplified and converted into digital signals to be transmitted to wired/wireless communication channels between the implanted system and the external world. Simultaneous access of multiple sites requires better noise immunity in analog-to-digital converters (ADC) in a small form factor at low power.

A successive approximation register (SAR) ADC is one of the suitable candidates for neural interface applications due to its simplicity, low power consumption, and reasonable resolution. With a gain of 60 dB prior to the ADC, the quantization noise is required to be less than 5 mV_{rms} which can be achieved by 8 bit or higher resolution capability of ADC. Fig. 1 shows a conventional 8 bit SAR ADC structure which typically consists of three parts: capacitor array (for sample and hold and DAC), comparator, and successive approximation register (SAR). For relatively lower resolution ADCs (<6b), the comparator and SAR consume most power [4]. However, as the resolution of ADCs increases, the power consumption required for charging and discharging the capacitor array becomes significant. Also, the total capacitance required for DAC increases exponentially

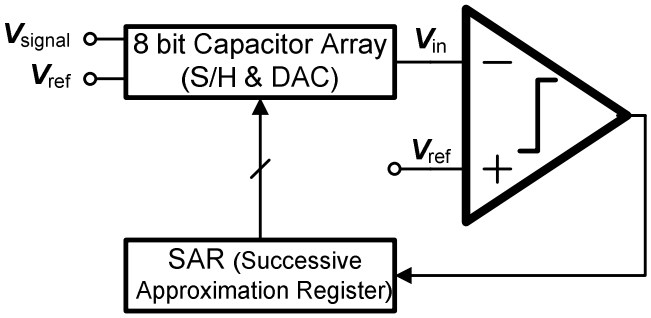

Fig. 1: The overall structure of conventional SAR ADC

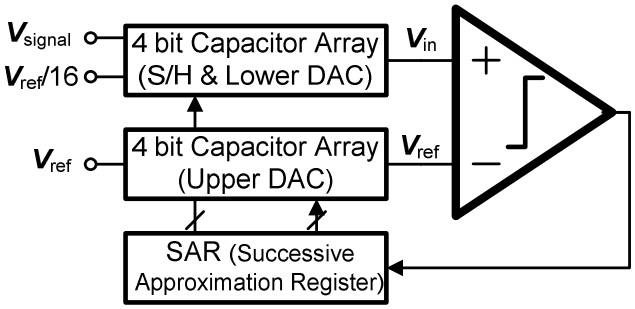

Fig. 2: The overall structure of the proposed area-efficient SAR ADC

proportional to the number of bits. In the high resolution ADCs, the capacitor array takes most of the area and power consumption. It becomes more important to reduce the total capacitance and area as the number of bits required in ADC increases and multiple implementations of ADCs is needed. Chang, *et al*. reported an effective switching method to reduce the power [5]. However, this switching technique can reduce only half of the power in conventional capacitor arrays. Yang, *et al*. proposed an energy-efficient ADC with a small form factor [6]. However, relatively complex algorithm has to be implemented for practical use in neural microsystems.

In this paper, we propose an area-efficient 8 bit SAR ADC using dual capacitor arrays. Using the dual capacitor array banks, we can reduce the required capacitor array area by a factor of $2^{N/2-1}$ compared to the conventional approaches. This feature can not only reduce the area but also the power consumption by eliminating the power required for charging/discharging the capacitor array.

II. Area Efficient SAR ADC Architecture

A. Dual Capacitor Arrays

The key idea of the proposed SAR ADC is to perform the successive approximation in both sides of comparator inputs using dual capacitor arrays rather than only in one side. As

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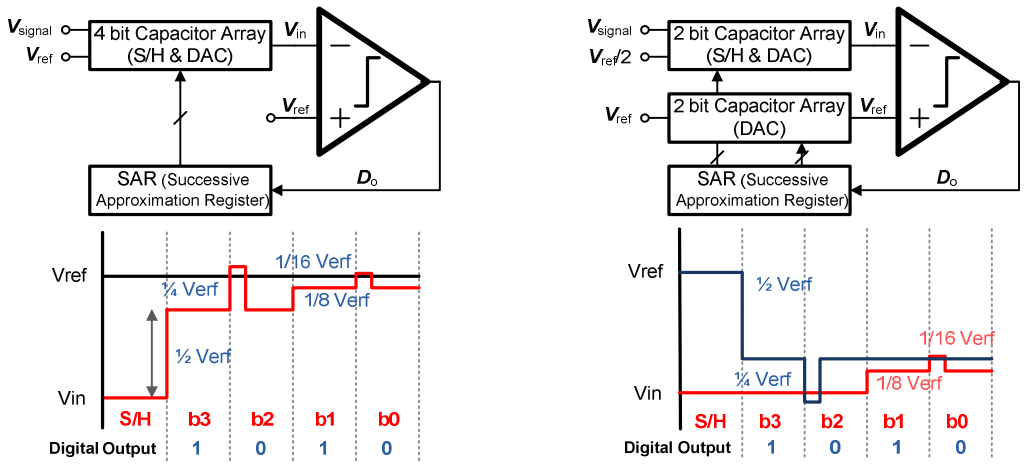


(a) Conventional SAR ADC (b) Area Efficient SAR ADC

Fig. 3: 4 bit SAR ADC operation examples: (a) Conventional SAR ADC, (b) Proposed area-efficient SAR ADC

shown in Fig. 2, the 8bit DAC can be split into two identical 4 bit capacitor arrays. The upper DAC is used to quantize upper 4 bits, while the lower DAC does lower 4 bits. The main advantage of the dual capacitor arrays is the reduction of the total capacitance and area for DAC capacitors by a factor of

$$\text{Redcution Factor} = 2^{\frac{N}{2}-1},$$

where N is the number of bit. For example, for 8 and 10 bit resolutions, the reduction factors become 8 and 16, respectively. And the power consumed by the capacitor array would be reduced by the same reduction factor. This advantage is more effective for higher resolution ADCs. By applying this technique, we can effectively implement the ADCs within the given area and power budget. This feature easily equips the neural interface system with a simultaneous real-time monitor capability of the multiple neural activities. The dual capacitor array operation will be explained in detail in the following sections.

B. SAR ADC Operation

Fig. 3 shows the example of 4 bit ADC operations in conventional SAR ADC and the proposed ADC. Basic operations of the 4 bit SAR ADC can be divided into two steps: sample/hold and 4-times of successive approximations. During each approximation step, V_{in} can be expressed as:

$$V_{in}[n] = V_{in}[n-1] + \frac{Vref}{2^{n+1}}(1-(-1)^{D_o[n]})$$

If the $V_{in}[n]$ is smaller than V_{ref}, the comparator output is 1, and the SAR sets the output $b_n = 1$ and generates the control signal to make $V_{in}[n]$ be $V_{in}[n-1] + V_{ref} / 2^n$. If the V_{in} is greater than V_{ref}, the output is $b_n = 0$, and the V_{in} stays from previous step. The red line shows V_{in} from each steps. By repeating this step four times, the signal can be quantized into a 4 bit resolution.

As shown Fig. 3 (a), the conventional ADC is performing the approximation in the one input node of the comparator while the other input side is fixed to reference. On the other hand, the proposed ADC uses both sides (signal side: 2 bit and reference side: 2 bit) to perform the approximation. During the first two steps, the upper DAC is operated to approximate V_{ref} to V_{in} as shown by blue line in Fig. 3 (b). Successively, during the following two steps, V_{in} is approximated to V_{ref} using the lower DAC. After 4 steps, the signal is digitized as 1010. For the same resolution, the proposed ADC requires only half (= 1/reduction factor = $1/2^{N/2-1}$) the area in the capacitor array and consumes half the power as compared to the conventional ADC. Here, it should be noted that we need more additional reference, $V_{ref} / 2^{N/2}$, in the proposed scheme, which can be provided externally.

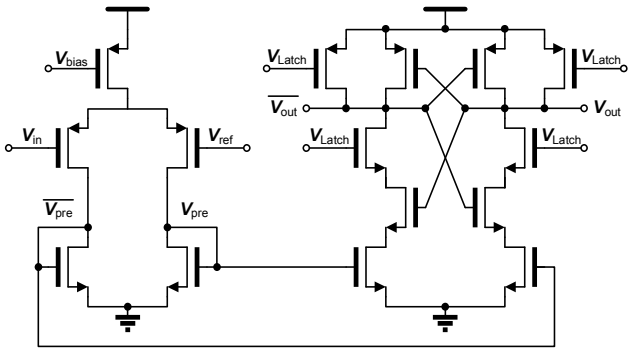


Fig. 4: Schematics of the comparator

III. SAR ADC Circuit Blocks

A. Comparator

Fig. 4 shows the schematic diagram of the comparator. Due to smaller capacitance in the dual capacitor arrays, the regenerative comparator may cause kickback effect during the regenerative phase. This coupling effect between input and output may severely deteriorate the performance of ADC. To suppress this phenomenon, a buffer stage with gain of 10 is introduced prior to the regenerative comparator. The difference between two inputs (V_{in} and V_{ref}) is sampled and amplified through the buffer stage and then forwarded to the regenerative stage during reset phase. In the positive rising edge of V_{Latch} when regenerative phase starts, the difference is

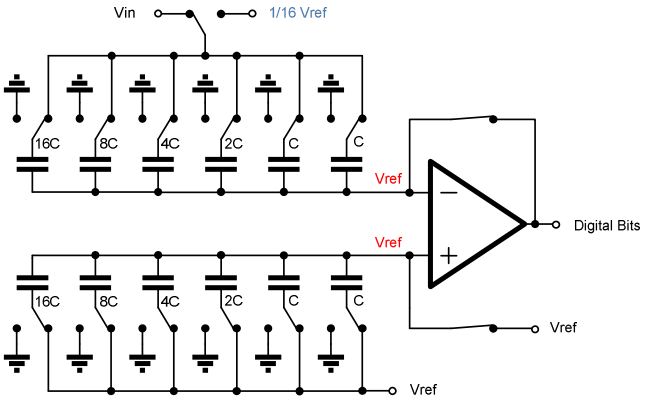


Fig. 5: Dual capacitor array (during reset phase)

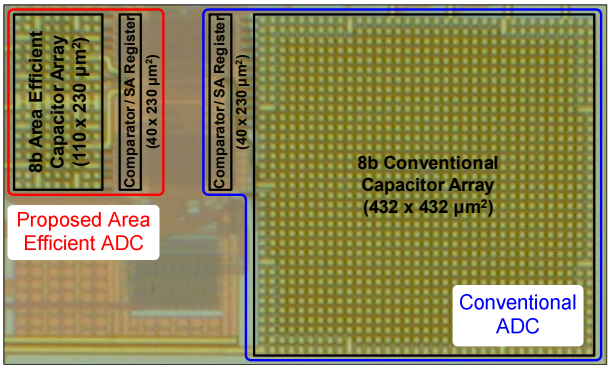


Fig. 6: Microphotograph of the fabricated preamplifier in a test chip

amplified and eventually the polarity of the difference is determined. In the proposed ADC, two identical capacitor arrays are located on both input nodes of the comparator. This configuration helps to suppress the comparator offset which may come from the charge injection from the reset switches or any unexpected possible leakage path.

B. Dual Capacitor Arrays

As shown in Fig. 5, to implement both upper and lower DACs, two identical capacitor arrays have been implemented using MIM capacitors, where a unit capacitance is given as 100fF. Total capacitance for the area-efficient 8 bit ADC is 2 x $2^4C_{unit} = 32C_{unit}$. The two 4 bit capacitor arrays are identical except that the lower DAC has an additional switch to sample and hold the signal during the comparison.

IV. Measurement Results

Fig. 6 shows the fabricated ADC using 0.25µm 1P5M CMOS process. To evaluate the proposed ADC, the conventional ADC is also fabricated, measured, and characterized. The total active area of the proposed ADC is 0.035 mm^2, while the conventional ADC occupies 0.196 mm^2. Performance of the ADC is summarized in Table 1. The fabricated ADCs have the resolution of 8 bit with the sampling frequency of 20kS/s. The total power consumption of the proposed ADC is 680nW at 1.8V (Analog) and 2.5 V (digital) supply. The comparator consumes most of power (~498 nW), and the proposed capacitor array consumes 92nW from 1.2V input range, while the conventional capacitor array consumes ~737 nW, which is eight times higher and even

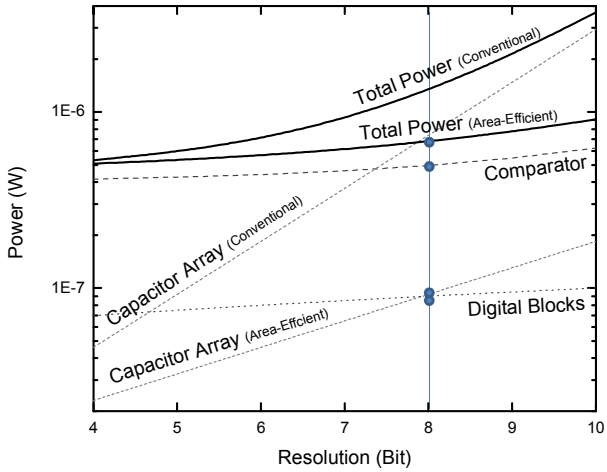
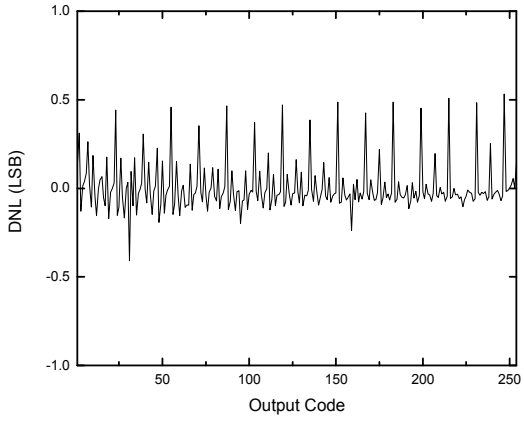
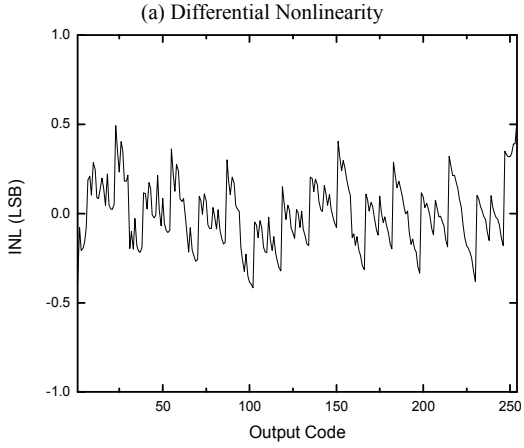


Fig. 7: Power consumption comparison with respect to the resolution



(a) Differential Nonlinearity



(b) Integral Nonlinearity

Fig. 8: The measured (a) DNL and (b) INL of the proposed ADC

higher than the comparator.

We also estimate the power consumption as a function of resolutions in ADC as shown in Fig. 7. The total power consumption increases with resolution. Especially, the power consumption by the conventional capacitor array becomes significant when the resolution is above 7 bit, and increases even exponentially with resolution (2^N). On the other hand, the power consumption of the proposed capacitor array slowly increases by a factor of $2^{N/2}$, and consumes much less power. Even in 10 bit resolution, the power consumption of the proposed capacitor array stays below that of the

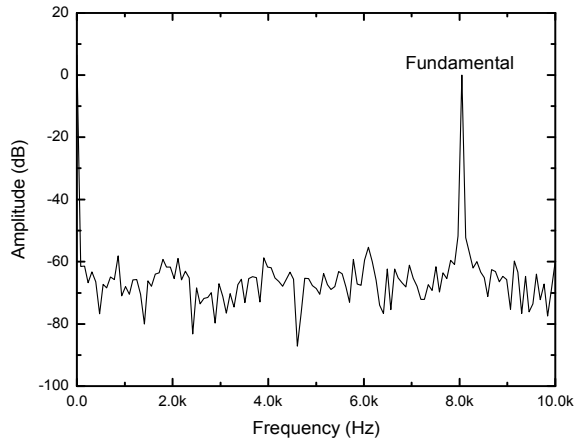


Fig. 9: FFT plot of the measured digital output codes for an input frequency of 8046.875 Hz

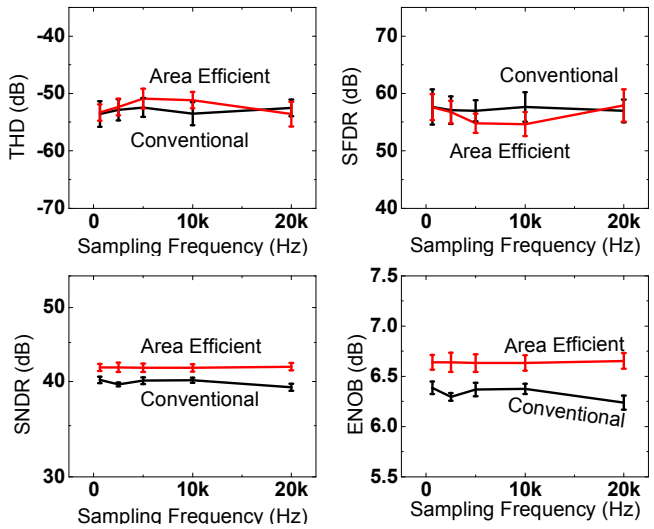


Fig. 10: Measured dynamic characteristics with different sampling frequency: Area efficient and Conventional ADCs

comparator.

A. *Static Characteristics*

Fig. 8 shows the measurement results of differential nonlinearity (DNL) and integral nonlinearity (INL). The measured INL and DNL are both below ±0.5 LSB.

B. *Dynamic Characteristics*

The measured 8 bits digital output codes are analyzed using the FFT from the input signal of 8046.875 Hz and 256 samples shown in Fig. 9. The measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 42.82 ± 0.47 dB and 57.90 ± 2.82 dB, respectively. Total harmonic distortion (THD) and effective number of bit (ENOB) are -53.58 ± 2.15 dB and 6.65 ± 0.07 bits, respectively.

We also measured the dynamic characteristics of ADC with different sampling frequencies to test leakage. Especially, leakage can be significant in small capacitor arrays at low sampling frequency (<1kS/s) such as EEG or ECoG applications. The results are shown in Fig. 10. The performance of the proposed ADC remains constantly with the range of the various sampling frequencies (625 Hz ~ 20 kHz) indicating leakage is not a serious issue even though we use the small capacitance array bank.

Parameter	Measured
Technology	0.25µm 1P5M CMOS
Supply Voltage	1.8V (Analog) / 2.5 V (Digital)
Sampling Frequency	20 kS/s
Power Consumption	680 nW
INL	< ± 0.5 LSB
DNL	< ± 0.5 LSB
SNDR	42.82 ± 0.47 dB
SFDR	57.90 ± 2.82 dB
THD	-53.58 ± 2.15 dB
Resolution / ENOB	8 bits / 6.65 ± 0.07 bits
Figure of Merit	0.34 pJ/conversion
Area	0.035 mm²

Table 1: Performance Summary Table

V. Conclusion

We have proposed, designed, fabricated and fully characterized an area-efficient SAR ADC using dual capacitor arrays for neural microsystems. The proposed ADC consumes 680nW and the total chip area is 0.035 mm^2. The measured SNDR, SFDR, THD, and ENOB are 42.82 ± 0.47 dB, 57.90 ± 2.82dB, -53.58 ± 2.15 dB, and 6.65 ± 0.07 bits, respectively. Compared to the conventional ADC, the proposed ADC consumes less power by a factor of $2^{N/2-1}$ (8 in this paper) and occupies less area. This reduction factor increases exponentially with the increase of resolution. This implies that the proposed scheme will benefit more at higher resolution ADCs in EEG or ECoG applications. With the proposed ADC, we can effectively implement the neural interface system with multiple ADCs within a given area and power budget.

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