31st Annual International Conference of the IEEE EMBS
Minneapolis, Minnesota, USA, September 2-6, 2009

A Low-Noise Low-Power Amplifier for Implantable Device for Neural Signal Acquisition

Ming-Ze Li and Kea-Tiong Tang, *Member, IEEE*
mzli@larc.ee.nthu.edu.tw, kttang@ee.nthu.edu.tw
Lab for Reliable Computing, NBME Group, Department of Electrical Engineering,
National Tsing Hua University, 101, Section 2, Kuang-Fu Road, Hsinchu, Taiwan 30013, R.O.C.

***Abstract*—This paper presents a low-noise low-power amplifier for implantable device for neural signal acquisition. By operating MOS transistors in the subthreshold region, smaller low-frequency noise and lower power consumption can be achieved. A low power, low-noise common-drain buffer and a low-noise, high-linearity, low pass filter are used for high frequency noise filtering. Post-layout simulation shows the input referred noise of the system is 2.19μVrms from 10Hz to 10 KHz, power consumption is 55.8μW, and the NEF is 2.53. The amplifier was fabricated using a TSMC 0.18μm 1P6M CMOS process. Simulation results show that this low-noise, low-power amplifier is suitable for implantable device applications.**

I. Introduction

Much research is being done on implantable devices, such as cochlear implants, retinal prostheses, motor prostheses, etc. Acquiring information regarding the stimulated neurons and recording the neural activities in these neural prosthetic devices is essential. It is also crucial to monitor and process the neural action potential signals in real time for closed-loop controlled deep brain stimulation (for example, in epilepsy and Parkinson's disease).

The front end of the implantable device is an array of stimulating/recording electrodes. These electrodes read extracellular neural signals (ENG), which are very small (5μV-500μV) and have a low frequency (10Hz-10 kHz). The distance between an electrode and the cell body determines the signal amplitude. In lab experiments researchers can keep this distance very small to obtain a larger neural signal. However, in the real implant, this distance is very difficult to control, and the resulting ENG can be very small requiring a low-noise amplifier (LNA) for signal amplification to acquire the neural signal.

A MOSFET has inherent 1/f noise that dominates at low frequencies. Unfortunately, ENG is in the same frequency band as 1/f noise, resulting in a very poor SNR. A common solution is chopper stabilization (CHS) [1…4]. The idea is to modulate the signal to a higher frequency than the flicker noise of the amplifier at the next stage. The advantage is a higher SNR while the disadvantage is the need of an amplifier operating at relatively higher frequencies with higher power consumption. For example, power dissipation is 1.3mW in [1], 500μW in [2] and 242μW in [3]. Higher power consumption is not desirable, especially for an implantable device.

Another possible solution is auto-zeroing (AZ) [5…7]. Auto-zeroing reduces noises lying in two different phases by doing sample and hold. Auto-zeroing techniques work quite well for very low frequency noise elimination (such as DC offset), but not in ENG applications (up to 10 kHz).

This work utilizes the fact that MOSFET flicker noise is smaller when operating in the subthreshold region. Therefore, the low-noise, lower power amplifier is composed of subthreshold MOSFETs (Sub-MOS). Section II describes the circuit principle. Section III presents post-layout simulation results. Sections IV and V have the discussion and conclusion, respectively.

II. Circuit Principle

The source of MOSFET flicker noise is the "traps" at the interface between the gate oxide and the silicon. When the transistor operates in the above-threshold region, the carrier transport mechanism is by drift current, which flows through the channel right underneath the silicon-oxide interface. When the carrier flows through the trap, the trapping and detrapping processes of the carrier cause current interference. Higher trap density results in more interference.

Alternatively, when the transistor operates in the subthreshold region, the carrier transport mechanism is by diffusion current, which happens away from the silicon-oxide interface. Since the carrier is further away from the traps, it has lower possibility for the carriers to be trapped and detrapped, thus the current interference is smaller in the subthreshold region.

Figure 1 shows the system architecture. The system has a pre-amplifier, a high pass function by means of feedback capacitors and resistors, a buffer, and a low pass filter.

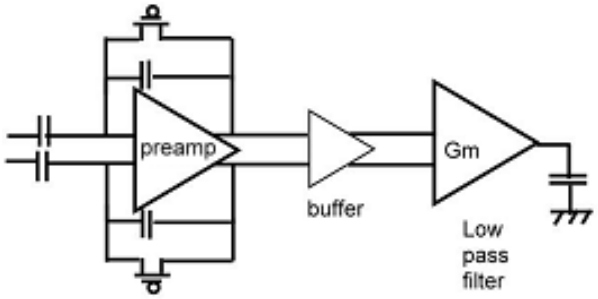

Fig. 1. System architecture of the low-power, low-noise amplifier

Function and operation of each circuit block is as follows:

A. Pre-Amplifier

Figure 2 shows the circuit diagram of the preamp. The three left-most transistors provide the biases. The other transistors are the body of the amplifier. The amplifier is designed to be fully differential to reduce the coherent noise from the sensitive input stage.

A noise analysis of the amplifier reveals the effective noise voltage power spectrum density:

$$e_{in}^{\ 2} = \frac{\left[gm_6^{\ 2} * \left(\frac{gm_1^{\ 2} * e_1^{\ 2} + gm_3^{\ 2} * e_3^{\ 2}}{gm_3^{\ 2}} + e_6^{\ 2} \right) + \frac{e_{10}^{\ 2}}{r_{o12}^{\ 2}} + gm_{12}^{\ 2} * e_{12}^{\ 2} \right] R_{out}^{\ 2}}{gm_1^{\ 2} * \frac{1}{gm_3^{\ 2}} * gm_6^{\ 2} * R_{out}^{\ 2}} \quad (1)$$

$$= e_1^{\ 2} + \frac{gm_3^{\ 2}}{gm_1^{\ 2} * gm_6^{\ 2}} * (...),$$

Where e is the power spectrum density of voltage noise, r_o is the output resistance of the transistor and R_{out} represents the effective output resistance looking into V_{o+}. According to the above equation, what influences the effective noise the most is M_1, which is the input transistor. Thus this design is based on $g_{m1} >> g_{m6} > g_{m3}$ to sufficiently reduce the effective noise from the later stage to the inputs.

Since M_1 most affects the noise performance, this work designs M_1 to operate in the subthreshold to reduce its noise. Additionally, increasing the area of M_1 is an effective way to reduce low-frequency noise. The number of traps in a unit area at the gate oxide/silicon interface is related to the fabrication process. Increasing the transistor area will not change the density of the traps, but will affect the number of carriers flowing through a unit area. Thus, the number of carriers flowing through a unit area decreases, resulting in a decreased possibility of carriers being trapped and detrapped.

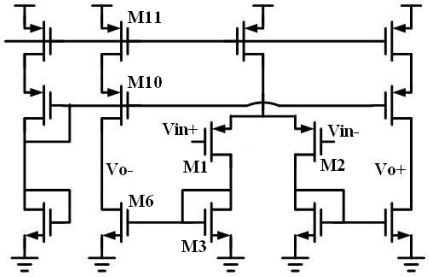

Fig. 2. Circuit diagram of the pre-amplifier

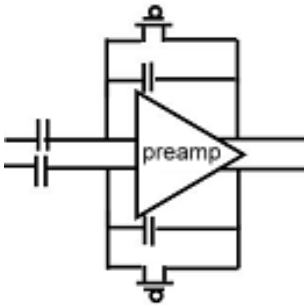

Fig. 3. Connecting feedback capacitors and resistors with LNA for high pass function.

B. High Pass Function

When reading the neural signals in an implantable device, the DC voltage of the body fluid where electrodes reside is usually different than the LNA input common-mode voltage. Additionally, the DC voltage value of body fluid is unknown depending on the status of the body. When this DC voltage connects to the input of the LNA through the electrode, it can easily saturate the output of the LNA. To solve this problem, feedback capacitors and resistors are connected to the LNA to form a high pass function to filter the DC voltage from the body fluid, as shown in Figure 3. Since the resistor itself is a noise source, the design uses subthreshold MOSFETs to replace the resistors.

C. Buffer

The buffer makes the low pass filter at the next stage operate within the appropriate working voltage range. The buffer structure is a common-drain single stage amplifier. The design is to be low power dissipation and low noise. Figure 4 shows subthreshold PMOS transistors used for the buffer .

D. Low Pass Filter

The low pass filter removes the high-frequency noise carried in the unwanted band (>10kHz). The circuit is adapted from [8]. In this work, in addition to modifying the circuit to be single-ended, the four input transistors operate in the subthreshold region. Figure 5 shows the circuit. The nucleus is a g_m-C filter using a differential pair in series with a capacitor. The two transistors in the subthreshold linear region can be viewed as large resistors in a small-signal analysis. Therefore, these transistors cause source degeneration and increase the linearity of g_m. This g_m-C filter provides not only a filtering function, but also signal gain and at the same time converts the differential signal into a

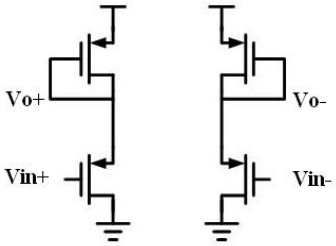

Fig. 4. A low power, low-noise, common drain voltage buffer operating in the subthreshold region.

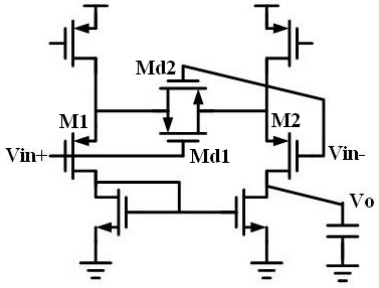

Fig. 5. The low-noise, high linearity, low-pass filter

single-ended output.

III. Post-Layout Simulation Results

The index of a low-power LNA is the noise efficiency factor (NEF), which is a combined estimation of power, noise, and bandwidth. NEF represents the noise performance and bandwidth under a power constraint. Thus, NEF represents the efficiency from a given power. A lower NEF means the efficiency of the LNA is better. The definition of NEF can be found in [9]. Table I shows the post-layout simulation results of the pre-amplifier including the NEF.

Figure 6 shows the simulation results of the buffer. The buffer works as a voltage shifter such that the low-pass filter would operate within an adequate DC voltage range. Since the designed input common mode voltage of the LPF is 0.1V, while the output common mode voltage of the preamp is -0.5V, the DC transfer curve of the buffer should convert the DC output of the LNA to 0.1V before sending it to the input of the LPF. Simulation results show very good linearity for the voltage conversion. The gain of the buffer is about 0.7dB. Figure 7 depicts the frequency response of the LPF. The 3dB frequency is about 11.9 kHz. Figure 8 shows the layout of the

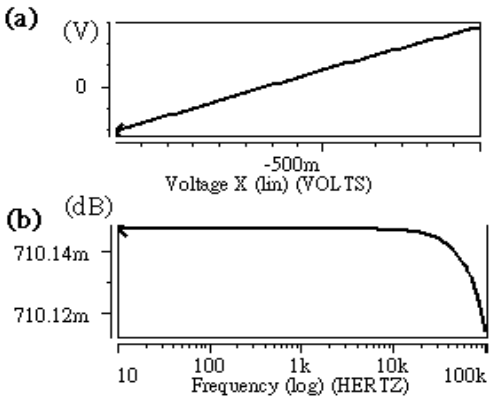

Fig.6. (a) Voltage transfer curve of the buffer
(b) The DC gain of buffer is about 0.7dB

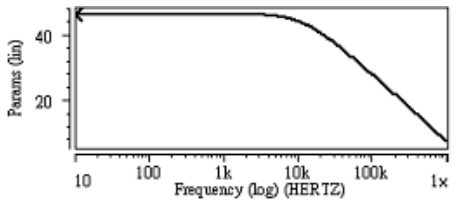

Fig.7. The 3dB frequency of this low pass filter is about 11.9 kHz.

TABLE I
Post Simulation of Preamp

Input Referred Noise Voltage (μVrms @10Hz-10kHz)	2.3
Power (μW)	46.7
Gain (dB)	30.4
3dB Frequency (kHz)	25.1
Phase Margin	115.6
Unity Gain Frequency (MHz)	5.1
NEF	1.63

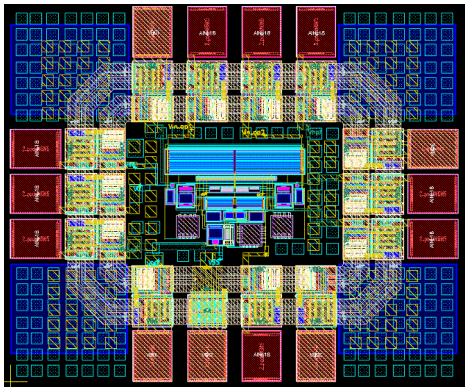

Fig.8. Chip layout of the overall amplifier.

TABLE II
Benchmark

reference	year	Tech (μ m)	gain(dB)	bandwidth (Hz)	power(μ W)	Vin,rms(μ V)	NEF
this work	2009	0.18	89.9	10-10.9k	55.8	2.19	2.53
[10]	2006	0.8	80	1-5k	2400	0.291	4.3
[11]	2006	0.35	77	100-7k	1.4786	6.852	N/A
[12]	2006	1.5	40-90	0.5-5k	N/A	4.4	N/A
[13]	2007	0.5	36.1	0.3-4.7k	N/A	3.6	1.8
[14]	2007	0.5	40.9	392m-295	2.08	1.66	3.21
[15]	2007	0.8	40	0.05-100	N/A	0.95	4.6
[16]	2008	0.5	40-60	0.01-10k	50	4.8	N/A
[17]	2008	0.35	45.5	0.052-200	1.1	2.1	2.9
[18]	2009	0.35	45.6-60	4.5m-292	N/A	2.5	3.26
[19]	2009	0.5	39.6	94-8.2k	N/A	1.94	2.9

chip and Table II shows the post-layout simulation results of the overall low-noise, low-power amplifier.

IV. Discussion

A theoretical value of the NEF (2.02) is derived with the assumption that κ=0.7 ([11]). But we must remember that κ is affected by the process, bias, and many other environmental factors. Therefore, the NEF in Table I is still a possible value as long as κ approaches 0.88.

Table II compares this work and other related works. In contrast with other related works (0.8μm to 0.35μm processes), this work uses a more advanced 0.18μm process. One of the reasons for this advanced process not being so popular for a low-noise amplifier is because of its noise characteristics. Although a more modern process has advantages, such as higher speed, lower power consumption, smaller area, etc, advanced process also inherits a larger noise floor. The following equation clearly reveals this:

$$Sid = \frac{KF * ID^{AF}}{f^{EF} * Cox * WL} \quad (2)$$

where *Sid* represents the power spectrum density of the flicker current noise. *KF* and *AF* are process dependent noise constants. For example, *KF* for the 0.18μm process is nearly 3 times that of the 0.35μm process. If all things else being equal, the noise level for the 0.18μm process is 3 times than that of the 0.35μm process not to mention that the relationship of *AF* to noise is actually exponential and the noise level will be much higher than 3 times!

Even with the drawback of the higher noise level for the advanced process, the advanced process is still of interest because the low-noise amplifier is just one block of the whole system. Going for a more advanced process is still attractive for optimizing overall system performance. Therefore, this work chooses the 0.18μm process with its naturally higher noise level and then carefully analyzes and reduces this noise level. This work achieves a NEF of 2.53, which is comparable to, if not better than, other works with the larger process.

V. Conclusion

This study proposes a low-noise, low-power amplifier for biomedical implantable devices. Low noise and low power consumption are achieved by operating the transistors in the subthreshold region. Post-layout simulation shows the input referred noise of the system is 2.19μVrms from 10Hz to 10 kHz, power consumption is 55.8μW, and the NEF is 2.53. The amplifier was fabricated using a TSMC 0.18μm 1P6M CMOS process.

Acknowledgment

The authors would like to acknowledge the support of the National Science Council of Taiwan, under Contract No. NSC 97-2220-E-007-036. We also acknowledge the support of the Chung-Shan Institute of Science and Technology, under Contract No. CSIST-808-V110. We also thank the National Chip Implementation Center for chip fabrication.

References

[1] A. Uranga, X. Navarro, and N. Barniol, "Integrated CMOS Amplifier for ENG Signal Recording," IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING, VOL. 51, NO. 12, DECEMBER 2004.

[2] T Yoshida, Y Masui, T Mashimo, M Sasaki, and A Iwata, "A 1 V Low-Noise CMOS Amplifier Using Autozeroing and Chopper Stabilization Technique," IEICE Transactions on Electronics, Pp. 769-774, 2006.

[3] JH Nielsen, and E Bruun, "A CMOS low-noise instrumentation amplifier using chopper modulation," Analog Integrated Circuits and Signal Processing, pp. 65-76, 2005.

[4] Christian Menolfi, and Qiuting Huang, "A Low-Noise CMOS Instrumentation Amplifier for Thermoelectric Infrared Detectors". IEEE J. SOLID-STATE CIRCUITS, VOL. 32, NO. 7, JULY 1997.

[5] Chih-Wen Lu , "An Offset Cancellation Technique for Two-Stage CMOS Operational Amplifiers," Integrated Circuit Design and Technology, On page(s): 1-3, May 30 2007.

[6] Danchiv, A., and Bodea, M. ," Residual offset optimization for a continuous time auto-zero amplifier," ICSES, page(s): 281-284, 2008.

[7] Christian C.ENZ & Gabor C. Teams, "Circuit techniques for reducing the effects of op-amp imperfections: auto-zeroing, correlated double sampling, and chopper stabilization," Proceedings of the IEEE, VOL 84, NO 11,pp1584-1614, NOVEMBER I996.

[8] F Krummenacher, and N Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," IEEE J. SOLID-STATE CIRCUITS, VOI 23, NO 3, JUNE 1988.

[9] M. Steyaert, W. Sansen, and C. Zhongyuan, "A micropower low noise monolithic instrumentation amplifier for medical purposes," IEEE J. Solid-State Circuits, vol. 22, pp. 1163–1168, Dec. 1987.

[10] R Rieger, M Schuettler, D Pal, C Clarke, P Langlois, J Taylor, and N Donaldson, "Very low-noise ENG amplifier system using CMOS technology", IEEE TRANSACTIONS ON NEURAL SYSTEMS AND REHABILITATION ENGINEERING, VOL. 14, NO. 4, DECEMBER 2006.

[11] Woradorn Wattanapanitch, Michale Fee, and Rahul Sarpeshkar, "An Energy-Efficient Micropower Neural Recording Amplifier".IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, VOL. 1, NO. 2, JUNE 2007.

[12] Chua-Chin Wang, Chi-Chun Huang, Jian-Sing Liou, and Kuan-Wen Fang, "A 140-dB CMRR Low-noise Instrumentation Amplifier for Neural Signal Sensing", IEEE Asia Pacific Conference on Circuits and Systems, pp, 696-699, 2006.

[13] S Farshchi, and J W. Judy, " Low-Noise Amplifier Circuit for Embedded Electrophysiological Recording with Adjustable Gain and High-Pass Filtering," University/Government/Industry Microelectronics Symposium, page(s): 105-108, June 2006.

[14] Jeremy Holleman and Brian Otis, "A Sub-Microwatt Low-Noise Amplifier for Neural Recording," Engineering in Medicine and Biology Society, 2007.

[15] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 W 100 nV/RTHZ chopper-stabilized instrumentation amplifier for chronic measurement of neural eld potentials," IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[16] GE Perlin, AM Sodagar, KD Wise, "A neural amplifier with high programmable gain and tunable bandwidth," EMBS, pp. 3154-3157, 2008.

[17] Xiaodan Zou, Xiaoyuan Xu, Jun Tan, Libin Yao, Yong Lian. "A 1-V 1.1-μW Sensor Interface IC for Wearable Biomedical Devices," Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on, Page(s):2725 – 2728, 18-21 May 2008.

[18] Xiaodan Zou, Xiaoyuan Xu, Libin Yao, and Yong Lian, "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," J. Solid-State Circuits, page(s): 1067 - 1077, April 2009

[19] Mollazadeh, Mollazadeh, Kartikeya Murari, Gert Cauwenberghs, and Nitish Thakor, "Micropower CMOS Integrated Low-Noise Amplification, Filtering, and Digitization of Multimodal Neuropotentials," Biomedical Circuits and Systems, page(s): 1 – 10, 2009.