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A Low-Offset Analogue Front-End IC for Multi-Channel Physiological Signal Acquisition

Jinyong Zhang[1, 2], Lei Wang[1], Li Yu[1], Yabei Yang[1], Yuanting Zhang[1], and Bin Li[2]

Abstract—**This paper describes a low-offset analogue front-end (AFE) integrated circuit (IC) for multi-channel physiological signal acquisitions. The mixed signal IC consists of low-offset gain programmable instrumentation amplifiers (GPIAs), high sensitive current-to-voltage converters (I-V converters), reference and an 8-bit analogue-to-digital converter (ADC). The IC offered adjustable gains that were elaborated for various physiological signal acquisitions. The conditional signals were quantized by ADC that offered an optimal solution for portable applications. The circuit was fabricated in SMIC 0.18-µm mixed-signal CMOS technology, and core area of the whole IC measured 1.36 mm^2. The post-annotated simulations suggested that the system achieved a common-mode-rejection-ration (CMRR) of 142 dB, the adjustable gain from 31.6 dB to 76.5 dB, and the offset voltage less than 80 µV. The 8-bit ADC exhibited less than 0.8 LSB DNL and 1.1 LSB INL. Power dissipation of each channel and the ADC were approximately 348 µW and 1.65 mW under a 1.8 V single supply voltage, respectively. It is suitable for a wide range of high precision biomedical applications.**

I. Introduction

THE chronic measurement of low frequency and low amplitude physiological signals such as electrocardiography (ECG) and electroencephalography (EEG) using integrated systems requires analogue and digital signal processing with minimum number of external components and high performance [1, 2]. The analogue front-end (AFE) IC design is crucial for physiological signal acquisitions, because most physiological signals have relative weak signal strength and low frequency as listed in TABLE I [3, 4]. Besides, the input signal is DC-coupled directly with the skin-electrode interface. To accommodate these low signal-to-noise-ratio (SNR) signals, a multi-channel AFE IC with both low-offset gain programmable instrumentation amplifier (GPIA) and ADC is necessary, and for low amplitude current source signal a high sensitive current-to-voltage converter (I-V converter) should be incorporated.

In recent years, there are some biomedical front-end IC designs have been reported in [5-8]. However, some of them did not include an ADC, some of them did not have adjustable gain or multi-input-channel. In addition, a few attempts have been made for current signal acquisitions. Meanwhile, the acquisition system should be able to provide enough CMRR and low-offset performance.

In this paper we present a multi-channel configurable physiological signal acquisition AFE IC with low-offset voltage, where a high sensitive I-V converter and an 8-bit successive-approximation-register (SAR) ADC were integrated and the gain of the system was programmable. This initial version of the system was realized in a SMIC 0.18-µm mixed-signal CMOS technology.

TABLE I. PROPERTIES OF SEVERAL PHYSIOLOGICAL SIGNALS

Physiological Signals	Measurement Range	Gain Needed(dB)	Frequency Range(Hz)
EEG	25-300 µV	50-72	DC-150
ERG	5-900 µV	41-86	DC-50
EGG	10-1000 µV	40-80	DC-1
ECG	0.5-4 mV	28-46	0.01-250
EMG	0.1-5 mV	27-60	DC-500
PPG	5-100 nA	40-66*	0.05-40

* *amplified to be at 10 µA level.*

II. Circuit Implementation

The architecture of the implemented multi-channel AFE IC is shown in Fig. 1. It includes GPIAs, I-V converters, a multiplexer (MUX), reference, and a SAR ADC. The GPIA defines the offset level and common-mode-rejection-ration (CMRR) of the channel, and its gain is configurable to different physiological signal applications. I-V converters were designed for current signals. A multiplexer, time multiplexes the output of each channel and ADC to digitize the amplified signals from channels continuously at appropriate sampling rate. Moreover, a bias generator and a built-in digital control circuit were designed to generate the bias currents and gain select signals for the AFE IC, respectively.

A. Gain Programmable Instrumentation Amplifier

IA is a crucial block for high performance physiological signal acquisition systems. To solve the problems in resistors feedback network matching of a conventional IA [9], we adopted a novel IA circuit structure with current mirror [10]. It consists of low-offset operational amplifiers, current mirrors and a resistor array with the built-in digital interface.

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J.Y. Zhang is with Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China. He is also with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou, China. (e-mail: jy.zhang@sub.siat.ac.cn).

L. Wang, L. Yu, Y. B. Yang and Y. T. Zhang are with the Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China. (phone: 86-755-26803549; fax: 86-755-26803538; e-mail: wang.lei@siat.ac.cn).

B. Li is with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou, China.

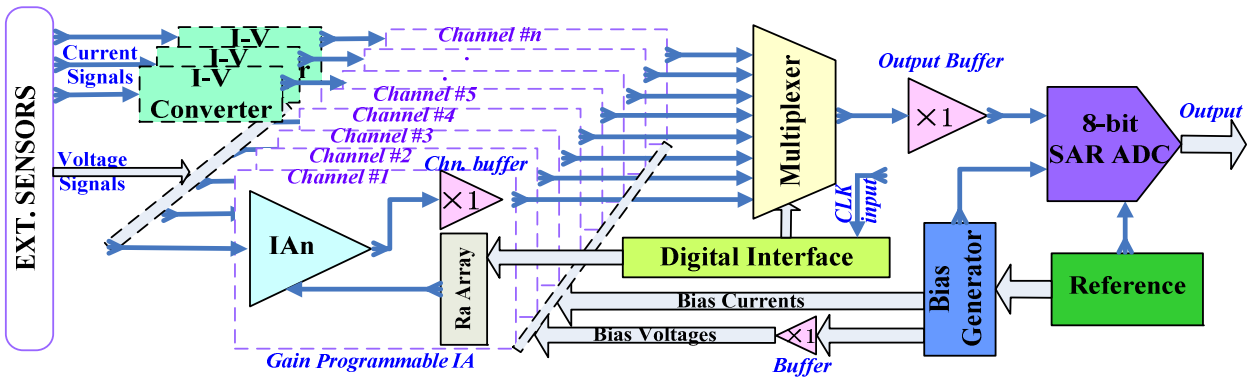

Fig. 1. Multi-channel analogue front-end IC architecture.

The gain of it is digitally configurable. Fig. 2 shows the block diagram of the GPIA.

As illustrated in Fig. 2, Vin+ and Vin- are physiological signals sensed from human body. The differential gain of the GPIA was given by: $A_v = 2[(Vin+)-(Vin-)]\times R_a / R_s$.

By digitally selecting the input of the decoder to connect the resistor array via the CMOS control switches, the GPIA was capable of providing programmable voltage gains when different Ra values were set.

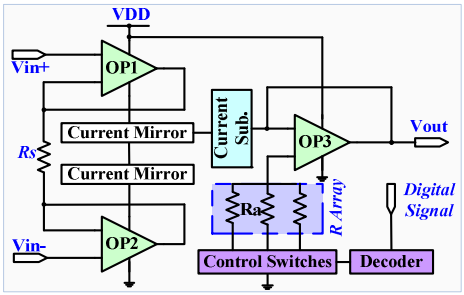

Fig. 2. Block diagram of the GPIA.

The circuit shown in Fig. 3 is the schematic of low-offset operational amplifier (OP-AMP). A continuous-time asymmetrical differential input structure with common-mode feedback (CMFB) circuit was used to minimize the offset of the operational amplifier [11]. In input stage, the MOS transistor pairs were designed as asymmetrical differential structure, they were cross-coupled to reduce the mismatching. In CMFB stage, the difference between Vin and Vout were detected and changed to feedback signals for input stage. This is a negative feedback network. By adjusting the bias current of the input stage, the Vin and Vout common-mode level could be maintained in same level. Finally, a careful layout was planned to reduce process-related deviations: (a) a common-centroid cross-coupling layout strategy together with poly guard rings were employed and (b) the layout of input pairs, active mirror loads and current sources were designed with dummies to minimize the effect of spacing-dependent parameter mismatch [12].

A. I-V Converter

I-V converter plays a vital role at the current input signal acquisition systems. Fig.4 shows the circuit of the proposed I-V converter that consists of the core converter, the error amplifier and the bias circuit. The output impendence of the MOS transistors to perform current conversions technology was used in this circuit [13]. But one potential problem in using such an approach was the biasing of the high-gain output nodes, which was solved by using a negative feedback circuit [14].

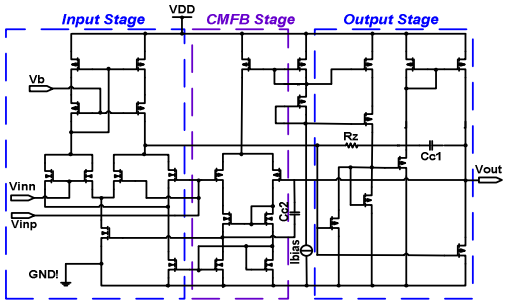

Fig. 3. Circuit of the low-offset operational amplifier.

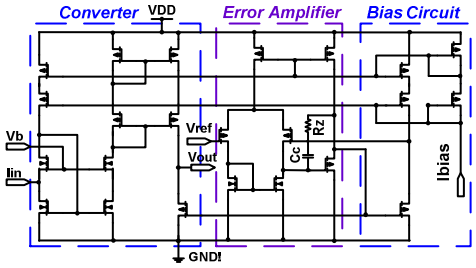

Fig. 4. Circuit of the I-V converter.

B. MUX/Analog-to-digital converter (ADC)

In this system, a MUX with multi-channel input and a resolution of 8-bit SAR ADC were usually presented when they used after the analogue signal conditioning. The block diagram is shown in Fig.5 (a). The SAR ADC consists of a sample-and-hold (SHA), an internal D/A converter (DAC), a comparator and a SAR logic block. The binary-weighted R-2R array is depicted in Fig.5 (b). It used a repeating cascaded structure of resistor values R and 2R. This improved the precision due to the relative ease of producing equal valued matched resistors.

A user controlled decoder selects up to 8-channel independent to sample and digitize the amplified signals. Every channel can be chosen by external selectable signals,

after conversion, digital data would be obtained. In this design, the signal after GPIA conditioning in each channel are multiplexed and digitized at the sampling rate of 1-500 ksps.

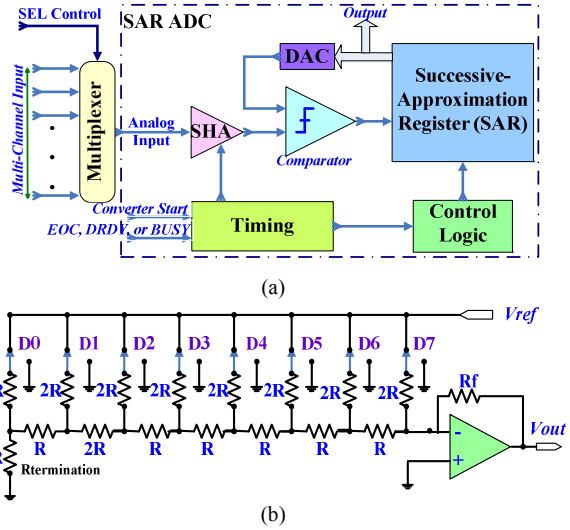

Fig. 5. Block diagram of MUX/SAR ADC (a) and binary-weighted R-2R array (b).

C. Reference/Bias generator

A novel compensation scheme for power- and temperature-independency of voltage/current reference was adopted in this design. The basic principle is that two outputs with the same dependency on supply and temperature were subtracted to obtain the compensation output [15]. Bias voltages and bias currents were generated from the voltage/current reference.

III. Results and Discussions

The presented multi-channel low-offset AFE IC was realized using the SMIC mixed-signal 0.18-µm 1P6M CMOS technology. Fig. 6 shows the complete layout of the AFE system chip, where the core circuit occupies about 1.36 mm^2 silicon area (excluding the ESD PADs).

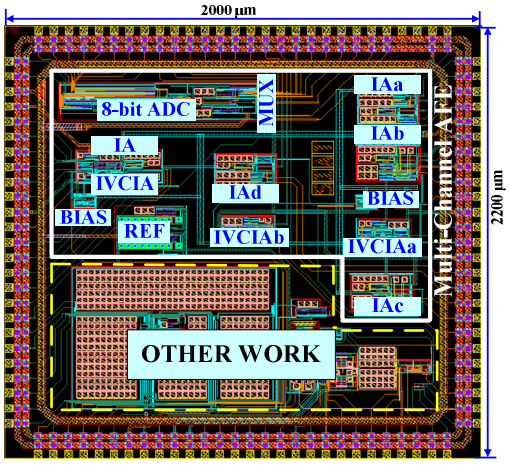

Fig. 6. Layout view of the analogue front-end IC.

Fig. 7 demonstrates DC sweep analysis of the low-offset OP-AMP. The OP-AMP was configured as a unity gain feedback. The simulation results showed good following characteristic between input and output voltage, the offset voltage was less than 80 µV by averaging.

The transfer characteristic of the I-V converter was plotted in Fig.8. The output voltage is almost linearly proportional to the input current signal at the rate of about 32mV/nA. The simulation results showed that the presented I-V converter capable of detecting very weak current source signals.

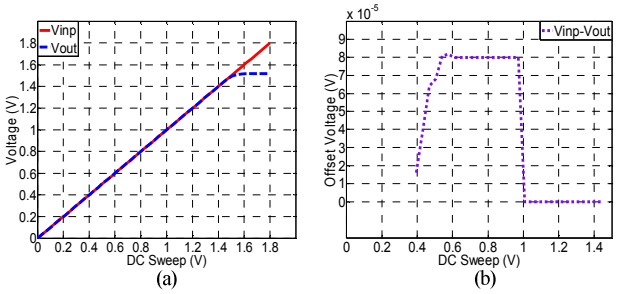

Fig. 7. The following characteristic (a) and offset tunning range simulations (b) of the OP-AMP connected as a unit-gain buffer.

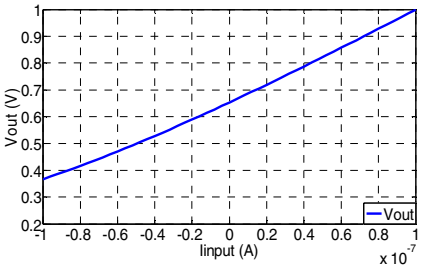

Fig. 8. Transfer characteristic of the I-V converter.

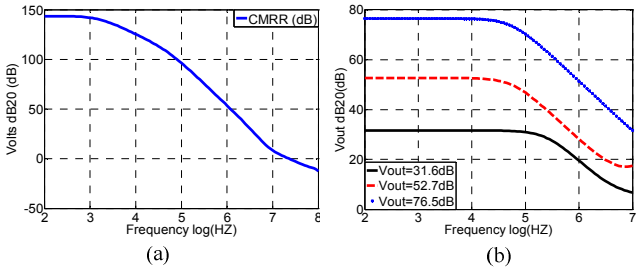

Fig. 9. CMRR performance (a) and frequency response (b)of the GPIA

The CMRR performance and frequency response of the GPIA are shown in Fig. 9. The results suggested at least 142 dB CMRR from DC to 1 KHz. The bandwidth of the GPIA was sufficient for physiological signals acquisitions since most of the physiological signals have bandwidths less than 1 KHz. According to the above simulation results, the GPIA gain could be programmed from 31.6 dB to 76.5 dB. Fig.10 shows the simulated waveform of one channel GPIA output and reconstructed ADC data output, where the analogue input was a voltage signal with amplitude about 2 mV. The signal was amplified by 60 dB and digitized by the ADC to 8-bit digital data at 250 ksps.

The ADC consumed 1.65 mW at 250 ksps from 1.8 V supply. Fig. 11 shows the integral nonlinearity (INL) and differential nonlinearity (DNL) of the 8-bit SAR ADC block.

The maximum value of DNL and INL are 0.8 LSB and 1.1 LSB, respectively.

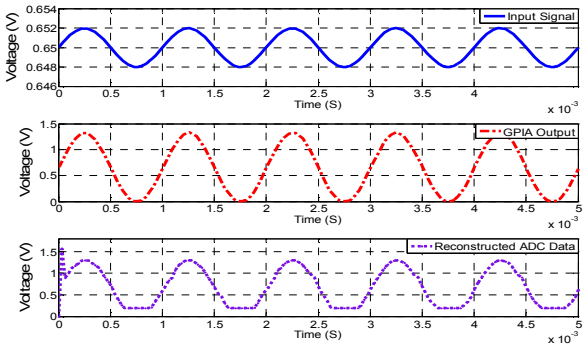

Fig. 10. Simulated waveform of the GPIA output and reconstructed ADC data.

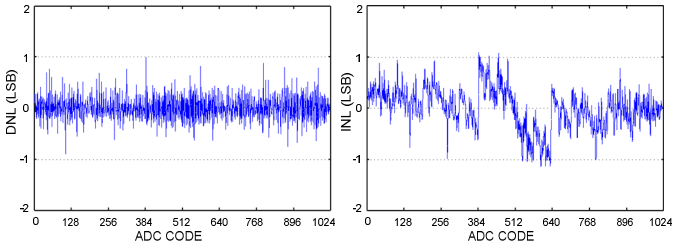

Fig. 11. The DNL and INL of the SAR ADC

Table II gives a summary of the performance of our design. It could be seen that the proposed AFE IC achieves a high CMRR, a low DC offset and a selectable gain, this system was fully integrated with a small chip area. The AFE IC has selectable system gain and supports multi-channel input. By integrated with a SAR ADC, it offered a good solution of physiological signal acquisitions. The ADC consumes relatively large power, so our future work will focus on reducing the power dissipation of the ADC.

TABLE II. PERFORMANCE SUMMARY OF THE AFE IC

BLOCK	PARAMETER	VALUE
GPIA	Supply Voltage (Typical)	1.8 V
	CMRR (@ 0~1kHz)	142 dB
	Gain Selection	31.6~76.5 dB
	Input Offset Voltage	<80 μV
	THD (@6mV Vpp input)	<0.9%
	Area	356×105 μm^2
	Power Dissipation (one channel including /excluding I-V converter)	348 μW
		114 μW
SAR ADC	Supply Voltage	1.8 V
	Resolution	8-bit
	Sampling Rate	1~500 ksps
	Input Range	0.21~1.56V
	DNL/ INL	±0.8 LSB/±1.1 LSB
	Gain Error	<1%
	Area	1000×200 μm^2
	Power Dissipation	1.65 mW @250 kHz
	Figure of Merit	25.8 pJ/conv

IV. CONCLUSIONS

A multi-input-channel low-offset AFE IC consisting of both front-end and ADC for physiological signal acquisitions was realized on a single chip. Gain per channel and channel can be electronically set according to varying needs of different physiological signal applications. Especially, it can be used for current signal acquisitions. The proposed system enables measurement of a multiplexed physiological signal with low-offset and reasonable power dissipation. The system offered the CMRR of 142 dB, the offset voltage less than 80 μV, one channel consumes only 348 μW from a single 1.8 V supply, and the 8-bit SAR ADC exhibited less than 0.8 LSB DNL, 1.1 LSB INL and 1.65 mW power dissipation at 250 ksps from 1.8 V supply voltage. This design was fabricated in SMIC mixed-signal 0.18-μm CMOS 1P6M technology and the core area of this IC measured 1.36 mm^2.

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