31st Annual International Conference of the IEEE EMBS
Minneapolis, Minnesota, USA, September 2-6, 2009

A Low-Power Noncoherent BPSK Demodulator and Clock Recovery Circuit for High-Data-Rate Biomedical Applications

Farzad Asgarian, *Student Member, IEEE*, Amir M. Sodagar, *Senior Member, IEEE*

***Abstract*—A novel noncoherent BPSK demodulator is presented for inductively powered biomedical devices. Differential Manchester encoding technique is used and data demodulation is based on pulse width measurement method. In addition to ultra low power consumption, high data rate without increasing the carrier frequency is achieved with the outstanding data-rate-to-carrier-frequency ratio of 100%. The proposed demodulator is especially appropriate for biomedical applications where high speed data transfer is required, e.g., cochlear implants and visual prostheses. The circuit is designed in a 0.18-µm standard CMOS technology and consumes as low as 232 µW@1.8V at a data rate of 10 Mbps.**

I. Introduction

IMPLANTABLE biomedical systems, which are being used in different applications such as functional muscular stimulation to overcome paralysis, and direct neural control of prosthetics [1], are mostly composed of three main parts: external controller, implant modules, and a wireless interface. Depending on the application, the external controller can be as simple as a power transmitter [2]. A more complicated controller can be in charge of generating and sending stimulation commands based on the acquired data from the external world. Moreover, power management and advanced signal processing are among the additional tasks that are expected from a powerful external controller [2]. The implant modules, including the central digital controller, stimulators and sensors are powered and connected to the external controller via the wireless interface. This interface should be able to wirelessly receive power and control/programming data (forward telemetry) and also transmit implant status and data to the external world (reverse telemetry). The wireless link for forward power and data telemetry is implemented using two closely-spaced, inductively-coupled coils. The RF front-end is comprised of a power regulator and a data demodulator/clock recovery block. In some biomedical applications, particularly where the implant interfaces with the central nervous system such as cochlear implants and visual prostheses (Fig. 1), high data rate transmission toward the implant is required [3], [4]. However, due to the fact that the power dissipation in the tissue increases with the carrier frequency squared ($\propto f^2$) [4], this high data rate can not be achieved by increasing the carrier frequency. Thus, in designing demodulator circuits for implantable biomedical devices, the goal is to maximize the data-rate-to-carrier-frequency ratio in order to obtain higher data rates with lower carrier frequencies and power consumption.

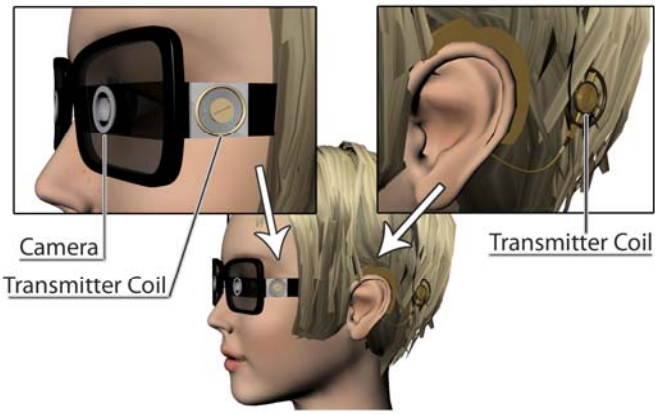

Fig. 1. Two examples of implantable biomedical devices.

Between different types of modulation techniques that have been reported, digital modulation schemes including binary amplitude shift keying (BASK) [5]-[7], binary frequency shift keying (BFSK) [8]-[12], binary phase shift keying (BPSK) [13]–[16], and quadrature phase shift keying (QPSK) [17], [18] are mostly used in implantable biomedical devices.

Generally in RF applications, FSK and PSK have wider usage than ASK because of their lower sensitivity to amplitude noise [19]. Also, nonconstant amplitude symbols in ASK, reduce the maximum amount of transferred power via the inductive link [2]. In the other hand, although the amplitude of symbols is fixed in FSK, using two different frequencies for data transmission will make this modulation only applicable on wideband inductive link applications [2]. These types of links require a low quality factor of the resonant circuit, which leads to inherently low power-transmission efficiency [2]. Another disadvantage of employing two carrier frequencies is limiting the data rate to the lower frequency and consequently decreasing the data-rate-to-carrier-frequency ratio. Thus, PSK modulation with constant amplitude symbols and fixed carrier frequency can be the best choice for high-data-rate biomedical applications.

Manuscript received April 23, 2009.

F. Asgarian is with Integrated Circuits and Systems Laboratory, Electrical & Computer Eng. Dept., K.N. Toosi University of Technology, Tehran, Iran (asgarian@ieee.org).

A.M. Sodagar is with Integrated Circuits and Systems Laboratory, Electrical & Computer Eng. Dept., K.N. Toosi University of Technology, Tehran, Iran, also with Center for Wireless Integrated Microsystems (WIMS), University of Michigan, Ann Arbor, USA (asodagar@umich.edu).

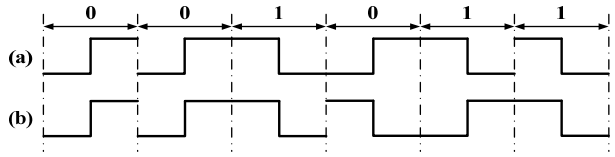

Fig. 2. Data encoding techniques: (a) Manchester encoding, (b) Differential Manchester encoding.

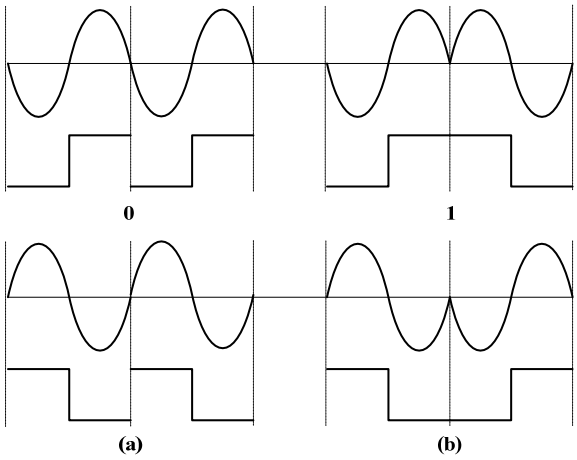

Fig. 3. Analog and digital waves of logic (a) "0" and (b) "1" symbols.

The authors have recently reported a BPSK demodulator [16] that benefits from a data-rate-to-carrier-frequency ratio of 100%, while [18] and [15] achieve a ratio of 59% and 20% respectively. In this paper another low power BPSK demodulator with a data-rate-to-carrier-frequency ratio of 100% is presented, which takes advantage of differential Manchester encoding in PSK modulation scheme. This paper is organized as follows. In section II after introducing the differential Manchester encoding technique, the proposed BPSK demodulator architecture and its components are described. Section III covers the simulation results and a comparison of PSK demodulators. Finally the conclusions are provided in section IV.

II. Proposed BPSK Demodulator

A. Differential Manchester Encoding

As shown in Fig. 2(a) in Manchester encoding there is always a mid-bit transition, which is used as a clocking mechanism and also its direction represents the digital data. Logic "0" is expresses by a low-to-high transition while logic "1"is indicated by a high-to-low transition at the center of each bit-time (according to different conventions the reverse definition might be true). However, in differential Manchester encoding, mid-bit transitions are only for clocking and the digital data is represented by the presence (logic "0") or absence (logic "1") of transition at the beginning of the bit intervals (Fig. 2(b)).

Manchester encoding is considered as a special case of BPSK modulation, where the data controls the phase of a square wave carrier whose frequency is the data rate. Therefore, it can be said that all conventional noncoherent

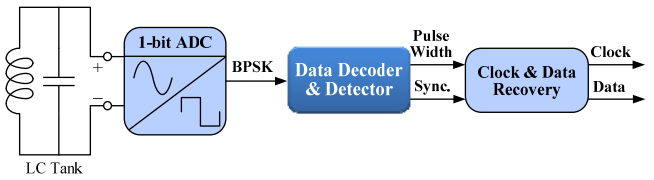

Fig. 4. Block diagram of the proposed demodulator.

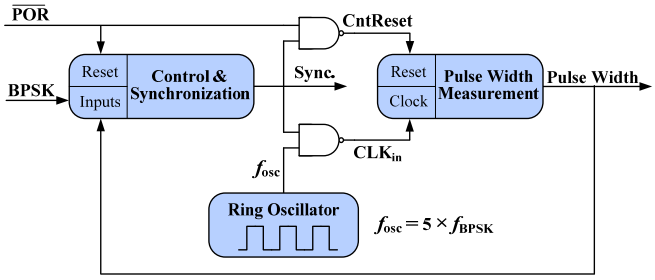

Fig. 5. Block diagram of the data decoder/detector.

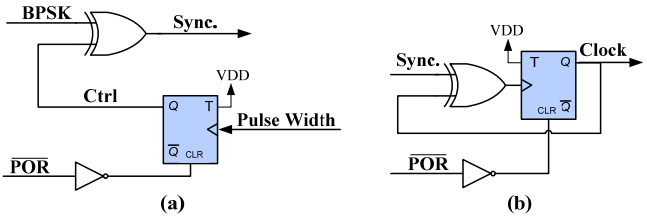

Fig. 6. Schematic diagram of (a) Control and synchronization module, (b) Clock recovery unit.

BPSK demodulators [15], [16] use this type of data encoding technique. In this paper differential Manchester encoding is employed with BPSK modulation, which results in two different waveforms for each logic "0" and "1" symbols (Fig. 3).

B. Demodulator Architecture

Block diagram of the proposed demodulator is shown in Fig. 4. In this architecture, a low power comparator is used to digitize the received analog carrier. The digitized signal (*BPSK*) is then fed to the data decoder/detector block. This module implements the core idea proposed in this paper and is capable of measuring the pulse width between two consecutive transitions that occur in the middle of each bit-time. Based on Fig. 3 it is clear that when a "1" is received, the *BPSK* signal remains unchanged for a bit-time (T_{BPSK}) between the mid-bit transitions. However, when a "0" is received, the *BPSK* signal changes its state after $0.5T_{BPSK}$.Thus, to detect the received data, this block must discriminate between the pulse widths of $0.5T_{BPSK}$ and T_{BPSK}. The data detector and its components are illustrated in Fig. 5 and will be discussed in part B of this section. Finally the clock and data recovery unit generates the desired bit-stream and also extracts a constant frequency clock from the received carrier. This block is explained in part C of this section.

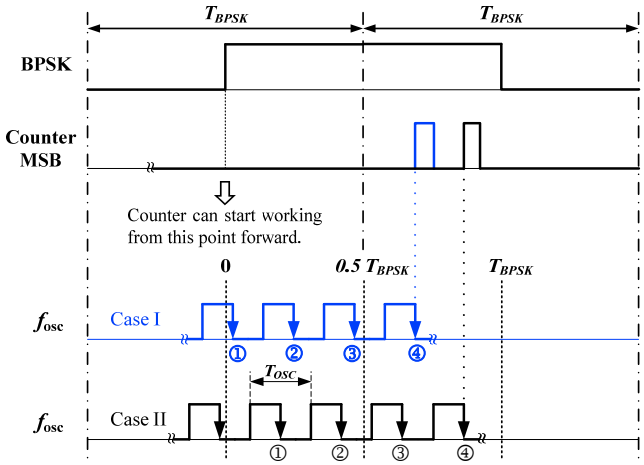

Fig. 7. Two worst cases for determining the range of f_{OSC}.

C. Data Decoder/Detector

As shown in Fig. 5 the data decoder/detector consists of a pulse width measurement unit along with the control and synchronization module (Fig. 6(a)). The pulse width measurement unit comprises a 3-bit asynchronous counter. This counter measures the time between the occurrence of each mid-bit transitions and the proceeding level change in the *BPSK* signal. For a received "1" symbol, the most significant bit of the counter (MSB) goes high between $0.5T_{BPSK}$ and T_{BPSK}. This bit is shown as the *Pulse Width* signal in Fig. 5.

In order to fulfill these requirements and due to the fact that in differential Manchester encoding after each "1" symbol the direction of the mid-bit transition changes, the counter is controlled by both *BPSK* and *Pulse Width* signals (Fig. 5). The *Sync.* signal is indeed the *BPSK* signal, which is conditionally inverted using an XOR gate every time a "1" symbol is detected (Fig. 6(a)).

Another important parameter for the counter is the frequency range of the ring oscillator (f_{OSC}). As mentioned before, when the *BPSK* signal is unchanged between two consecutive mid-bit transitions, the MSB of the counter goes high somewhere between $0.5T_{BPSK}$ and T_{BPSK}. According to Fig. 7 where two worst cases are illustrated, we need to have:

$$3T_{OSC} > 0.5T_{BPSK} \quad (1)$$

and

$$4T_{OSC} < 0.5T_{BPSK}, \quad (2)$$

which result in:

$$1/6\ T_{BPSK} < T_{OSC} < 1/4\ T_{BPSK}. \quad (3)$$

Thus, the oscillator frequency range is defined as:

$$4f_{BPSK} < f_{OSC} < 6f_{BPSK}. \quad (4)$$

D. Clock and Data Recovery Circuit

The *Sync.* signal always produces a rising edge in the middle of each bit-time. Therefore, this signal can be used to recover a constant-frequency clock from the received signal. However, if only the rising edges are used, the frequency of the recovered clock will be half of the data rate, which will not be appropriate for data manipulation. Thus, both rising and falling edges are used to generate the *Clock* signal (Fig. 6(b)). Although the duty cycle of this clock is not 50%, the frequency of its rising edges is the same as the data rate, allowing for proper data handling.

To synchronize the detected data with the recovered

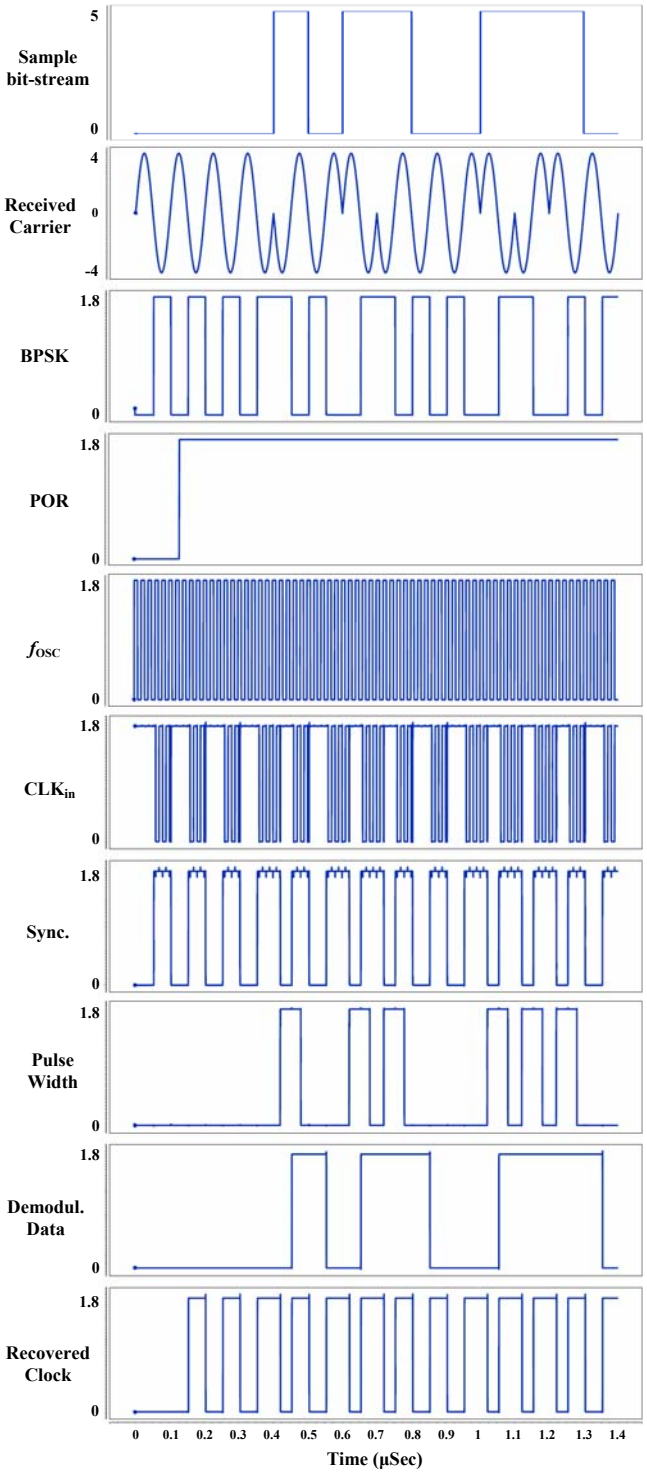

Fig. 8. Simulation waveforms of the proposed BPSK demodulator.

TABLE I
COMPARISON OF PSK DEMODULATORS

Reference	Modulation	Carrier Frequency (MHz)	Data Rate (Mbps)	D.R.C.F[a] Ratio	Power Consumption (μW)
[13]	BPSK	10	1.12	11.2 %	610 at 1.8 V
[14]	BPSK	13.56	0.02	0.15 %	3000 at 3.3 V
[15]	BPSK	4	0.8	20 %	59 at 1.8 V
[16]	BPSK	10	10	100%	251 at 1.8 V
[17]	QPSK	13.56	4	29.5 %	750 at 1. 8 V
[18]	QPSK	13.56	8	59 %	910 at 1.8 V
This work	BPSK	10	10	100%	232 at 1.8 V

a. Data Rate to Carrier Frequency.

clock, the MSB of the counter is stored in a D latch. The received data bit-stream is recovered by sampling the output of this latch with the rising edges of the *Sync.* signal, which leads to equal bit-times for detected 0's and 1's.

III. Simulation Results

The proposed demodulator has been designed in a 0.18-μm CMOS technology. Important waveforms resulted from circuit simulations are shown in Fig. 8 for a sample data bit-stream with a carrier frequency of 10 MHz. All other traces are named with the ones used in Figs. 4-6. According to simulation results, the demodulator circuit merely consumes 232/132 μW with/without the ring oscillator from the 1.8V power supply at 10 Mbps data rate.

A brief comparison between the previously reported PSK demodulators and our work is given in Table I. It is clear that except this circuit and the one introduced recently by the authors [16], all other reported works suffer from low data-rate-to-carrier-frequency ratio. This ratio is a key factor in designing demodulators for implantable biomedical devices. In comparison with our previous work [16], this architecture exhibits lower power dissipation.

IV. Conclusions

A novel noncoherent BPSK demodulator and clock recovery circuit was presented, which uses pulse width measurement method in order to extract both clock and data from the received RF signal. Besides simplicity and low power consumption, the proposed demodulator benefits from an outstanding data-rate-to-carrier-frequency ratio of 100%. Thus, it can easily achieve high data rates with lower carrier frequencies, which is desirable in biomedical implants.

References

[1] A.M. Sodagar, K. Najafi, "Wireless interfaces for implantable biomedical microsystems," Proc. IEEE Int. Midwest Symp. Circuits and Systems, vol. 2, pp. 265-269, Aug. 2006.

[2] M. Sawan, Y. Hu, and J. Coulombe, "Wireless smart implants dedicated to multichannel monitoring and microstimulation," IEEE Circuits and Systems Magazine, vol. 5, Issue 1, 2005.

[3] J.D. Weiland, M.S. Humayun, "Visual prosthesis," Proc. IEEE, vol. 96, Issue 7, pp. 1076-1084, July 2008.

[4] M. Ghovanloo, and K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," IEEE Trans. Circuits and Systems I: vol. 51, pp. 2374-2383, Dec. 2004.

[5] J. Coulombe, J.-F. Gervais, and M. Sawan, "A cortical stimulator with monitoring capabilities using a novel 1 Mbps ASK data link," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), vol. 5, pp. 53-56, May 2003.

[6] H. Yu and K. Najafi, "Low-power interface circuits for bio-implantable microsystems", Technical Digest, IEEE Int. Conf. Solid-State Circuits, San Francisco CA, February 2003.

[7] A. Djemouai, M. Sawan, "New CMOS current-mode amplitude shift keying demodualtor (ASKD) dedicated for implantable electronic devices," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), vol. 1, pp. I-441-4, May 2004.

[8] M. Ghovanloo and K. Najafi, "A high data transfer rate frequency shift keying demodulator chip for the wireless biomedical implants," Proc. 45th IEEE Midwest Symp. Circuits and Systems, vol. 3, pp. 433-436, Aug. 2002.

[9] M. Ghovanloo and K. Najafi, "A high data-rate frequency shift keying demodulator chip for the wireless biomedical implants," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), vol. 5, pp. 45-48, May 2003.

[10] M. Ghovanloo and K. Najafi, "A fully digital frequency shift keying demodulator chip for the wireless biomedical implnats," Proc. IEEE Southwest Symp. Mixed-Signal Design, pp. 223-227, Feb. 2003.

[11] M. Ghovanloo and K. Najafi, " A tri-state FSK demodulator for asynchronous timing of high-rate stimulation pulses in wireless implantable microstimulators," Proc. 2nd Int. IEEE/EMBS Conf. Neural Eng, pp. 116-119, Mar 2005.

[12] M. Dong, "A wideband frequency-shift keying demodualtor for wireless neural stimulation microsystems," Proc. IEEE 19th Int. Conf. VLSI Design, 2006.

[13] Y. Hu, and M.Sawan, "A fully-integrated low-power BPSK demodualtor for implantable medical devices," IEEE Trans. Circuits and Systems-I: Regualr Papers, vol. 52, Issue 12, pp. 2552-2562, Dec. 2005.

[14] Z. Luo, S. Sonkusale, "A novel BPSK demodulator for biological implants," IEEE Trans. Circuits and Systems-I: Regualr Papers, vol. 55, Issue 6, pp. 1478-484, July 2008.

[15] C.-S.A. Gong, M.-T. Shiue, K.-W. Yao, T.-Y. Chen, "Low-power amd area-efficient PSK demodualtor for wirelessly powered implantable command receivers," Electronics Letters, vol. 44, Issue 14, pp. 841-842, July 2008.

[16] F. Asgarian, A.M. Sodagar, "A high-data-rate low-power BPSK demodulator and clock recovery circuit for implantable biomedical devices," Proc. 4th Int. IEEE/EMBS Conf. Neural Eng., pp. 407-410, April 29 – May 2, 2009.

[17] S. Deng, Y. Hu, M. Sawan, "A high data rate QPSK demodulator for inductively powered electronics implants," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), pp. 2577-2580, May 2006.

[18] Z. Lu, M. Sawan, "An 8 Mbps data rate transmission by inductive link dedicated to implantable devices," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), pp. 3057-3060, May 2008.

[19] B.Razavi, *RF Microelectronics*, Prentice-Hall Inc., 1998.