

An Integrated Circuit for Wireless Ambulatory Arrhythmia Monitoring Systems

Hyejung Kim, *Student Member, IEEE*, Refet Firat Yazicioglu, *Member, IEEE*, Tom Torfs, Patrick Merken, Chris Van Hoof, *Member, IEEE*, and Hoi-Jun Yoo, *Fellow, IEEE*

Abstract— An ECG signal processor (ESP) is proposed for the low energy wireless ambulatory arrhythmia monitoring system. The ECG processor mainly performs filtering, compression, classification and encryption. The data compression flow consisting of skeleton and modified Huffman coding is the essential function to reduce the transmission energy consumption and the memory capacity, which are the most energy consuming part. The classification flow performs the arrhythmia analysis to alert the abnormality. The proposed ESP IC is implemented in 0.18- μm CMOS process and integrated into the wireless arrhythmia monitoring sensor platform. By integration of the ESP, the total system energy reduction is evaluated by 95.6%.

I. INTRODUCTION

Recently, with the increase of the interests in the healthcare, the need for the ambulatory arrhythmia monitoring system has been rising exponentially. The monitoring system records ECG signal continuously in ambulatory condition for a sizable time like several hours. The system transmits the record data to the user or the healthcare center like hospital when the alert ECG signal is detected or the recording period is finished. In order to monitor and analyze the ECG signal, the functions operated at the clinical instrument such as signal sensing and the classification should be integrated into the light-weight, ambulatory monitoring system [1].

The most important requirements for the ambulatory monitoring system are ultra low energy operation for the long battery life time and a small footprint for wearability. In general, since the highest energy consuming parts are the memory transaction blocks and the wireless communication blocks than the processing block [2, 3], the data processing as much as possible before transmission is the most efficient method to reduce the total system energy consumption. Many micro-watt power sensor processors have been proposed [2, 5, 6]. However, they still require too many operating cycle, which is related to the energy consumption. In this paper, the ECG signal processor (ESP) is proposed to perform the required signal processing for the ECG monitoring system under very low energy budget.

Manuscript received April 17, 2008.

Hyejung Kim and Hoi-Jun Yoo are with the Korea Advanced Institute of Science and technology (KAIST), 373-1, Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea (phone: +82-42-869-8068; fax: +82-42-869-3410; e-mail: seeseah@eeinfo.kaist.ac.kr).

Refet Firat Yazicioglu, Tom Torf, Patrick Merken, and Chris Van Hoof are with the IMEC, 3001 Leuven, Belgium.

Chris Van Hoof is also with Katholieke Universiteit Leuven, Belgium.

The energy reduction is achieved by the efficient transmission mode, data reduction scheme, the arrhythmia detection. In addition, by evaluating the wireless ambulatory arrhythmia monitoring platform integrating the ESP, the effectiveness of ESP will be discussed.

II. WIRELESS TRANSMISSION MODE

We propose the scenario for three wireless transmission modes to reduce the radio power module as shown in Fig.1. The first mode of continuous monitoring mode transmits all the samples at every few seconds or minutes. In order to reduce the transmission bandwidth, the sampled data is packed by the compression algorithm before transmission. The second mode of alert detection mode transmits only the sections that are physiologically important instead of continuously transmitting the total range of ECG signal. For example, if the abnormal heartbeat is detected, only the detected abnormality including the 2 seconds before and after the detected abnormal heartbeat is transmitted as shown in Fig.1(b). The last heart rate monitoring mode monitors the heart rate (average RR interval) or other significant extracted features instead of the ECG signal, and transmits periodically. In the presented modes, the ESP has to perform the compression algorithm, feature extraction such as RR interval, and abnormal heartbeat analysis. In order to perform the presented mode, the various algorithms such as compression, feature extraction, and abnormal heartbeat analysis should be performed in real time. The ESP is designed and integrated to perform the mentioned functions.

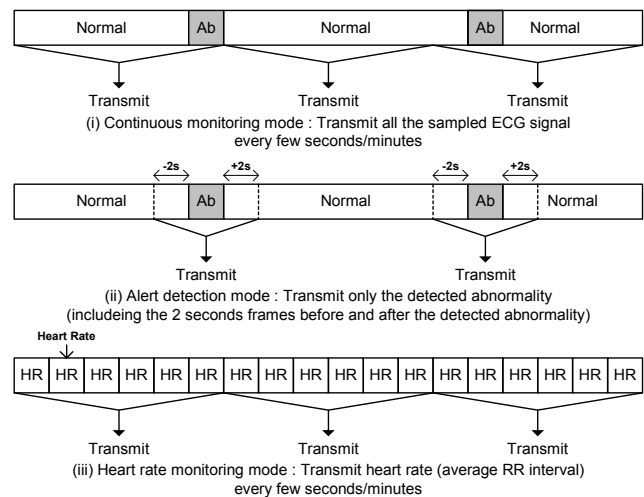


Fig. 1. Three Wireless Transmission Modes

III. ECG SIGNAL PROCESSOR

A. Algorithm Overview

The proposed ECG signal processor executes four functions: filtering, compression, ECG classification and encryption. Fig.2 illustrates the functions along with its simplified block diagram. The ECG sensing data is digitized and transmitted to the ESP module. At first, the filtering unit is applied to reduce the noises such as baseline wander, power line interference, and high frequency noise. After filtering, two major main processing steps, compression and classification, are applied. The compression flow combines the lossy and the lossless algorithm, which are the skeleton, delta coding and the Huffman coding. The classification flow extracts the features and analyzes whether the current heartbeat has the abnormality. Finally, the compressed data and the analyzed results are encrypted for protecting the user privacy and authentication and stored to the data memory until the user wants to get the results.

To increase the parallelism and utilization of the hardware, the three heterogeneous-processor architecture is proposed: pre-processor, main processor, and post-processor. Each processor provides the specific functionalities operating independently. The register and the 3 kinds of memory blocks are integrated. The function specific processor integration reduces the required the cycles per sample, to 1 cycle/sample. Moreover, for low power consumption, each processing unit can be individually enabled or disabled by the clock gating method according to the necessity. In the alert detection mode, a clock controller monitors an incoming workload, and enables the clock to the required unit when it is necessary.

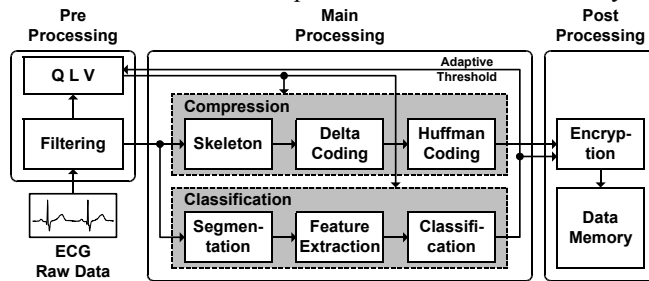


Fig.2. Flow graph of the proposed ECG signal processing Algorithm

B. Data Compression Flow

The compression flow consists of three steps: skeleton, delta coding, and Huffman coding (Fig.3(a)). The first step of skeleton is constructed with essential sample to reduce not only the transmission bandwidth, but also the on-chip memory capacity and number of the memory access during the processing. The main idea of the proposed skeleton algorithm is that the number of bits is assigned differently according to the information level by quad level vector (QLV) [4]. In other words, more bits are assigned to the highest level block like QRS, and fewer bits are assigned to the lower level block like TP segment (Fig.3(b-ii)). Since the skeleton is a lossy compression algorithm, a compression error is produced.

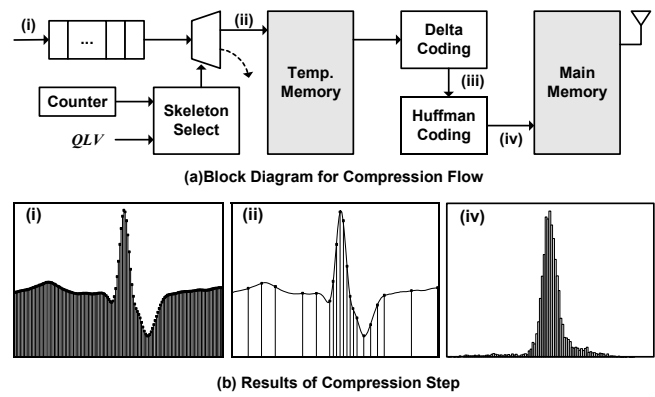


Fig.3. Data Compression Flow

Thus, the goal of the skeleton is reduction of the error rate while maintaining the high compression ratio (CR). The output format of the skeleton consists of the signal amplitude and the sampling interval for the later decoding operation. When decoding, the linear interpolation method is used for the smooth reconstructed waveform with small error rate.

The delta coding and the lossless compression algorithm are adapted after the skeleton method. The Huffman coding is selected because it provides minimum encoding cost when the original data has the unique distribution [7]. After the delta coding, the input data has Gaussian distribution as shown if Fig.3(b-iv). More than 50% of the data are located near the zero, thus, these high frequently occurring data can be transformed with the short length of code by the Huffman coding table. In this work, the modified 4-bit-wise Huffman coding table is proposed, which divides the entire range into the 4 groups to reduce the length and the number of the prefix code bits. The modified coding method transforms the sample oriented format into the 4-bit-word oriented stream for the efficient memory access with the variable resolution.

The compression performance is evaluated by using MIT/BIH Arrhythmia Database [8] as shown in Fig.3(b). The average CR of the skeleton and the Huffman coding is approximately 8.4:1 and 1.88:1, respectively. The overall CR would be 15.8:1. The error rate between the original and the reconstructed data is indicated by percentage root mean square difference (PRD) index. The PRD is defined as:

$$PRD(\%) = \sqrt{\frac{\sum_{i=1}^N (x_i - \tilde{x}_i)^2}{\sum_{i=1}^N x_i^2}} \times 100 \quad (1)$$

where x_i and \tilde{x}_i are the original data and the reconstructed data, respectively. The PRD is 0.641%.

C. ECG Classification Flow

The second flow of the main processing is the classification. It consists of the segmentation, the feature extraction and the classification stages. One heartbeat is segmented from the P wave to the next P wave of the following heartbeat. The significant features of each heartbeat, such as the R point, RR interval, amplitude of R point, average RR interval, QRS duration and existence of QRS [9], should be extracted for the next classification stage.

The classification algorithm checks whether the current heartbeat has abnormal arrhythmia. Various classification algorithms can be employed according to the variability of subjects and the environmental variation. Thus, the RISC architecture is adapted to enhance programmability at the classification stage. The RISC is designed in 3-stage pipeline with 16-bit Instruction Set Architecture (ISA) with 2kB code memory. Some function-specific datapath and the related instructions are supplemented to reduce the operating cycle and the code size.

In this paper, the 9 disorder symptoms are chosen, such as bradycardia, tachycardia, asystole, skipped beat, R-on-T, bigeminy, trigeminy, PVC (Premature Ventricular Contraction), and APB (Atrial Premature Beat), and each symptom can be characterized by the simple numerical calculation based RR interval [10]. Fig.4 shows the flow diagram for the arrhythmia detection operation, and the arrhythmia conditions. When the extracted features meet the specific condition, the current heartbeat is classified as the disorder heartbeat. Otherwise, the heartbeat is regarded as normal. The accuracy of R peak detection is crucial for the reliable analysis in this flow, because the R peak contains the primary data for arrhythmia analysis like RR interval [6]. Table-I shows the evaluation results of sensitivity and the positive predictivity in proportion to the white noise level.

D. Post Processing Stage

The post processing stage consists of encryption and data memory. AES-128 algorithm for data encryption is selected because it is widely used [11]. The results from the main processing are post-processed only when the abnormal heartbeat is detected to save the system resource. So if the disorder heartbeat is detected, the abnormal heartbeats with 2 seconds before and after the abnormality are transmitted to the post processing block. Otherwise, when the normal beat is detected, the post processing block and main memory block goes to sleep by clock gating method.

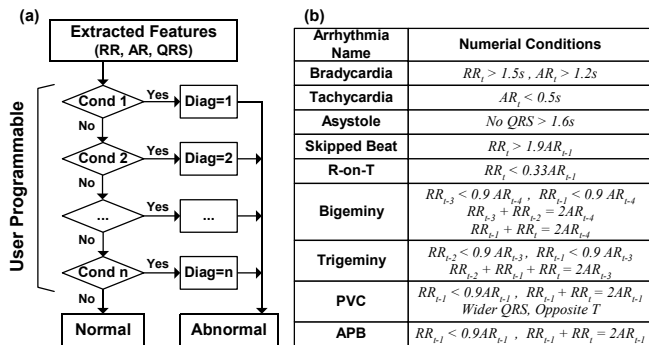


Fig.4. (a) Arrhythmia Analysis Flow Diagram (b) Selected 9 Major Arrhythmia Symptoms and Their Numerical Conditions [10]

TABLE - I. R PEAK DETECTION EVALUATION PERFORMANCE WITH THE NOISE

SNR (dB)	-10	-5	0	5	10	15	20	No Noise
SS (%)	95.63	97.38	98.25	100	100	100	100	100
PP (%)	97.04	99.70	100	100	100	100	100	100

IV. ARRHYTHMIA MONITORING SYSTEM PROTOTYPE

The ESP is implemented into a chip by using 1-poly 6-metal 0.18μm CMOS technology. Fig.5 shows the chip microphotograph and the size is 3.0 mm x 3.0 mm with the 10.5kB SRAM. The operating frequency is same as data sampling rate, between 250 and 1000 sample/sec. Table-II shows the performance summary. The ESP has been integrated into IMEC's single channel biopotential monitoring platform as shown in Fig.5. This platform consists of IMEC's proprietary single channel biopotential readout circuit [12], an off-the-shelf low-power microcontroller (MSP430) [5], a low-power radio chip [13], and the ESP.

The operation of the system can be described as follows: The single channel biopotential readout circuit performs the amplification and signal conditioning on ECG signal, while rejecting mains interference and electrode polarization offset voltage. The readout circuit makes use of chopper modulation, which ensures low 1/f noise and high CMRR [12]. Microcontroller digitizes the output of the readout circuit and sends the digitized ECG waveform to the ESP chip. The ESP performs the ECG signal processing in real time and the processed output such as the compressed/encrypted data, R peak detection, alert detection and the diagnosis are received by the microcontroller. The skeleton data and the alert detecting are transmitted through the wireless channel.

An ECG signal from MIT-BIH [8] (record 118, 213) is fed to the monitoring system. The sampling rate and the operating frequency of the test setup is 360Hz. Fig.6 shows the measured waveform for the skeleton operation at the continuous monitoring mode. The QLV is generated according to the ECG delineation. Afterwards, the essential samples for skeleton are extracted and stored to the temporary memory (TM). TM write enable signal occurs more frequently at the QRS complex than the other part like plane T-P segment (Fig.6(b)). So we can see that the QRS complex data is more preserved than other parts. The skeleton output consists of QLV and the signal amplitude (Fig.6(c-d)), and they are reconstructed on the receiver side with small error rate (Fig.6(e)). The measured CR is 8.1:1 with 0.94% PRD.

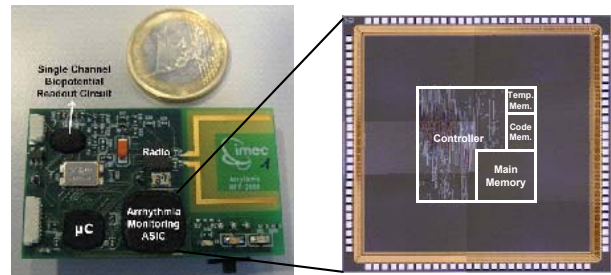


Fig. 5. The Wireless Arrhythmia Monitoring System with ESP IC

TABLE-II. PERFORMANCE SUMMARY

Process Technology	0.18 μm
Sampling Rate	250 – 1000 sample/sec
Operating Frequency	250Hz – 1kHz
Data Bit Width	12bit (AFE) / 16bit (ESP)
Memory Capacity	0.5kB TM / 2kB CM / 8kB DM
Area (Pad Limit)	9mm ² (Chip) / 2.25mm ² (Core)

Fig.7 shows the measured waveform for the alert detection mode operation. The R peak are successfully detected after the pre processing (Fig.7(b)), and the alert detection signal for the abnormal heartbeat is generated after the classification processing (Fig.7(c)). The only skeleton data for the abnormal heartbeat with ± 2 seconds range is transmitted to the receiver, then they are reconstructed (Fig.7(d-e)).

Fig.8 shows the evaluation result for energy break-down and the effectiveness of the proposed EPS chip. The sampling rate is 1kHz, and the probability of abnormality is assumed to be 10%. By integration of the ESP with data compression, classification and the alert detection mode operation, the overall energy consumption is reduced by 95.6%. The significant energy reduction can be achieved at the radio energy saving.

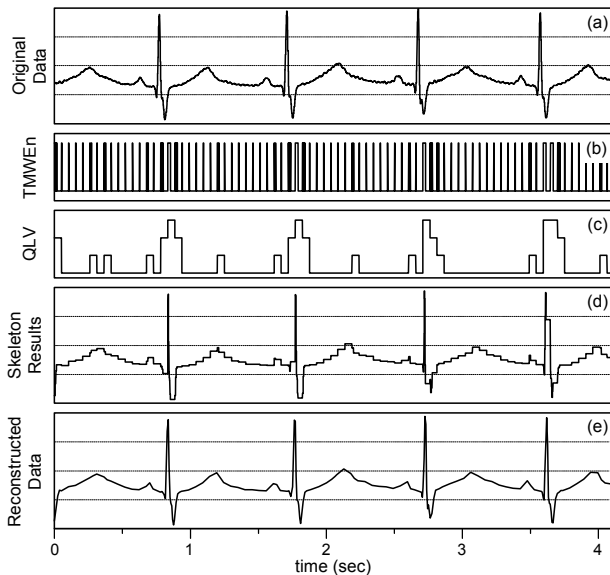


Fig. 6. Measured Results of Skeleton Operation with MIT-BIH Record 231 (a) Original Data (b) Temporary Memory Write Enable (c) QLV Output (d) Skeleton Data Output (e) Reconstructed Data on the Receiver Side

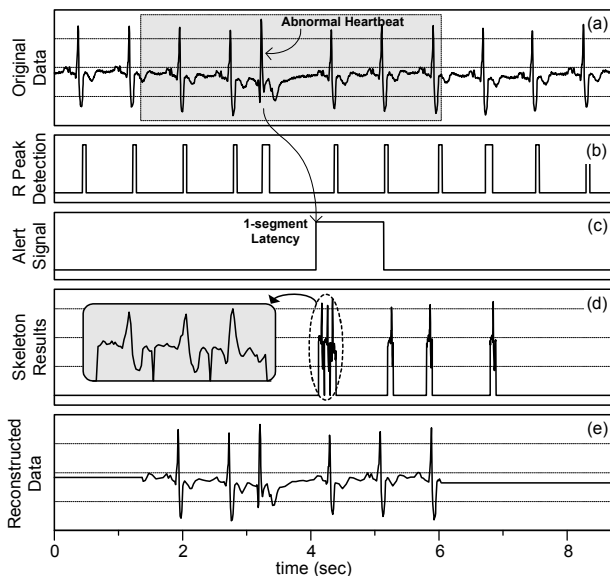


Fig. 7. Alert Detection Mode with MIT-BIH Record 118 (a) Original Data (b) R Peak Detection Output (c) Alert Detection Output (d) Selective Skeleton Output for Abnormal Heartbeat (e) Reconstructed Data on the Receiver Side

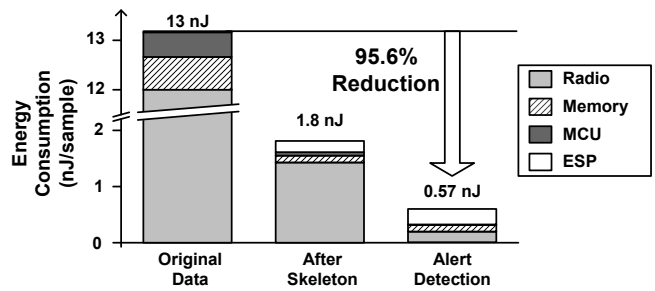


Fig.8. Energy Break-down of the Wireless Arrhythmia Monitoring System by Using ESP Chip

V. CONCLUSION

An ECG signal processor IC is proposed and implemented to reduce overall system energy consumption for the wireless arrhythmia monitoring system application. The ESP mainly performs the data compression and the arrhythmia detection. The performance is evaluated by implementing the sensor platform with MIT/BIH Arrhythmia Database. The measure CR is 8.1:1 with 0.94% PRD. The total system energy reduction is evaluated by 95.6% at the proposed alert detection mode.

REFERENCES

- [1] D. Jambaudon, J. Sztajzel, K. Sievert, T. Landis, and R. Sztajzel, "Usefulness of Ambulatory 7-Day ECG Monitoring for the Detection of Atrial Fibrillation and Flutter After Acute Stroke and Transient Ischemic Attack," *Stroke, Journal of American Heart Association*, pp. 1647-1651, vol.35, May 2004
- [2] H. Kim, S. Choi, and H.J Yoo, "A Low Power 16-bit RISC with Lossless Compression Accelerator for Body Sensor Network System," *Proc. of ASSCC*, Nov.2006
- [3] S. J Song, N. Cho, S. Kim, J. Yoo and H.J Yoo, "A 2Mb/s Wideband Pulse Transceiver with Direct-Coupled Interface for Human Body Communications," *Proc. of ISSCC*, Feb.2006
- [4] H. Kim, Y. Kim, and H.J Yoo, "A Low Cost Quadratic Level ECG Compression Algorithm and Its Hardware Optimization for Body Sensor Network System," *IEEE Proc. of EMBC*, Aug. 2008
- [5] Texas-Instruments, "MSP430F149 mixed signal microcontroller datasheet," online, June 2004
- [6] N. Ickes, D. Finchelstien, and A. P. Chandrakasan, "A 10-pJ/instruction, 4-MIPS Micropower DSP for Sensor Application," *Proc. of ASSCC*, Nov.2008
- [7] "Health informatics. Standard communication protocol. Computer-assisted electrocardiography," *British-Adopted European Standard BS EN 1064:2005*
- [8] <http://www.physionet.org/physiobank/database/mitdb/>
- [9] P. Chazal, S. Palreddy, W.J. Tompkins, "Automatic Classification of Heartbeats Using ECG Morphology and Heartbeat Interval Features," *IEEE Trans. Biomed. Eng.*, vol.51, no.7, pp.1196-1206, Jul. 2004
- [10] D.C. Reddy, "Biomedical Signal Processing - Principles and Techniques," *Mc.Graw Hill*, 2005
- [11] T. Good, "Very Small FPGA Application-Specific Instruction Processor for AES," *Tran.CAS*, vol.53, no.7, Jul.2006
- [12] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μ W 60nV/ $\sqrt{\text{Hz}}$ Readout Front-End for Portable Biopotential Acquisition Systems" *IEEE JSSC*, vol. 42, no. 5, May 2007
- [13] Nordic-VLSI, "nRF2401A ultra low-power 2.4GHz transceiver," <http://nvlssi.no>