31st Annual International Conference of the IEEE EMBS
Minneapolis, Minnesota, USA, September 2-6, 2009

Towards Circuit Integration on Fully Flexible Parylene Substrates

Ke Wang, Marice v Deurzen, Nico Kooyman and Michel M. J. Decré

Abstract— **We present a substrate transfer technology which allows devices to be fully processed using conventional silicon-based fabrication techniques prior to their integration with parylene. A parylene-based metal microelectrode array with high-temperature silicon oxide passivation layers was demonstrated. Combining high quality devices from well-established processes with thin, flexible and biocompatible substrates, this technology could provide exciting opportunities, especially in biomedical applications such as implantable neural interfaces.**

I. INTRODUCTION

Over the past years, the integration of MEMS and electronics on flexible plastic substrates has received significant interest and research effort. These flexible devices have found applications in an increasing number of fields, such as displays, chip-in-paper, sensor skins, wearable electronics and biomedical technologies. Pioneered by the display industry, one of the common fabrication approaches is to build the device structure directly on polymer films supported by rigid substrates. A major problem is that the maximum temperature tolerated by polymers is typically 150ºC or less, much lower than what is needed in many standard silicon-based fabrication steps. Therefore studies in this area have focused on developing low-temperature processes and materials. Amorphous silicon [1] and polysilicon [2] thin film transistors [2](TFTs) have been realized at temperatures below 200°C, though the device performance is usually compromised due to lower charge carrier mobility. Organic semiconductors are extremely promising new materials with the advantage of low-cost and easy integration with plastic substrates [3]. However, since these materials oxidize in air, the device stability needs to be improved before their potential wide use.

In a different approach, polymers are introduced *after* all the high-temperature fabrication steps have been completed (ex., post-IC or post-CMOS process). The aim is to gain mechanical flexibility without compromising high device performance. One route is to fabricate separate silicon islands containing conventional integrated circuits [4] [5]. These islands are typically 200-300µm thick. They are mechanically connected to each other by a flexible polymer film, which undertakes most of the stress when the entire structure is bent. In another interesting work, flexible CMOS structures were realized by printing doped single-crystalline silicon nanoribbons onto polymer layers [6]. Our organization has developed a substrate transfer technology, named CIRCONFLEX, in which RF circuits fabricated on SOI wafers were transferred onto ultra-thin polyimide films. The functionality of the circuits after the transfer and while bended has been demonstrated [7] [8].

This work presents an extension of the CIRCONFLEX process to integrate circuits fabricated at high temperatures onto parylene substrates. We are interested in parylene because it is a particularly attractive material for biomedical applications. The biocompatibility of parylene has been proven (UPS Class VI, highest grade for plastics in the United States), and it has been FDA approved for chronic human implantation. Its pin-hole free deposition and low water permeability offer excellent protection of the electronic circuits against the aggressive fluidic *in vivo* environment.

While parylene is already widely used as dielectric coating for electronic devices, its advantageous properties could be further exploited if it is used also as a highly flexible supporting substrate. Parylene-based microelectrode arrays, which involve direct deposition of metals on parylene, are already being used in retinal prosthesis [9]. We believe that the further integration of more complex elements on parylene substrates would provide interesting opportunities, particularly in biomedical applications. For example, in long-term neural recording and stimulation, multiplexers and pre-amplifiers can be fabricated on the same implantable flexible substrate with the electrodes. The vicinity of amplifiers to recording sites could significantly enhance the signal to noise ratio; while the on-chip multiplexer could greatly reduce the number of transmission lines needed in the interconnect cable.

The integration of such complex circuits on parylene faces similar challenges as other plastic substrates: the process temperature needs to be kept low in order to prevent parylene degradation; high-level stress is easily introduced due to the difference in thermal expansion coefficients between parylene and the inorganic layers. In the substrate transfer method we have investigated, the circuits were first

Manuscript received April 23, 2009. Author KW is supported by TOK Marie Curie grant from the European Commission (contract number: MTKD-CT-2006-042442). Author MD acknowledges support from the European Information Society Technologies (IST) Integrated Project *Neuroprobes* of the 6th Framework Program (FP6) of the European Commission (project number: IST-027017).

K. Wang is with Minimally Invasive Healthcare Department, Philips Research, Eindhoven, The Netherlands (phone: +31 40 27 48501; fax: +31 40 27 46321; e-mail: ke.wang@philips.com).

M. v. Deurzen and N. Kooyman are with Thin Film Facilities Department, Philips Research, Eindhoven, The Netherlands.

M. M. J. Decré is with Minimally Invasive Healthcare Department, Philips Research, Eindhoven, The Netherlands.

fabricated on standard silicon substrates using conventional processes including high-temperature steps. Parylene was then deposited at room temperature, and the substrate was glued onto a glass carrier. After the removal of the silicon substrate, processing could continue (ex. second parylene deposition, bond pad opening) before the devices were released from the glass carrier. As a proof of concept, a simple metal microelectrode array with high-temperature oxide passivation layers was transferred onto parylene. The cross-sectional structure is illustrated in Fig. 1. A metal layer is sandwiched between two layers of oxide and parylene. The layer thicknesses are symmetric on each side in order to balance the stress in the critical (metal) layer.

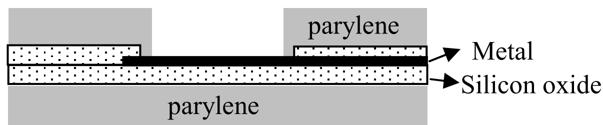

Fig. 1. Cross-sectional structure of the parylene-based microelectrodes with oxide passivation (not to scale).

II. FABRICATION PROCESS

Parylene-based microelectrodes with high-temperature oxide passivation layers were fabricated as shown in Fig. 2. The process started with 6” <100> silicon wafers. A thermal oxide layer was first grown, followed by a Ti/Pt/Ti metal stack which was sputtered and patterned with ion beam etching. A second oxide layer was deposited at 400°C by plasma-enhanced chemical vapor deposition (PECVD).

Parylene-C was then deposited (Special Coating Systems, U.S.) on the front side of the wafer, while the back was protected with a foil. A primer (AP3000) was spun on the wafer before parylene deposition to promote the adhesion. Then photoresist was spun on the parylene surface. The resist was baked at 90°C and exposed under UV before a 500nm-thick aluminium layer was sputtered on top. A ring mask was used during the aluminium deposition, so that no aluminium was deposited at the edge of the wafer.

The wafer was bonded top-down onto a glass wafer. An adhesion promoter was applied and a home-mixed glue was dispensed. The glass wafer was placed and pressed. Care was taken to avoid air bubble formation since they would cause defects after silicon removal. The glue was cured by UV exposure. The final thickness of the glue was between 10 and 20 µm. The silicon substrate was removed by first grinding down to less than 100µm, followed by etching in 30% KOH bath at 70°C. The thermal oxide layer served as an etch stop.

The thermal oxide layer was then patterned by plasma etching to open the electrode and contact pad sites. Titanium at these sites was also removed by plasma etching so that the platinum underneath was exposed as the electrode material. The wafer was again primed with AP3000 and a second parylene-C film was deposited. The parylene film was patterned by O_2/CF_4 plasma reactive ion etching (RIE), using a thick photoresist (AZ9260, Clariant, US) layer as etch mask.

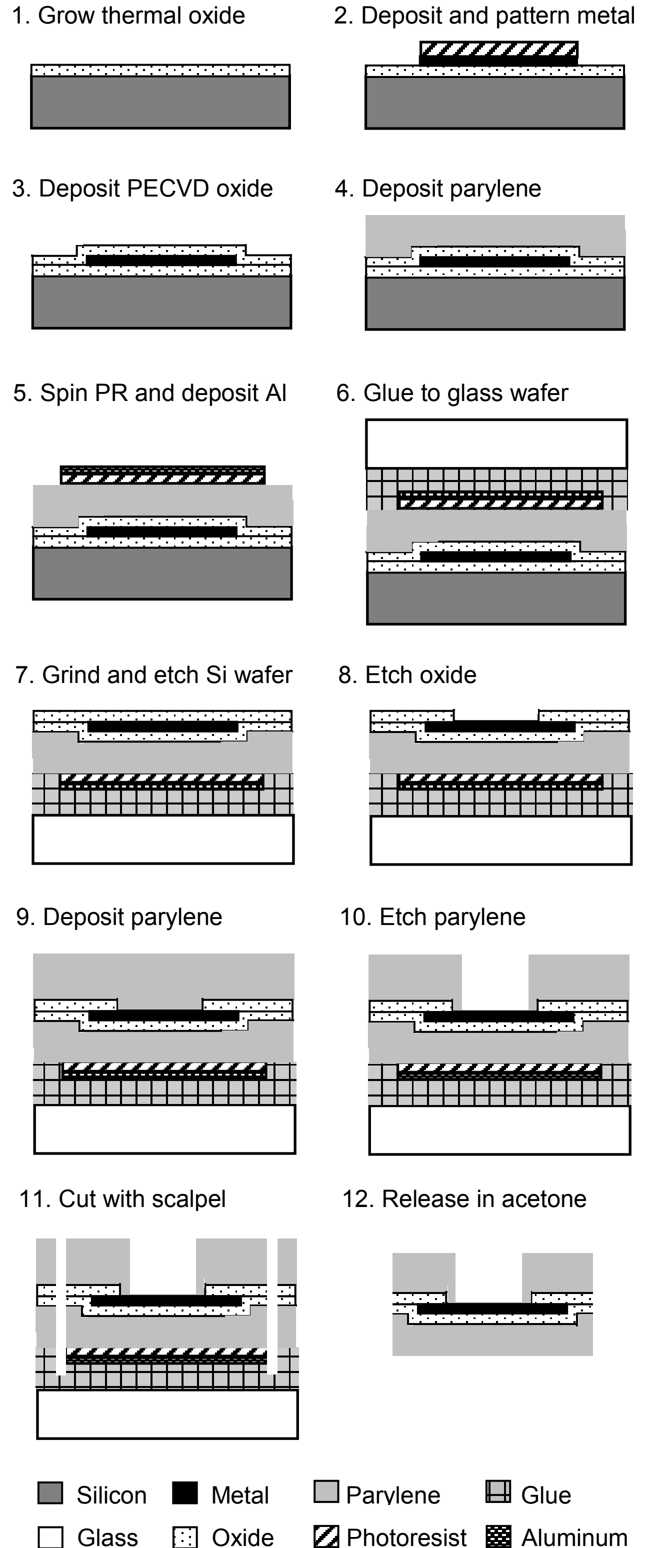

Fig. 2. Fabrication process for parylene-based microelectrodes with high-temperature oxide passivation.

Cuts were made with scalpel and the wafer was soaked in acetone overnight. The sacrificial resist layer dissolved and

the devices were released from the glass carrier. The parylene-based microelectrode arrays and test structures after releasing are shown in Fig. 3.

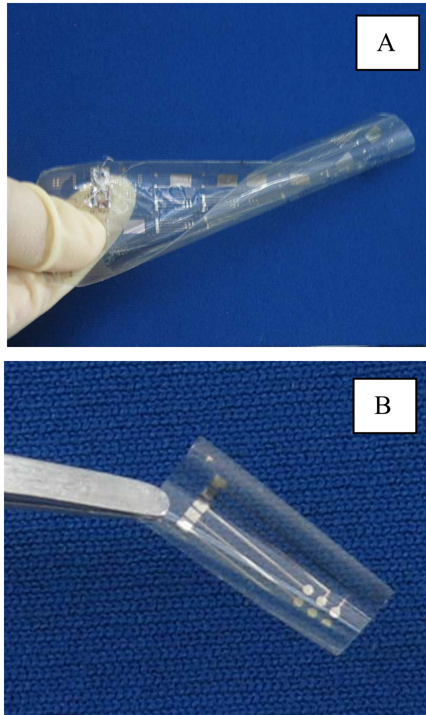

Fig. 3. (A) A stripe of 20µm-thick parylene film with test structures consisting of metal, thermal oxide and high temperature PECVD oxide layers. (B) A parylene-based oxide-passivated microelectrode array.

III. DISCUSSION

A. Parylene Etching

Parylene was etched using oxygen-based plasma RIE (Reactive Ion Etching). Conventionally, standard photo resists of a few microns thick are used to mask parylene etching in oxygen-based plasma. Although the etch selectivity is marginal, it is acceptable for many applications in which parylene is used as a thin coating layer. However, parylene serves as the substrate which gives mechanical support in this work. Its thickness (>10 µm) is significantly greater than what is commonly used. Therefore, standard photo resists are not sufficient to mask the etching.

Initial effects were focused on finding a hard etch mask. Several groups have reported using PECVD silicon oxide and nitride as etch masks for parylene [10][11]. Typical deposition temperatures are between 300-400°C. Although parylene has been reported to have thermal stability at as high as 270°C in air and 450°C in nitrogen [12], we avoided such high temperature steps to prevent undesired changes in parylene properties such as oxidation and crystallization, as well as to minimize thermal stress between different layers. Silicon oxide and nitride can also be deposited at lower temperatures with PECVD. However, the resulting films are highly porous and cannot be used as etch masks.

Among different metals, aluminium and chromium were chosen to be tested because of their low deposition temperature, as well as the easy, clean and less hazardous removal. However, evaporated or sputtered chromium on parylene cracked, presumably due to high intrinsic stress. The deposition of aluminium onto parylene was acceptable. However, aluminium was sputtered during the reactive ion etching of parylene. Re-deposited aluminium formed micro-masks on the parylene surface and resulted in parylene "grass" after etching (Fig. 4).

Satisfactory results were achieved using a thick film photoresist AZ® 9260 as etch mask (Fig. 5). The resist reached a thickness of over 12µm with one spin, sufficient to mask the etching of 10µm thick parylene film. Features smaller than 5µm could be resolved.

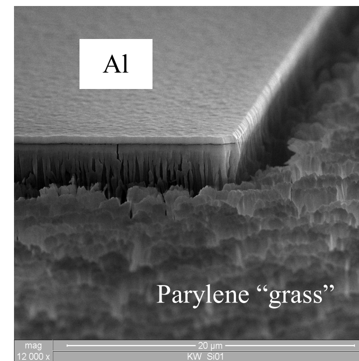

Fig. 4. Parylene after etching, using aluminum as etch mask. Re-deposited aluminium formed micro-masks on parylene surface and resulted in parylene "grass" after etching.

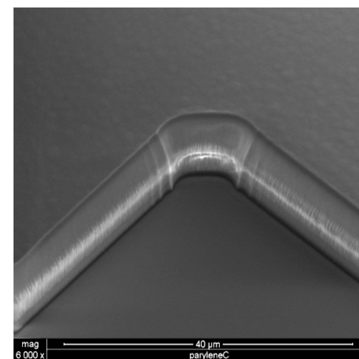

Fig. 5. Micro-patterned 10µm thick parylene layer using photoresist AZ9260 as etch mask.

B. Bond Pad Opening

Two paths seemed to exist for opening the bond pads and electrode sites: they could either be opened before the bonding onto glass (i.e., patterning the first parylene layer and the PECVD oxide layer in the example structure), or they could be opened after the silicon wafer has been removed (i.e., patterning the second parylene layer and the thermal oxide layer). The first path (named as "front side opening") initially seemed favorable, since it would involve minimal post-transfer processing and minimal interference with the critical device layer in the case a more complex structure (such as CMOS) was to be transferred.

However, while pursuing the "front side opening" approach, the device layer was severely damaged after silicon removal in KOH. It seemed that stress built up at the edges of electrode sites and contact pads (where large topography was created after parylene etching) during the bonding and silicon removal processes. Once the supporting silicon substrate was completely removed in KOH, the brittle oxide layers failed under such high stress. Some possible origins for this topography-related stress include glue shrinkage during UV curing, defects, thermal expansion mismatch and residual stress.

The "back side opening" path circumvented this topography-stress problem. However, if more complex structures such as CMOS circuits are to be transferred, the layout should be designed so that the bond pads could be reached from the back side without disrupting the device layers. Alternatively, the "front side opening" path could also be more carefully investigated with attempts to minimize the stress.

C. Gluing and Releasing

The bonding between the silicon wafer and the glass wafer needs to be strong enough to endure the grinding, KOH etching and post-transfer processes; while on the other hand, the device layer needs to delaminate from the glass carrier in the end. These two requirements were fulfilled by using a multi-layer stack (photoresist/aluminium/glue).

The adhesion between parylene and the glue is strong. Therefore, a separation layer (aluminium) is needed in between so that delamination from the glue could be possible. The parylene-based device layer could then be peeled off from the glass carrier. However, this aggressive procedure introduces a lot of stress in the film and may impair the performance of more complicated devices.

A less aggressive releasing method is by dissolving the aluminium layer in its etchant (H_3PO_4/HNO_3/HAc). The drawback is that the process is time consuming due to the low etch rate. For stress-free and faster releasing, a sacrificial photoresist layer was added and the device layer delaminated after acetone soak. The aluminium layer was still needed to protect the resist from the glue.

IV. Conclusion

We have demonstrated a process which transfers device layers from silicon wafers onto parylene. Unlike existing techniques which directly deposit layers on parylene [9], the devices are fully processed using conventional fabrication conditions *prior to* their integration with parylene. This substrate transfer technology could enable the use of high quality films (e.g. single-crystalline silicon, LPCVD silicon nitride) in parylene-based devices, thus contributes towards the realization of truly flexible, biocompatible integrated circuits. Current research is focused on investigating the integrity and functionality of the parylene-based circuits after the transfer process and under mechanical stress.

Acknowledgment

The authors benefited from insightful discussions with Ronald Dekker and Piet Bouten. We would like to thank Pascal de Graaf for help with parylene deposition, and Theo Michielsen for the bonding process.

References

[1] H. Gleskova, S. Wagner, W. Soboyejo, Z. Suo, "Electrical response of amorphous silicon thin-film transistors under mechanical strain", *Journal of Applied Physics*, Vol. 92, No. 10, pp. 6224–6229, 2002.

[2] S. D. Theiss, P. G. Carey, P.M. Smith, P. Wickboldt and T. W. Sigmon, "Polysilicon thin film transistors fabricated at 100°C on aflexible plastic substrate", Electron Devices Meeting, 1998, pp. 257-260, 1998.

[3] M. Muccini, "A bright future for organic field-effect transistors", Nature Materials 5, pp. 605 – 613, 2006.

[4] Yong Xu Yu-Chong Tai Huang, A. Chih-Ming Ho, "IC-integrated flexible shear-stress sensor skin", Microelectromechanical Systems, Journal of, 12 (5), pp. 740- 747, 2003.

[5] P.W. Barth, S.L. Bernard, J.B. Angell, "Flexible circuit and sensor arrays fabricated by monolithic silicon technology, *IEEE Transactions on Electron Devices,* 32 (7), pp. 1202- 1205, 1985.

[6] D. H. Kim, J. H. Ahn,W. M. Choi, H. S. Kim, T. H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, J. A. Rogers, "Stretchable and Foldable Silicon Integrated Circuits", *Science*, Vol. 320. no. 5875, pp. 507 – 511, 2008.

[7] R. Dekker, M. Dumling, J. H. Fock, O. Gourhant, C. Jonville, T. M. Michielsen, H. Pohlmann, W. Schnitt, A. M. H. Tombeur, "A 10 µm thick RF-ID tag for chip-in-paper applications", *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting,* pp. 18- 21, 2005.

[8] R. Dekker, M. Dumling, J. H. Fock, O. Gourhant, C. Jonville, R. Kubrin, T. M. Michielsen, H. Pohlmann, W. Schnitt, A. M. H. Tombeur, T. Zoumpoulidis, "CIRCONFLEX: an Ultra-Thin and Flexible Technology for RF-ID Tags", *EMPC 2005, June 12-15,* Brugge, Belgium.

[9] D. C. Rodger, A. J. Fong, W. Li, H. Ameri, A. K. Ahuja, C. Gutierrez, I. Lavrov, H. Zhong, P. R. Menon, E. Meng, J. W. Burdick, R. R. Roy, V. R. Edgerton, J. D. Weiland, M. S. Humayun, Y. C. Tai, "Flexible parylene-based multielectrode array technology for high-density neural stimulation and recording", *Sensors and Actuators B*, 132, pp. 449-460, 2008.

[10] R. D. Tacito, C. Steinbrüchel, "Fine-Line Patterning of Parylene-n by Reactive Ion Etching for Application as an Interlayer Dielectric", Journal of the Electrochemical Society, 143 (6), pp. 1974-1977, 1996.

[11] T. E. F. M. Standaert, P. J. Matsuo, X. Li, and G. S. Oehrlein, T.-M. Lu R. Gutmann, C. T. Rosenmayer, J. W. Bartz, "High-density plasma patterning of low dielectric constant polymers: A comparison between polytetrafluoroethylene, parylene-N, and poly(arylene ether)", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, 19 (2), pp. 435-446, 2001.

[12] J. Marra, Philips internal publication.