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Hafnium Transistor Process Design for Neural Interfacing

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***Abstract*—A design methodology is presented that uses 1-D process simulations of Metal Insulator Semiconductor (MIS) structures to design the threshold voltage of hafnium oxide based transistors used for neural recording. The methodology is comprised of 1-D analytical equations for threshold voltage specification, and doping profiles, and 1-D MIS Technical Computer Aided Design (TCAD) to design a process to implement a specific threshold voltage, which minimized simulation time. The process was then verified with a 2-D process/electrical TCAD simulation. Hafnium oxide films (HfO) were grown and characterized for dielectric constant and fixed oxide charge for various annealing temperatures, two important design variables in threshold voltage design.**

I. Introduction

PREVIOULY a methodology[1, 2] to predict the gain of an open gate oxide semiconductor field effect transistor structures (referred to in the literature as an OGFET (Fig. 1) or OSFET[3]) that used simple, yet accurate, 1-D analysis was presented. The insulator material of an open gate transistor has to be impervious to the sodium and potassium that the tissue cultures required to survive during the recording process.

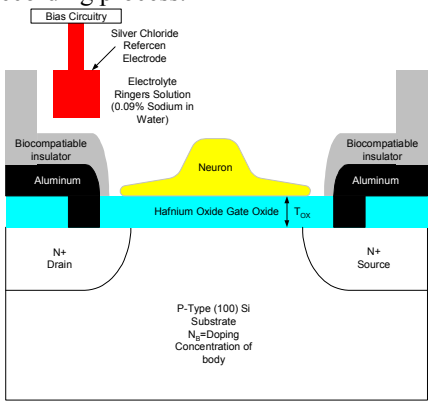

Fig. 1: Open Gate MOSFET with Hafnium Oxide as a gate dielectric, with the body of a neuron in close proximity to the open gate

A common method to increase transistor gain and protect against sodium and potassium contamination is to incorporate high-k dielectrics. Hafnium dioxide (HfO) gate dielectrics have been explored as alternative to silicon dioxide gate dielectrics for biological applications [4-6]. Here we explore the impact of using an HfO dielectric in a systematic way using a transistor design methodology. This methodology would be used once a general transistor structure has been selected using [1] and[7].

The first part of this paper briefly highlights an HfO thermal evaporation procedure and annealing results for dielectric constant and fixed oxide charge. These constants are then used to accurately design the threshold voltage of an MIS capacitor and ultimately a transistor in the second part of the paper.

The transistor process flow used is based on native transistors (no threshold voltage adjust implant step) with an aluminum gate for electrical testing. This ensures that the transistors are as low noise as possible. The process consists of only four masking steps (which keeps process time and costs low): source and drain diffusion, gate oxidation/formation, contact to source drain and substrate and metal gate interconnect formation[1].

II. Hafnium Oxide MIS results

In order to design the threshold voltage of a hafnium oxide based transistor, the fixed oxide charge (Q_{ss}) and relative dielectric constant (ϵ_{ox}) need to be determined. Hafnium oxide was deposited by thermal evaporation[8] on chemically clean (100) p-type silicon substrates and was annealed at 450°C, 700°C and 900°C in N_2 gas for 30 minutes. The dielectric constant was found via the capacitance voltage method using MDC's analysis software and mercury probe (www.mdc.com). The thickness required for this analysis was measured with the Filmetrics optical reflectance tool. The films were destroyed by the 900°C anneal; thus, they were not characterized. Fig. 2 shows that the maximum was achieved for a 30 minute 700°C anneal, and Fig 3 shows the CV repose of the 600A thick film producing a Q_{ss} of $5x10^{11}q/cm^2$. These values were then used to design the threshold voltage of the transistor.

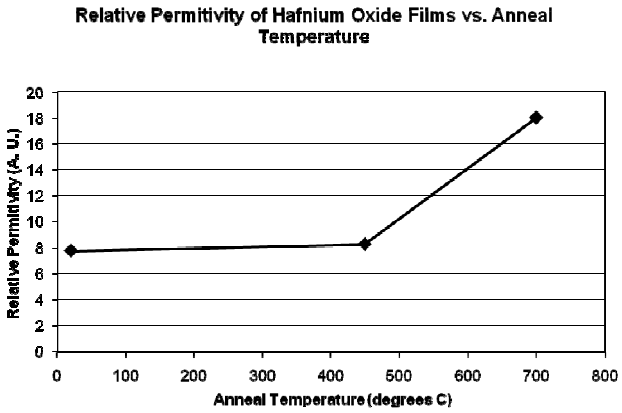

Fig. 2: 600 Å hafnium oxide film on (100) silicon substrate annealed at 450°C, and 700°C for 30 minutes. Maximum ϵ_{ox} achieved was 18.

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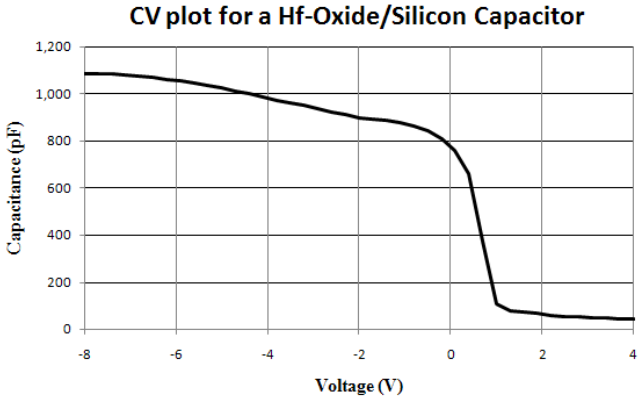

Fig. 3: CV plot for 600 Å film on (100) silicon substrate. Extracted Q_{ss} was $5x10^{11}q/cm^2$.

III. Design Flow for Process Design of Transistors used as Common Source Amplifiers

Once estimates for ϵ_{ox} and Q_{ss} were found, the first step in designing a transistor process was to select the oxide thickness (T_{ox}) substrate doping (N_b) pair for a given threshold voltage specification. The threshold voltage for an MIS capacitor is given by[9]:

$$V_T = \Phi_{ms} - \left(\frac{Q_{ss}+Q_D}{C_{ox}}\right) + 2\Phi_F \,. \quad (1)$$

Where Φ_{ms} is the metal semiconductor work function, and the Aluminum/Silicon system is given by:

$$\Phi_{ms} = -0.554V - U_T \ln\frac{N_b}{n_i} \,. \quad (2)$$

Where $n_i$is the intrinsic carrier density ($1.5x10^{10}cm^{-3}$ at 300K), and U_T is the dynamical thermal voltage, which is given by:

$$U_T = \frac{kT}{q} \quad (3)$$

T is temperature in Kelvin, and k is the Boltzmann constant ($1.38066x10^{-23}J/K$). The charge of an electron (q) is $1.6x10^{-19}C$. Cox is the gate oxide capacitance due to the dielectric and depends on the relative permittivity of the oxide and the thickness of the oxide:

$$C_{ox} = \frac{\epsilon_0\epsilon_{ox}}{T_{ox}}. \quad (4)$$

ϵ_0 is the permittivity of a vacuum ($8.85x10^{-14}F/cm$) and ϵ_{ox} is the relative permittivity of the oxide layer. ϵ_{ox} is 3.9 for silicon dioxide, and 18 for hafnium oxide.

Q_{ss} is the fixed oxide charge due to defects in the oxide. The value of Q_{ss} depends on the growth conditions of the oxide. For silicon (100) oriented substrates with $Si0_2$ or Hf-Oxide, insulators can vary between $\sim10^{10}q/cm^2$ to $10^{12}q/cm^2$. Q_D is the charge in the depletion region under strong inversion and is given by:

$$Q_D = -2\sqrt{\epsilon_0\epsilon_{Si}qN_b\Phi_F}. \quad (5)$$

ϵ_{Si} is the relative permittivity of the silicon with a value of 11.7. Φ_F is the Fermi level and represents the doping of the substrate is and energy band diagram, which is given by:

$$\Phi_F = U_T \ln\frac{N_b}{n_i} \,. \quad (6)$$

Using equations 1-6, a hafnium oxide thickness (T_{ox}) of 620Å and a substrate doping (N_b) of $2.1x10^{17}cm^{-3}$ produced a threshold voltage of 0.5Volts for a Q_{ss} of $5x10^{11}cm^2$.

The next step was to use an electrical TCAD simulation to verify that a hafnium oxide thickness (T_{ox}) of 620Å, substrate doping (N_b) of $2.1x10^{17}cm^{-3}$, ϵ_{ox} =18, and $Qss=5x10^{11}q/cm^2$ will produce a threshold voltage of 0.5Volts. To this end, a 1-D simulation environment was created to draw the dimensions of the structure, adjust the grid spacing, perform an electrical simulation, and extract threshold voltage. Fig. 4 shows a MIS structure with a T_{ox} of 2000Å, with a grid spacing of 0.85um to illustrate the dimensions properly. Fig 5 shows the capacitance voltage response of the target MIS structure properties of T_{ox}= 620Å, N_b =$2.1x10^{17}cm^{-3}$, ϵ_{ox} =18, and $Qss=5x10^{11}q/cm^2$. The inversion region can be seen around 0.5 volts. A grid sensitivity analysis was performed to find the optimum grid spacing (0.01um) by reducing the grid spacing until the extracted threshold voltage converged. The capacitance-voltage (CV) extraction methodology can be requested from www.mdc.com. The extracted threshold voltage was 0.5095V which is less than one U_T (26mV at 300K) from the value predicted from equations (1)-(6) of 0.508V. The difference of 1.5mV can be explained by the fact that the depletion width and thus, the depletion capacitance are approximated. Another important use of this 'as drawn' simulation environment is that the simulation and extraction methodology is verified. The approximate CPU time to draw and simulate the structure was 1 minute.

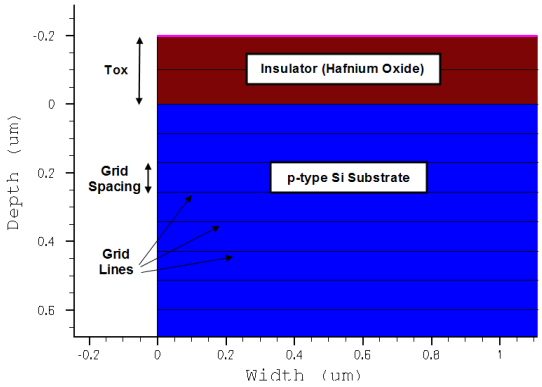

Fig. 4: Structure used to verify 'as dawn' MIS capacitors. Grid Spacing 0.085um, T_{ox}=0.2um (T_{ox} set larger than specification for clarity), $N_b=2.1x10^{17}cm^{-3}$. The simulator automatically invokes 1-D drift and diffusion simulation at each grid line. The aluminum top and bottom contacts are invoked at the top and bottom interfaces of the structure. V_T=2.59V, for $Q_{ss}=5x10^{11}q/cm^2$, ϵ_{ox}=18.

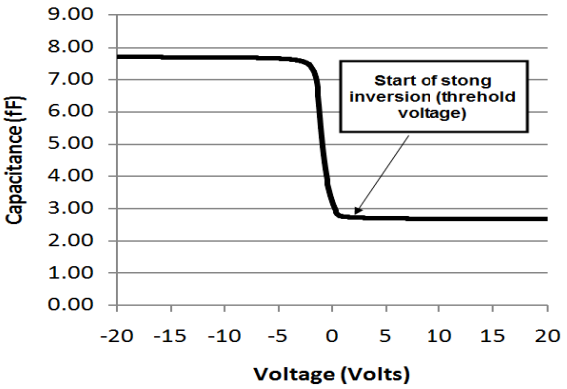

Fig. 5: Capacitance Voltage Plot Hafnium Oxide MIS structure for Grid Spacing 0.01um, T_{ox}=0.062um, N_b=2.1x10^{17}cm^{-3}, Q_{ss}=5x10^{11}q/cm^2, ϵ_{ox}=18, Extracted V_T=0.5095 Volts. The area of the structure was 3x10^{-8}cm^2.

Once the oxide thickness and substrate doping targets are verified, the next step is to develop a process to set the substrate doping. (One cannot purchase arbitrarily doped substrates.) The substrate doping is achieved by implanting a lowly doped p-type substrate with a high concentration of boron (Fig. 6), and then performing a high temperature diffusion step (drive in) to bring the substrate concentration to the correct level (Fig. 6). The implant process variables are energy (how far the ions go into the substrate) and dose (how many ions are implanted, given as Q). The energy is set to 100kV so that 90% of the ions pass through a screening oxide and are implanted into the substrate. The drive in process variables are time and temperature, which create a Gaussian distribution of boron dopant. (The Gaussian dopant distribution after the well drive step, is not apparent due to the choice of maximum displayed depth of 2µm.) Given that the depletion width is small compared to the Gaussian doping profile, it can be assumed that the surface concentration (N_c) of the boron will be equal to the substrate doping concentration (N_b), the drive in time (τ_{WD}), and temperature (T_{WD} in K). The dose can be used to design the substrate doping [10]:

$$N_b \cong N_S = \frac{Q}{\sqrt{\pi D_{WD}\tau_{WD}}} \qquad (7)$$

where D_{WD} is the diffusion of constant of boron, which is given by:

$$D_{WD} = 0.77 \times e^{-\frac{3.46eVq}{kT_{WD}}} \qquad (8)$$

A Sentaurus process run deck consisting of the implant, drive in, filed oxidation and hafnium oxide deposition steps was used to verify equations (7) and (8). The implant energy dose of 100kV and 3.4x10^{14} ions/cm^2 respectively along with a drive time of 1440 minutes and temperature of 1150^{o}C with a field oxidation temperature/time of 1100^{o}C/60 minutes gave an extracted N_b of 8.24x10^{17}cm^{-3} (no boron segregation) using equations (7) and (8) and an extracted substrate doping (with boron segregation[11]) of 2.12x10^{17}cm^{-3} with a V_T=.56V using the TCAD run deck. Boron segregation (Fig. 6) can be modeled by reducing the result from equation (7) from 0.2 to 0.5 of the pre-oxidation surface concentration. The Sentaurus tools uses the models presented in [12, 13] to take into account Boron segregation and oxide enhanced diffusion. The approximate CPU time to simulate the process and electrical response of the structure was 5minutes.

Fig. 7 shows the resulting MIS structure for the process. The boron depletion can be seen to extend approximately 0.4um from the oxide.

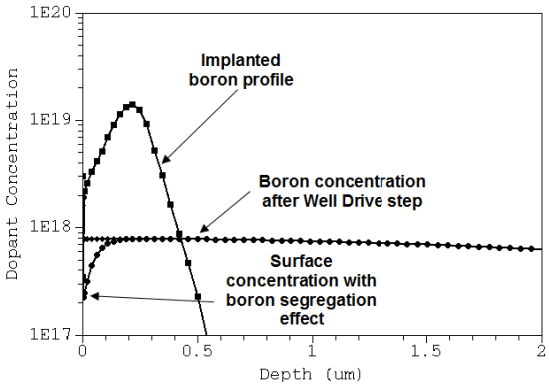

Fig. 6: Three boron doping profiles (atoms/cm-3) showing an implant with E=100kV, Q=3x10^{14} ions/cm^2, a well drive of 1150^{o}C, for 1440 minutes, and a depleted surface due to born segregation caused by oxidation step. Left to right depth is the same as the top down depth of Fig. 4 and Fig. 7.

Given that transistors can exhibit short channel effects, which reduce the threshold voltage, a full 2-D process run deck was used to verify the process recipe rather than a 1-D MIS simulation. The simulated process consisted of a boron implant (E=100kV, Q=3x10^{14}ions/cm^2), Well Drive (1150^{o}C, 1440 minutes), Field oxidation (wet 1100^{o}C, 60 minutes), Source/Drain Diffusion (1100^{o}C, 60 minutes), and a 620Å hafnium oxidation deposition/annealing step. Fig. 8 shows the results of a 2-D process simulation using the Sentaurus sprocess tool. The simulation for the process to 'grow' the transistor is approximately 30 minutes.

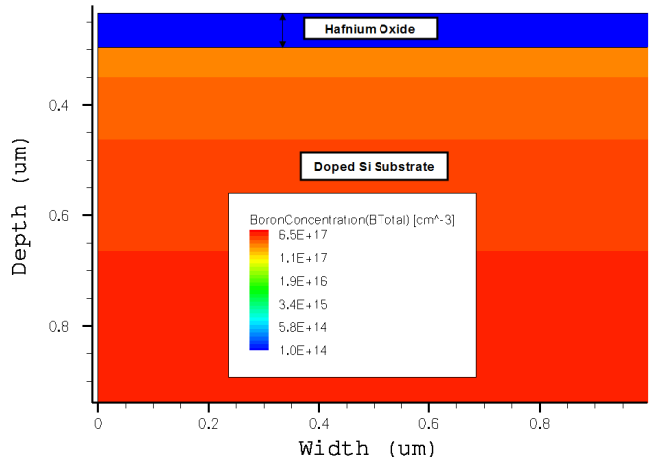

Fig. 7: Structure used to verify implant and well drive process. Grid Spacing 0.045um, T_{ox}=0.062um, N_b extracted =2.12x10^{17}cm^{-3}. V_T extracted was 0.56V, for Q_{ss}=5x10^{11}q/cm^2, ϵ_{ox}=18.

The electrical results can be seen in Fig. 9. The extracted V_T for the 2-D simulation was 0.512V for T_{ox} of 550Å. This is

in good agreement with 1-D simulation. The implication of this is that the T_{ox} and N_b can be explored at 5 minutes a simulation and then verified for a single 20 minute simulation.

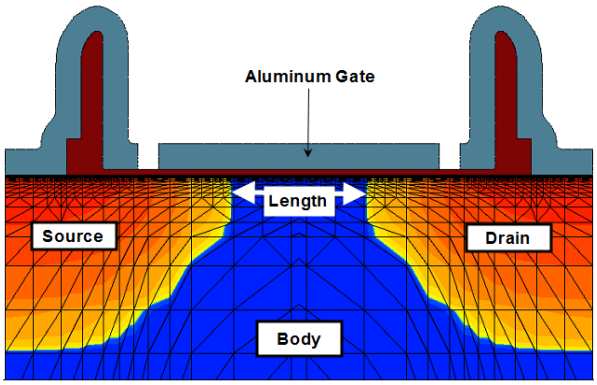

Fig. 8: 2-D process simulation of Hafnium oxide based transistor. (E=100kV, Q=3x10^{14}ions/cm^2), Well Drive (1150^{o}C, 1440minutes), Field oxidation (wet 1100^{o}C, 60 minutes), Source/Drain Diffusion (1100^{o}C, 60 minutes), and a 620 Å hafnium oxidation deposition/annealing step. The extracted V_T from a 2-D current voltage simulation was 0.587volts. A 550Å T_{ox} gave a V_T of 0.512V. The actual length was shortened in the figure to improve clarity.

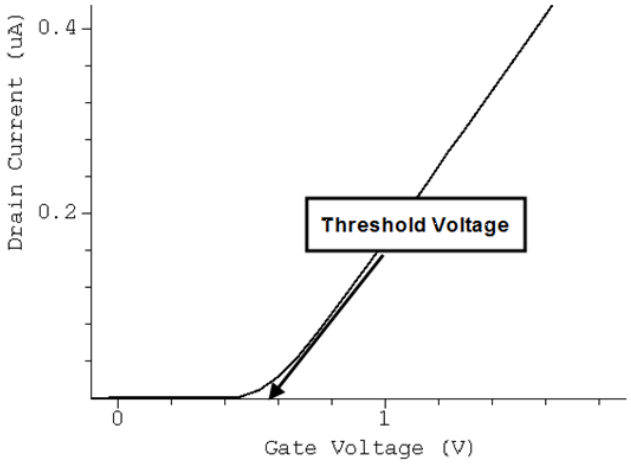

Fig. 9: 2-D electrical simulation of a hafnium oxide based transistor. (E=100kV, Q=3x10^{14}ions/cm^2), Well Drive (1150^{o}C, 1440 minutes), Field oxidation (wet 1100^{o}C, 60 minutes), Source/Drain Diffusion (1100^{o}C, 60 minutes), and a 620Å hafnium oxidation deposition/annealing step. The extracted V_T from a 2-D current voltage simulation was 0.587volts. A 550Å T_{ox} gave a V_T of 0.512V.

IV. Conclusions

A design flow was developed to rapidly explore the design space for a HfO based transistor by using quick 1-D process simulations to narrow the range of structure parameters, and then verify the process recipe with a single long 2-D process simulation. Hg probe CV results for thermally evaporated HfO films were used to increase the accuracy of the design. Future work will include fabricating the transistors, and testing these in open gate configuration. The run decks for the process and electrical simulations can be found [14].

Acknowledgment

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