A LabVIEW™ Based Multichannel Recording Architecture for High Density Electrical Mapping

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Abstract

The goal of our work is to describe and test a novel multichannel recording equipment architecture for cardiac mapping based on LabVIEW: the Reconfigurable Architecture for Electrical Mapping (RAEM).

The RAEM architecture covers the communication between a generic acquisition hardware and a computer by means of a FPGA and a Real-Time Controller. Evaluation of the performance, versatility and limitations of the presented architecture has been done by using three different National Instruments (NI) hardware solutions (Single-BoardRIO-9631, Single-BoardRIO-9642 and the CompactRIO-9024+CompactRIO-9104). Maximum data throughput obtained for each hardware solution were: 19, 24 and 51 Mbps.

The design of the RAEM system, based on LabVIEW and RIO hardware, allows migration to new hardware platforms keeping the same architecture.

1. Introduction

The term cardiac mapping refers to any equipment or experiment that records and analyzes cardiac electrical waveforms from several exploring electrodes. These systems can be used for endocardial, epicardial or body surface electrical mapping [1].

The analysis of activation patterns of the heart by cardiac mapping has greatly contributed to the knowledge about arrhythmia mechanisms; in fact fibrillatory conduction behaviors such as re-entries, focal activity, etc. could not be described without the help of cardiac mapping techniques. Since 1941, when Harris used the technology available at the time to record simultaneously from three electrodes using three string galvanometers [2], more than 100 studies have been published in which electrical mapping of atrial or ventricular activation was performed. During this time the knowledge on the fibrillation process has grown together with the number of recording channels [1]: between the 70s and 90s, systems grew from 30 to 300 electrodes. If this increase in the number of recording channels had followed the same trend, current mapping systems would employ up to 30.000 electrodes. However, the maximum number of recorded channels in the literature is 1700. A larger number of electrodes with smaller interelectrode distances sampled at higher rates may help in understanding observed phenomena such as rotors, electrotonic propagation, etc [3].

There are several reasons why the increase in the number of channels has been decelerated: 1) the lack of novel analysis methods for such amount of data, which require automatic analysis software and 2) the non-existence of standard hardware architectures that allowed a continuous increase in equipment characteristics. Our and other groups have been working from years in the development of novel signal processing techniques to overcome the first limitation [3-4]. However, little work has been done in order to overcome the standardization of multichannel recording equipment.

A multichannel recording system, such as a cardiac mapping equipment, can be divided in two main blocks: 1) the analog block which involves electrodes, amplifiers and filters that provides signals to the analog to digital converters (ADC) and 2) the digital block which involves digitalization, communication, storage and other control tasks. Several works have evaluated different architectures for the analog block [5], however there is very little achieved so far in the development of versatile and standardized architectures for the digital block.

The goal of our work is to describe and test a novel multichannel architecture for the digital block based on LabVIEW [6]: the Reconfigurable Architecture for Electrical Mapping (RAEM). The main characteristic of the RAEM is that its design is independent of the hardware platform, consequently it will be able to increase its features (i.e. number of channels, sample rate, etc.) together with National Instruments (NI) hardware keeping the same architecture.

In this work the RAEM will be presented and tested under different NI hardware solutions in order to demonstrate its versatility. Additionally the maximum data throughput will be evaluated for each NI hardware solution.

2. Methods

In this section, the proposed architecture for the digital control of a multichannel recording equipment is described: the RAEM. This architecture covers the communication between a generic analog block and a generic personal computer (PC) by means of a high-performance Field Programmable Gate Array (FPGA) and a Real-Time Controller (RTC) (Fig. 1). The RAEM solution has been tested under different NI hardware solutions in order to corroborate its versatility. The maximum data throughput, which is the product of number of channels, sampling rate and ADC resolution, is evaluated.

2.1. Reconfigurable architecture for electrical mapping

A schematic representation of the RAEM architecture is depicted in Fig. 1. The first step of the RAEM system is the temporal storage of a certain number of samples acquired from the analog block in a temporal memory installed in the FPGA. A solution for this task has been programmed using the LabVIEW FPGA Module by means of a state machine that implements the Serial Peripheral Interface (SPI) protocol and stores the data resulting from the communication with the ADCs into a Direct Memory Access First Input, First Output (DMA-FIFO). One of the main tasks of this state machine is to generate clock and control signals for the ADCs, and so a high clock rate is needed. This is not a limitation since the minimum default operation rate of any NI FPGA platform is 40MHz, much higher than the clock rate necessary to perform the analog to digital conversion of bioelectrical signals, fulfilling the Nyquist criterion. The second task of the FPGA is the temporal storage of the data into the DMA-FIFO memory. Since any electrical mapping system should work in real time, the size of this memory will influence the maximum data throughput of the architecture. In this work, we perform a detailed analysis of the relation between the size of the temporal memory and the maximum data throughput of the architecture.

The second step of the RAEM system involves sending the data stored in the temporal memory to a PC. A solution for this task has been programmed on the RTC using the LabVIEW Real-Time Module. RTC works in parallel with the FPGA and is responsible for acquiring the data stored in the DMA-FIFO memory of the FPGA via a peripheral component interconnect (PCI) bus. Once the data from memory are collected, they are packaged via Transmission Control Protocol (TCP) and sent to the PC. This operation is performed under master-slave programming structure: the master deployed on a Real-Time Loop has a deterministic behavior, reading from the DMA-FIFO located in the FPGA with a given cadence. Time between readouts, or Data Readout Period (DRP), determines the period of operation of the RTC. The amount of data demanded to the DMA-FIFO (e.g. Data Segment) is given by the amount of data obtained by the ADC converters during an DRP. This number depends of the sampling rate, the number of channels, the bits per sample and the DRP. The data obtained is fed into a data queue that communicates with the slave. The slave packages the data available from the queue in TCP and sends it to the PC. The slave only is executed when there are elements available in the queue, freeing the processor while waiting for data.

The third step of the RAEM system involves reassembling the information collected from the RTC in order to store and represent it into the PC. This has been programmed in the PC with a structure similar to that of the RTC but, in this case there are two slaves instead of one. The master is responsible for acquiring the data via TCP/IP and the two slaves are responsible for the representation and data storage respectively. Both slaves acquire information through queues, similar to that of the RTC slave.

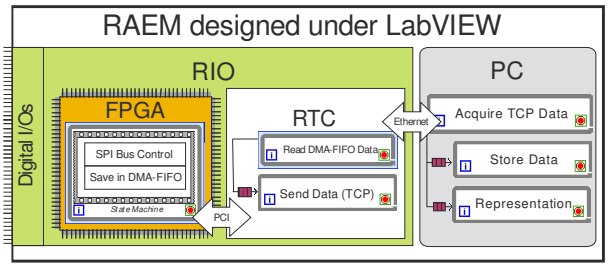

Figure 1. Schematic representation of the Reconfigurable Architecture for Electrical Mapping (RAEM).

2.2. Experimental setup

In order to evaluate the performance and versatility of the presented architecture, three different NI hardware solutions were used (table 1). Impact on the maximum throughput of different RAEM configurations was evaluated separatedly.

Effects of the size of the temporal memory on the FPGA for varying DRP lengths were analyzed by comparing the maximum data throughput obtained using three different DMA-FIFO memory sizes: 32, 64 and 128 kBytes and the same RTC: sbRIO9642 (400MHz, 128 MB RAM).

Impact of the RTC used on the maximum data throughput was analyzed for varying DRP lengths and using three different RTCs: sbRIO9631 (266MHz, 64MB RAM), sbRIO9642 (400MHz, 128MB RAM) and cRIO9024 (800MHz, 512MB RAM) and the same DMA-FIFO memory: 64 kBytes.

Finally, the DRP which results in maximum data throughputs was obtained for each NI hardware platforms at their maximum operating rate and FIFO sizes.

Table 1. Characteristics of National Instruments Hardware Solutions

	sbRIO-9631	sbRIO-9642	cRIO-9024 +cRIO-9104.
Maximum FIFO size	64 kB	128kB	256kB
RTC Performance	266 MHz 64MB RAM	400MHz 128MB RAM	800MHz 512MB RAM

3. Results

3.1. Analysis of the temporal memory

In Fig. 2 the analysis of the effects of different sizes of the DMA-FIFO memory are depicted. As it can be observed, for DRPs shorter than 6 ms, the maximum data throughput was similar for all memory sizes and depended only on the DRP. However, for DRPs longer than 6 ms data throughput depended greatly on memory size, achieving greater data throughputs when working with larger DMA-FIFOs (i.e. 20, 22 and 24 Mbits/s for the 32, 64 and 128 KBytes DMA-FIFOs respectively). Data Segments used were also dependent on the DRP size: for DRPs shorter than 6 ms, the size of the Data Segments was independent of the DMA-FIFO size, whereas for DRPs longer than 80 ms, the size of the Data Segments was limited by the DMA-FIFO size independently of the DRP. The presented analysis showed that the size of the temporal memory used in the RAEM architecture was a critical factor for long Data Readout Periods.

3.2. Analysis of the real-time controller

In Fig. 3 the analysis of the effects of different RTCs using an specific DMA-FIFO memory size is depicted. As it can be inferred, for DRPs longer than 30ms the data throghput is independent of the RTC, this is due to the limitations introduced by 64kbytes DMA-FIFO (see 3.1). However, for DRPs shorter than 30ms the data throughput depends on the RTC processor capability, achieving better results for the RTCs with higher performances (i.e. 19, 22 and 47 Mbps for the sbRIO9631, sbRIO9642 and cRIO9024 respectively). RTC usage was evaluated for varying RTC times. Notice that when the data throughput depends on the platform the RTC usage was close to 100%.

The presented analysis showed that the operation rate of the RTC used in the RAEM architecture was a critical factor for short Data Readout Periods.

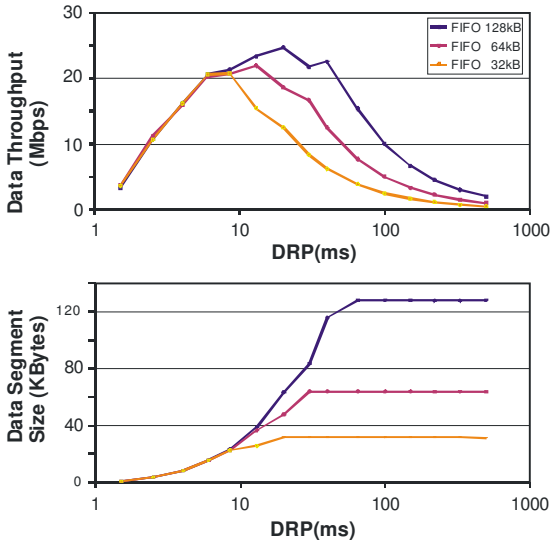

Figure 2. Data throughput and data segment size against DRP length for three different FIFO sizes.

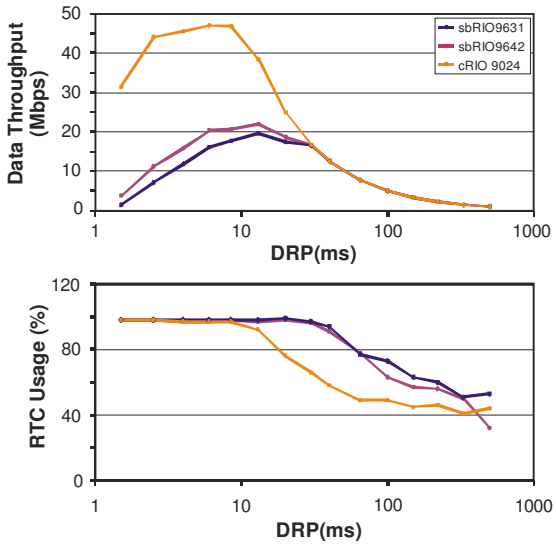

Figure 3. Data throughput and RTC usages against DRP length for three different hardware solutions.

3.3. Performance of the reconfigurable architecture for electrical mapping

In Fig. 4 maximum data throughput as a function of the DRP for each one of the three used NI hardware solutions is depicted. As it can be observed, the maximum data throughput presented a Rayleigh distribution in which the short tail is dependent on the operation rate of the RTC, whereas long tail is dependent on the temporal memory size of the FPGA.

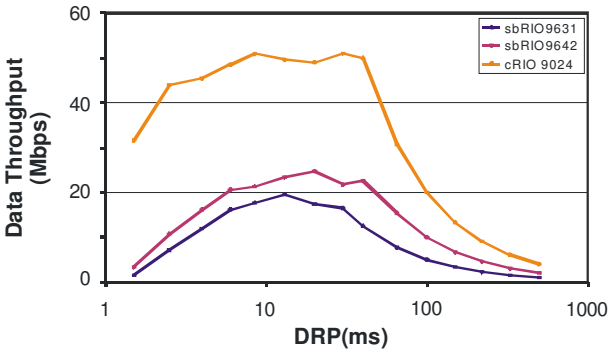

Figure 4. Maximum data throughput obtained for each one of the three NI hardware solutions according to the Data Readout Period (DRP). Notice that in each case the largest temporal memory size was used (table 1).

Optimal transfer characteristics for each of the hardware solutions are summarized in table 2. The maximum data throughput of the CompactRIO system (cRIO 9024+cRIO 9104) would allow data transmission from 3340 channels at a sampling frequency of 1 kHz with 16-bit resolution.

Table 2. Optimal Implementation Characteristics for the National Instruments Hardware Solutions

	sbRIO-9631	sbRIO-9642	cRIO-9024 +cRIO-9104.
Maximum Throughput	19 Mbps	24 Mbps	51 Mbps
Optimal DRP	13 ms	20 ms	30 ms

4. Discussion

In this work a reconfigurable architecture for the development of electrical mapping equipments, the RAEM system, has been presented and tested. The RAEM architecture aims at standardizing the control system for the acquisition of a large number of bioelectrical signals independently of the hardware solution. Characteristics of the presented architecture have been studied in order to define the optimal implementation of the RAEM modules. This architecture has demonstrated its usefulness to control systems that acquire different amounts of data: from a short number of Kbps until hundreds of Mbps. Roles of the temporal memory of the FPGA and the processor capability of the RTC on the selection of optimal configuration parameters (Data Readout Period, Data Segment Size, etc) have been evaluated. Finally, the RAEM has been used under different National Instruments hardware solutions showing its versatility and ability to migrate to different hardware solutions.

The design of this system based on LabVIEW and RIO hardware architecture of National Instruments, allows to avoid the challenge of designing a customized embedded system (both hardware and software), strategy typically used for deployment of cardiac mapping systems [6]. In addition, RAEM is conceived with a modular structure and is programmed with a high-level language such as LabVIEW. This allows the adaptation to Hardware systems based on LabVIEW FPGA and Real Time Modules such as FPGA based R Series Multifunction RIO or NI FlexRIO with PXI (PCI eXtensions for Instrumentation) Controlers or PCs as RTCs. LabVIEW is a graphical programming environment which has emerged as an standard "de facto" for data acquisition, instrument control and analysis software. These properties, along with the amount of hardware compatible (signal generators, oscilloscopes, sensors...); make the RAEM architecture, an ideal tool for clinical research.

Acknowledgements

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