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Laser-micromachined, Chip-scaled Ceramic Carriers for Implantable Neurostimulators

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Abstract— **Hermetic encapsulation of long-term implantable devices using ceramics has been investigated over several decades. Our studies focus on the miniaturization of ceramic encapsulations for large numbers of stimulation channels. Laser-patterning of screen printed platinum (Pt) paste on cofired ceramics has been shown to enable the construction of features comparable in size to classical screen printing. A novel technique for embedding Pt structures into the surface of Al_20_3 substrates is shown to produce features with a line width minimum of 20 μm and a pitch of 40 μm. Polishing the ceramic substrates enables flip-chip bonding of application specific integrated circuits (ASIC) using gold stud bumps. A new technique for fine tuning of an ASIC stimulator with stud bump bridges is described. The technique eliminates the need for wire bond loops and increases reliability and integration density of the system, which are major requirements used to construct a visual prosthesis or other implantable devices requiring miniaturization. The methods for laser-patterned Pt tracks in alumina for fine pitch structures are described. Feasibility studies for flip-chip bonding and stud bump bridges were undertaken and the results were found to be promising.**

I. INTRODUCTION

Implant development, especially in the area of retinal prosthesis, has to overcome two major problems: the space available for implantation inside the host is very limited and the materials must withstand the harsh biological environments of the human body.

Some implantation sites offer a relatively large space to implant the devices in the human body. For example, pacemakers or bladder stimulators can be implanted into the torso where large pockets can be found. However, available space in regions of the brain or close to the brain is much more limited. Focusing on the development of a visual prosthesis, the use of micro-electronics is indispensable in regard to space limitations given. The still ongoing miniaturization could overcome the issues of macro-electronics which have been employed for neural stimulators in the '70s [1].

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Another problem in terms of miniaturization is packaging of the electronics. Chip-scale packaging is commonly used in the field of micro-electronics since the early '90s due to the need of smaller and cheaper devices. Modern microtechnologies have brought up multiple methods to connect integrated circuits (IC) to substrates on the die level [2]. The developments in miniaturization and advanced packaging in combination with new electrode designs and improvements in surgical methods have made new implantation sites viable alternatives for the placement of a visual prosthesis [3].

Although modern microtechnologies enable adequate miniaturization of the device, the materials utilized do not fulfill the second criteria. Corrosion, delamination, and subsequent failure of the electronics inevitably occur when appropriate precautions are not taken. However, hybrid packages made of alumina can withstand the harsh physiological environment supporting multiple electrical interconnects of 'feedthroughs' within the hermetic carrier substrate. On the downside, these hard shell packages are often critized as being too large [4]. Thick film technology to produce such feedthroughs was successfully employed by Donaldson over 40 years ago [5].

Many research groups are focused on avoiding the problems associated with polymer-based hermetic encapsulation. Here, we focus on the miniaturization of hybrid packages as a visual prosthesis for the blind [6].

Screen printing of metallic particles in slurry is a technique utilized widely in industry. Thixotropic properties and flow characteristics of the paste defines the minimal feature size. This is typically in the range of 125 μm and a pitch of 250 μm. Features of this size are too large for bonding a high density stimulator chip and would result in a device which is too large to accomodate within the patient.

There are challenges associated with mounting a chip inside a hermetic, hard, hybrid encapsulation. Wire bonding is commonly used to connect ICs to substrates. In 1993, 93% of all chips were connected using this technology whereas 26% of all IC failures were related to the wirebond [7]. Therefore, this technique cannot be considered as a reliable interconnection technology in regard to medical devices. A more reliable technology is flip-chip bonding. However, our previous method [9] was not compatible with flip-chip mounting due to inadequate surface smoothness and flatness. Flip-chip bonding in prototype applications employs gold (Au) stud bumps on both the substrate and chip. After bumps

are formed, the chip and substrate are bonded. This requires an average surface roughness and flatness below 0.5 μm and 1 μm, respectively [8].

ASICs for neural stimulation frequently contain configuration bits that need to be affixed to a power supply rail in order to place the ASIC in a preferred mode of operation for varying applications, or trim certain parameters. This can also be achieved via fuse bits or electrically erasable programmable read-only memory (EEPROM). However, fuse bits generally need to be supported by the foundry and EEPROMs require ancillary circuits which may not be favourable depending on the number of configuration bits required to achieve the same result. The pads could be ball-wedge wire bonded to another track on the substrate, however such an approach would raise reliability issues and result in increased implant volume. A preferable approach would be the use of stud bump bridges. This option is made possible via miniaturization of the screen printed tracks. To create a bridge, the configuration pads are brought as close as possible to a power supply track on the substrate and stud bumps are used to join the tracks where required. Such technique allows robust connections that demand minimal volume uptake. The connections themselves are lighter than the ball-wedge wire bond alternative, which place less stress on the tracks regardless of orientation of the final implant, thereby enhancing the reliability of the connections.

Recently, we have reported on a laser-patterning technique to reduce feature size and decrease prototyping time, which resulted in small features but poor surface quality [9]. This paper describes an advanced technique which results in smaller, chip-scale features, decreased surface roughness and improved surface flatness, thereby enabling flip-chip bonding and configuring of prototype ASICs through the use of stud bump bridges. The technology is compatible with an implantable, highly-reliable visual neuroprosthesis under development by the authors.

II. Methods

A. Laser Micro-Machining

An Nd:YAG marking laser (Genesis Marker, ACI) with a scanner head was employed for laser micro-machining. The structures to be created were designed using computer aided design (CAD) software. The designs were then split into single laser elements using custom written lisp routines. The resulting vector files were imported into the laser software and converted into hatch grid fields. This method resulted in an improved vector distribution of the hatching grids, thereby reducing the minimum possible feature sizes achievable with the scanner head of the laser.

1) Grooving: A 200 μm thick tape composed of alumina particles and binders was grooved using fine-tuned parameters (Fig. 1a).

2) Screen Printing: 50 μm stainless steel foil was machined with the same laser. An opening was cut into the foil and used as a stencil for screen printing. Platinum (Pt) paste was printed across the whole structure by running a rubber squeegee across the open area (Fig. 1b).

3) Drying: The paste was subsequently dried in a convection oven at 130 °C for 15 min to volatilize the solvents (Fig. 1c).

4) Sintering: Sintering of the ceramic tape and the metallic paste was carried out at 1500 °C in a horizontal tube furnace. To ensure initial flatness, the samples were placed on sinter setters and slow ramp rates used to ensure complete burnout of binders in the ceramic tape before reaching the dwell temperature (Fig. 1d).

5) Polishing: After firing, the ceramics were polished using diamond and silicon carbide polishing pads, followed by a diamond particle suspension (Fig. 1e). The polishing removed all excess Pt on the surface, leaving grooves in the surface of the ceramic filled with metal (Fig. 1f). This also resulted in the removal of contaminating layers which are commonly observed on the screen printed tracks after firing in furnaces without air flow.

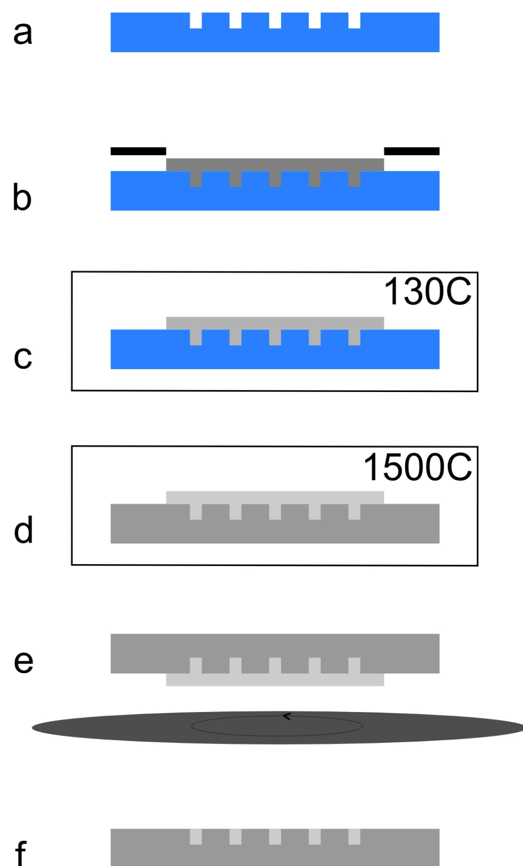

Fig. 1. Process flow of laser micro-machining. a. laser grooving of ceramic tape, b. screen printing of Pt paste, c. drying of Pt paste, d. sintering of ceramic and paste, e. polishing, f. ceramic with Pt filled grooves.

B. Flip-Chip Bonding

During sintering and densification process the ceramics shrank by up to 20% dependent on the processing parameters. However, the manufacturing tolerances were relatively

large and impeded the use of lithographic bumping technologies like indium bumping [10] due to mask alignment difficulties. To overcome this problem a technique with higher admissible tolerances was selected. The bumps were placed on the ASIC using a wire bonder. Fine pitch capillaries and 17 μm Au wire were required to place bumps corresponding to the small patterns of the ASIC. The chip was then flip-chip bonded to the substrates. The final step in the assembly was the underfilling of the chip with epoxy to provide stability.

C. Stud Bump Bridges

Stud bump bridges are a means to provide fixed connections to supply rails for configuration bits on the ASIC, and trim bits for fine adjustment of ASIC outputs. The authors prefer this approach over programmed settings for improved reliability. Pt tracks were designed to match the configuration pads of the ASIC. The tracks were routed to create a close gap between each other (Fig. 2). An Au stud bump was placed to bridge the gap and establish an electrical connection between the two using 25 μm Au wire bonds.

III. Results

A. Laser Micro-Machining

Laser micro-machined screen printing produced features with a line width of 20 μm and a pitch of 40 μm. In comparison to earlier results using laser-ablation of pastes or classical screen printing, this technique produced features that are smaller by a factor of 2 and 10, respectively.

The small sized features enable the construction of chip-scaled packaging technology smaller than has been previously reported [9].

Electrical characterization of the tracks showed a sheet resistance of 0.05 Ω.

Profilometer measurements of the surface indicated an average surface roughness of less than 200 nm and a flatness of less than 600 nm (Fig. 3). The larger value of the flatness may be due to the removal of grains from the bulk material by pullout during polishing. Nevertheless, the prerequisites for succesful flip-chip bonding were exceeded.

B. Flip-Chip Bonding

While flip-chip bonding is a well established process and widely applied, we focused on the bonding properties of the stud bumps to the substrate. While stud bumping of the chips was relatively simple (Fig. 4), flipping and bonding the ASIC to the substrate was not trivial due to adherence problems between a stud bumped chip and the Pt surface (Fig. 5). Two methods have been tested to overcome this issue: the tracks were electroplated with Au, or the substrate was stud bumped as well as the chip and the flip-chip bonding achieved between the two stud bumps. Both methods worked without any further problems. Because the substrate and the chip can be stud bumped with the same process cycle, the latter option was preferred.

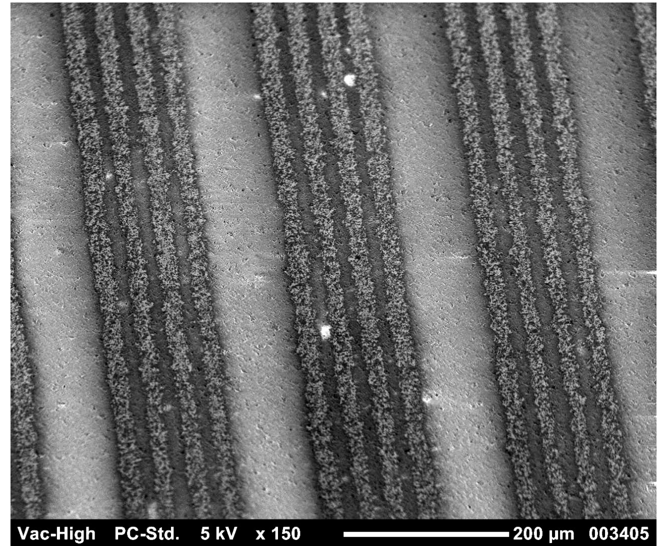

Fig. 2. Laser micro-machined Pt tracks showing three sets of 4 tracks embedded in a ceramic substrate with the minimum line width of 20 μm and a center-to-center distance of 40 μm for configuration bits of the ASIC.

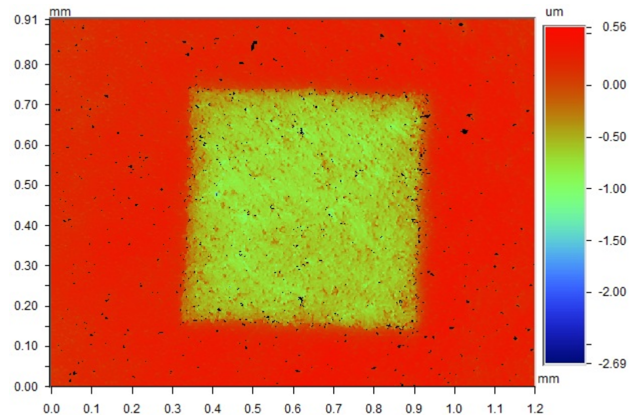

Fig. 3. Typical profilometer measurement of the polished ceramic and a Pt pad. Average roughness is below 200 nm and flatness is less than 600nm. The dark spots are due to pullout of grains from the bulk material during polishing.

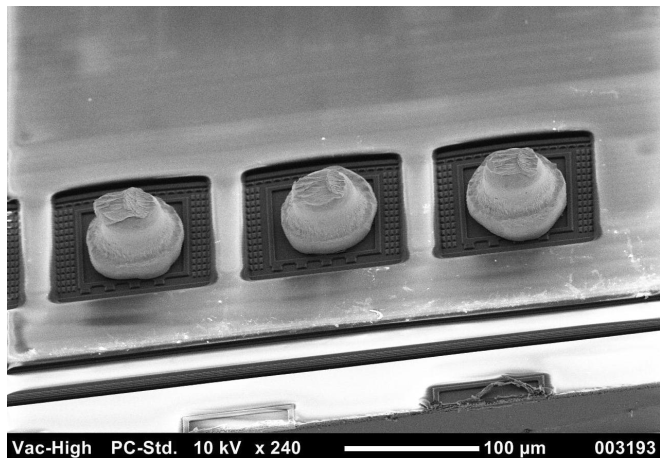

Fig. 4. Au stud bumps made with a fine pitch capillary on the ASIC in preparation for flip-chip bonding. The ASIC is then flipped onto the Pt pads on the ceramic substrate.

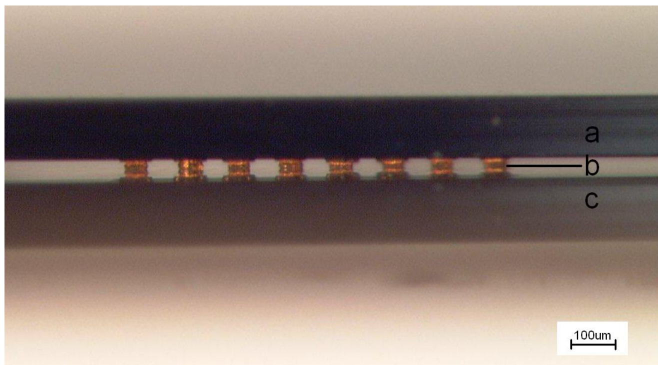

Fig. 5. Side view of a section of the ASIC (a) bonded with Au stud bumps (b) to the ceramic carrier (c) before the underfill was applied. The ASIC was flipped onto the ceramic carrier and bonded with ultrasound and thermo-compression.

C. Stud Bump Bridges

Stud bumping of the tracks was achieved without difficulty (Fig. 6). This was consistent with what was observed during flip-chip bonding. By reducing the feature sizes to approximately that of the wire bonder capillary, a significant amount of pressure could be applied while bonding the stud bump to the track. A stable thermocompression bond between Au and Pt could be achieved, passing the requirements of destructive shear testing according to ASTM F 1269-89.

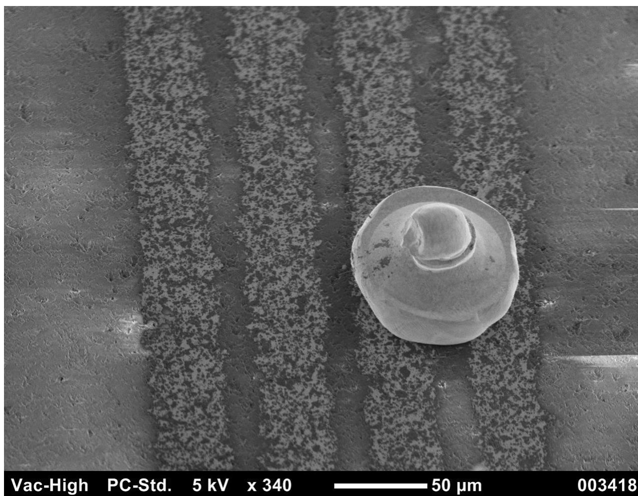

Fig. 6. An electrical interconnection is created by placing an Au stud bump to join a configuration track of the ASIC to a power supply track in order to place the ASIC in a preferred mode of operation for varying applications.

IV. Discussion and Conclusions

Sintering structured alumina substrates that are completely covered with Pt paste is a new technique of producing embedded tracks. Laser micro-machining of screen printed Pt paste has been shown to be a feasible technique to miniaturize hybrid technologies down to the chip-scale level. The anticipated problem of extensive stress generation in substrates sintered with printed metal tracks covering a large proportion of the surface has been proven wrong [9]. Mechanical stresses arrising due to the mismatch of the thermal expansion coefficients of the different materials and the associated delamination problems are reduced by embedding the tracks into the bulk material. The use of polishing techniques eliminates the problem of varying film thickness of the Pt paste. This problem was associated with previous techniques.

The higher quality of tracks produced by the new laser micro-machining process enabled flip-chip bonding at the level of the substrate and rendered wire bonds unnecessary. Furthermore, chip-scale configuration of the ASIC for rapid prototyping using stud bump bridges was possible.

However, there are several limitations and shortcomings which should not be overlooked: Embedded tracks can only be applied on the outer surfaces of a substrate. Laser ablation of thick film pastes is indispensible in the intermediate layers of a multiple layer substrate [11]. Configuration bits on ASICs have known solutions which require less space - fuse bits or EEPROMs can be implemented in ASICs, although not all foundries and ASIC processes support this approach.

In summary, the technique of laser micro-machining screen printed Pt paste can be used to fabricate hybrid packages which are sufficiently small for use in devices like retinal implants and can withstand the harsh biological environment in the human body for the remaining lifetime of the implant receipient.

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