# A Band-Tunable, Multichannel Amplifier for Neural Recording with AP/LFP Separation and Dual-Threshold Adaptive AP Detector

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Abstract—This article presents a low-power low-noise neural recording system comprising a set of 4-channel amplifiers and a dual-threshold adaptive action potential detector. The front-end amplifier is optimized for power efficiency, noise, and silicon area. A balanced tunable pseudo-resistor is used to acquire local field potential (LFP) and action potential (AP) separately. The post-layout simulation results show that the system achieved input referred noise 4.7µVrms and noise efficiency factor (NEF) 2.79 with mid-band gain of 51.9dB and power consumption of 5.22µW. The bandwidth is highly tunable in the range of 2.38Hz-300Hz for high-pass corner and 248Hz-12.9kHz for low-pass corner, which can acquire AP and LPF without out-band noise. The proposed dual-threshold adaptive AP detector can capture action potential precisely from background activity, thus data reduction can be realized by only processing these significant waveforms. The results show that the proposed low-power, low-noise biomedical system is suitable for implantable device applications.

#### I. INTRODUCTION

**R**ECENTLY, progress in CMOS technology and low-power circuit design make the applications of implantable prosthetic devices come true. Multi-electrode array has been used in recording/stimulating animal neurons. The signals recorded by electrode array are generally known as extracellular neural signals (ENG), including action potential (AP) and local field potential (LFP). The amplitudes of these signals are in the order of tens to hundreds of micro volt and the frequencies range from sub-hertz to tens of kilo-hertz [1].

To record these indistinct signals, front-end neural amplifier is the most capital block in biomedical implantable devices. The total input-referred noise of the front-end amplifier must be maintained smaller than the background noise of the electrode ( $5-10\mu$ V). Hence, low-noise design is the first thing to be considered in this article. Several methods have been reported, such as chopper stabilization (CHS) and auto-zeroing (AZ).

However, chopper stabilization consumes much more power and auto-zeroing works well only for low-frequency noise such as DC offset. The most popular solution is utilizing the MOSFET at sub-threshold [1]-[6]. Further, the front-end amplifiers should have accurate bandwidth to pass the action potential (300Hz-10kHz) and local field potential (1Hz-300Hz) respectively while rejecting the unwanted DC offset. High tunable range makes design a challenge. In addition, low power consumption is desirable in the application of implantable devices, heat produced from the power-hungry chip can eventually injury the deep-skin cells.

This work utilizes transistors operating in sub-threshold

region with capacitive feedback to implement a set of low-power low-noise 4-channel front-end amplifiers. The capacitive feedback scheme affords robust low frequency noise suppression without additional feedback circuitry. The design of two bands for recording AP and LFP is demonstrated. It can acquire two kinds of signals clearly, which is different from many other works of band-tunable amplifier [4], [5]. Action potential detector is an indispensable block in multichannel recording system for the reason that the appearance of action potential is only 1% of the time [2]. A precise AP detector can reduce unnecessary computation and power for processing raw data. We proposed a low-power, dual-threshold adaptive AP detector without interference of back-ground noise.

This paper is organized as follows. Section II describes the system architecture. Section III presents the post-layout simulation results of the system. Section IV concludes the paper.

#### II. SYSTEM ARCHITECTURE AND IMPLEMENTATION

Fig. 1 shows the block diagram of the biomedical system comprising 4-channel front-end amplifiers with multiplexer and a dual-threshold adaptive action potential detector.

Conventional designs used single stage to achieve mid-band gain; however, in a neural amplifier, the gain is decided by the ratio of the feedback capacitor  $C_f$  and the input capacitor  $C_{in}$ . Using two-stage scheme can save much more silicon area than the single stage.

In this work, the feedback capacitor was chosen to be 150fF, which is larger than the parasitic capacitances of recording site. The high cutoff frequency is decided as below [2]



Fig. 1. Block diagram of the 4-channel neural recording system, consisting of low-noise pre-amplifiers with a multiplexer and dual-threshold adaptive AP detector

$$f_{H} = \frac{G_{m}}{2 \pi C_{L} (\frac{C_{in}}{C_{f}})}$$
(1)

The first-stage is design as a low-noise stage with the gain of 30dB and second-stage is a high-swing stage with 20dB gain. Lower power consumption is achieved because of lower  $C_{in}/C_f$  ratio at the second-stage.

### A. Band-Tunable, Low-Noise Neural Amplifier Design

The input referred noise of the overall system is dominated by the noise of the first-stage transistors. We chose the telescopic differential topology to achieve the best noise-power trade-off, as indicated in Fig. 2. The noise analysis of first stage is:

$$e_{eq}^{2} = \frac{e_{to}^{2}}{(g_{m1}R_{out})^{2}} = 2en_{1}^{2} + 2(\frac{g_{m7}}{g_{m1}})^{2}en_{7}^{2} + 2(\frac{1}{g_{m1}r_{o1}})^{2}en_{3}^{2} + 2(\frac{1}{g_{m1}r_{o1}})^{2}en_{5}^{2} \approx 2en_{1}^{2}(1 + (\frac{g_{m7}}{g_{m1}})^{2}\frac{en_{7}^{2}}{en_{1}^{2}})$$
(2)

The result reveals the effective noise voltage power spectrum density, where *e* is power spectrum density of the noise voltage,  $R_{out}$  is the effective output resistance, and  $r_o$  represents the output resistance of the transistor. According to the concept of the inversion coefficient (IC) introduced in [7], the intrinsic transconductance of a transistor can be expressed as below by EKV model:

$$g_m = \frac{kI_D}{U_T} \frac{2}{1 + \sqrt{1 + 4IC}}$$
(3)

Consequently, the power spectrum of flicker noise and thermal noise can be represented by IC, and we can achieve low-noise circuit by choosing proper IC for each transistor. IC<0.1 represents the transistor operating in the weak inversion regime; for IC>10, transistor works in the strong inversion regime.

Eight diode-connected transistors are used as voltage divider for common mode voltage of the first stage. For the second stage, a folded-cascade structure is implemented to achieve a higher output swing. The noise contribution is smaller than the first stage, thus input transistor sizes can be reduced to save the chip area and the bias current can be lower. Moreover, this two-stage topology consumes less power when maintaining the same bandwidth.

The main purpose of the neural recording system is its ability of acquiring local field potentials together with action potential. Precisely tunable bandwidth can remove undesired signals and out-of-band noise. A tunable balanced pseudo-resistor from [8] was modified by using 3.3V MOSFETs, because thicker oxide can enlarge the resistance. Balanced resistors are required to avoid signal-dependent output shift caused by asymmetric resistances.

High cutoff frequency is designed to be highly tunable by utilizing an effective large capacitor [9]. In this capacitor scaler, current through the capacitor is sensed and amplified by the current mirror; the equivalent impedance is reduced by this mechanism and an effective large capacitance is achieved.



Fig. 2. Circuitry of the low-noise stage amplifier.

#### B. Signal Recording Multiplexer

While analyzing biomedical signal, acquiring a collection of neural signals at the same time is essential. For the multiplexer, a control circuit is used to obtain signals of each channel automatically instead of the conventional decoder. The multiplexer is indicated in Fig. 3.The offset-free buffers are used to replace the common-drain circuit in [10]. An over-back counter is used in control circuit, and the operation steps are: (1) when Rst\_bar signal is released, all channels trace the signals; (2) when HOLD signal is released, transmission gates are turned off and signal in each channel are held; (3) each channel is turned on alternately. Transmission gates connected with output buffer are alternately turned on, and the output buffer transmits the held signals from each channel.

#### C. Dual-Threshold Adaptive Action Potential Detector

The proposed AP detector utilizes the characteristic of extracellular signal having biphasic peak to apply a dual-threshold method [6]. However, it is difficult to determine the threshold due to the background activity. An adaptive threshold settled by background noise sensing circuit is used to decline the error rate of spike detection.

The extracellular signal first generates a negative peak, and a positive peak occurs at about 1.5ms later than negative peak.

After the AP detector sensed a negative peak, a window is produced by windowing circuit and the action potential is detected only when the positive peak is captured within the window. Therefore, the exactness of the threshold in positive peak detector is crucial. Our strategy is to combine adaptive threshold setting circuit [2] with the above dual threshold method. Fig. 4 shows the details of the AP detector.



Fig. 3. Four-channel analogue multiplexer and digital control circuit

The function of the adaptive threshold setting circuit is to measure the standard deviation of the Gaussian background noise and set a threshold voltage according to this value. A two-stage gm-C filter is used to implement a low-pass filter. By using current division and source degeneration OTA [11], low power and low cutoff frequency filter can be achieved. In Fig. 4, current division is implemented through MF1 and MF2. Transistors Mr1 and Mr2 act as source-degeneration resistors.

The windowing circuit consists of a charging circuit and a Schmitt trigger. When a peak is detected, the output of charging circuit will pull down rapidly by large-scale transistor M1; meanwhile, output of the Schmitt trigger  $V_{wout}$  will be pull up to high. The capacitor starts to charge the output node  $V_{cho}$  until reaching a particular threshold which forced the node  $V_{wout}$  to low level. Transistors Mp3 and Mn3 act as pull-up and pull-down transistor, respectively. A window which possesses the duration of 1.5ms is achieved by this mechanism.

## III. POST LAYOUT SIMULATION RESULT

The proposed 4-channel front-end amplifiers, signal recording multiplexer and AP detector were implemented in a 0.18- $\mu$ m standard CMOS process. The total silicon area is 1.28×1.14 mm<sup>2</sup> including pads. Post-layout simulation results show that the mid-band gain is 51.9dB, with tunable low cutoff frequency ranges from 2.38Hz to 300Hz and high cutoff frequency ranges from 248Hz to 12.9kHz, as shown in Fig. 5. The input referred noise is 4.7 $\mu$ V<sub>rms</sub> while consuming 5.22 $\mu$ W.

The phase margin, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) of the first-stage telescopic OTA and the second-stage folded-cascade OTA are shown in Table I.

Fig. 6 shows the waveforms of the control signals and the multiplexer output when recording a set of four signals. For Fig.6 (a), the row 3-6 demonstrate a set of alternately-triggered control signals, row 7-10 are signals from channel-0 to channel-3. The top row shows the multiplexer waveform which traces the signals from each channel in turns. The top row of Fig. 6(b) presents the output of multiplexer when holding signals . At the falling edge of Hold signal, the values of four signals in row 7-10 are held. During each selection, the multiplexer output presents these held signals individually.





imitated neural waveform consists of spikes and background noise. Row 2 and row 3 show the result of positive peak detection and negative peak detection, respectively. The window produced after negative peak detector catches a positive peak is shown in row 4. The last row is the consequence of the neural signal detection.



Fig. 5. Frequency responses for (a) local field potential and (b) action potential



Fig. 6. The multiplexer output waveforms of (a) tracing signal and (b) recording signal



 ${\rm Fig.7}$  . Detection waveform of the dual-threshold adaptive action potential detector

To estimate power, noise, and bandwidth among pre-amplifiers, noise efficiency factor (NEF) is widely used to compare pre-amplifier designs [12].

$$NEF = \frac{V_{rms,in}}{\sqrt{\frac{4kT(BW\frac{\pi}{2})}{\frac{I_c}{U_T}}}} = V_{rms,in}\sqrt{\frac{2I_c}{4kT \cdot \pi U_T \cdot BW}}$$
(4)

Lower NEF indicates higher efficiency of pre-amplifier. Table II compares the post-layout simulation results of this work with previously reported literatures. The power consumption item is the comparison of single amplifier.

## IV. CONCLUSION

A system of low-power, low-noise 4-channel neural amplifiers with signal recording multiplexer and AP detector was fabricated using TSMC 0.18 $\mu$ m 1P6M CMOS process, the circuit layout is shown in Fig. 8. Balanced pseudo-resistors with ultra-wide tunable range facilitate the acquisition of LFP and AP signals separately. Two-stage structure improves the power efficiency. A front-end amplifier consumes only 5.22 $\mu$ W and the noise efficiency factor of 2.79 is achieved. The proposed action potential detector combines double threshold method with adaptive strategy to promote the detection efficiency. As a result, the system is a good candidate for multi-channel implantable device.



Fig.8. Chip layout of the overall system

 TABLE I

 POST-LAYOUT SIMULATION OPEN-LOOP PERFORMANCE

Parameter	<b>Open-loop Performance table</b>		
	First stage	Second stage	
Power supply(V)	+0.9/-0.9		
Gain(dB)	90.4	89.3	
Phase margin( ° )	56.3	.3 87.8	
CMRR(dB)	89.2	89.2 109.0	
PSRR+/-(dB)	98.2/90.6	75.1/99.1	

TABLE II					
BENCHMARK					
Parameter	This	[1]	[3]	[4]	
	work	07JNL	09JNL	10JNL	
Power supply (V)	+0.9/-0.9	3.3	3	3.3	
Power(µW)	5.22	N/A.	15	8.4	
Gain(dB)	51.9	>46	48-68	73	
High-cutoff	248-	1k-	500-	500-	
frequency(Hz)	12.9k	10k	5k	10k	
Low-cutoff	2.38-	0.1	0.01-70	0.5-	
frequency(Hz)	300			50	
Input-referred noise	4.7	13	7	6.08	
$(\mu V_{rms})$					
NEF	2.79	3.6	4.6	5.5	
Number of channels	4	256	256	128	
Tech.( µm)	0.18	0.35	0.35	0.35	

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#### REFERENCES

- J. N. Y. Aziz, et al., "Brain-silicon interface for high-resolution in vitro neural recording," IEEE Trans. on Biomedical Circuits and Systems, vol. 1, no.1, pp. 56-62, March 2007.
- [2] R. R. Harrison, "The design of integrated circuits to observe brain activity,"Proc. IEEE, vol. 97, no. 7, pp. 1203–1216, Jul. 2008.
- [3] J. Aziz et al, "256-channel neural recording and delta compression microsystem with 3D electrodes," IEEE J. Solid State Circuits, 2009, vol. 44, no. 3, pp. 995-1005.
- [4] F. Shahrokhi, K. Abdelhalim, D. Serletis, P.L. Carlen, R. Genov, "The 128-Channel fully differential digital integrated neural recording and stimulation interface," IEEE Trans on Biomedical Circuits and Systems, vol. 4, no.3, pp. 149-161, June 2010.
- [5] R. H. Olsson III, D. Buhl, A. M. Sirota, G. Buzsaki, and K. D. Wise, "Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays," IEEE Trans. Biomed Eng., 52, pp. 1303-1311, July 2005
- [6] Borghi, T.; Bonfanti, A.; Gusmeroli, R.; Zambra, G.; Spinelli, A. S., "A power-efficient analog integrated circuit for amplification and detection of neural signals" Engineering in Medicine and Biology Society, 2008.Page(s): 4911 – 4915
- [7] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," Analog Integrat. Circuits Signal Process., vol. 8, pp. 83–114, 1995.
- [8] A. Tajalli, Y. Leblebici and E. J. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors," Electron. Lett., vol. 44, Feb. 2008.
- [9] Josh Silva-Martinez and Sergio Solis-Bustos, "Design considerations for high performance very low frequency filters" Circuits and Systems, 1999, vol.2, Page(s): 648 - 651
- [10] M. Kachel, M. Żołądź, P. Kmon, "Design of 64-channel analogue multiplexer for neural application in CMOS 180 nm technology", Signals and Electronic Systems, September 2008, ICSES '08, pp. 77-80
- [11] Veeravalli, A.; Sanchez-Sinencio, E.; Silva-Martinez, J , "Transconductance amplifier structures with very small transconductances:A comparative design approach" Solid-State Circuits, IEEE, 2002. Page(s): 770 - 775
- [12] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," IEEE J. Solid-State Circuits, vol. SC-22, pp. 1163–1168, Dec. 1987.