33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

# A 1.72μW, 23.2fj/conversion step Successive Approach ADC for Bio-medical Signal Acquisition

Wei-Sheng Wang and Kea-Tiong Tang, Member, IEEE
E-mail: wswang@larc.ee.nthu.edu.tw, kttang@ee.nthu.edu.tw

**Abstract—This paper presents a successive approach register (SAR) analog-to-digital converter (ADC) with a novel hybrid digital-to-analog converter (DAC) architecture: half junction splitting (J.S.) and half binary weighted capacitor DAC. This DAC maintains low power consumption of J.S. DAC and the high signal-to-noise plus distortion ratio (SNDR) of binary weighted capacitor DAC. The power dissipation of the circuit is 1.72μW, SNDR 59.17dB, spurious free dynamic range (SFDR) 73.39dB, and the FOM 23.2fj/conversion step with 0.9V supply voltage. The proposed circuit is fabricated in TSMC 0.18μm 1P6M CMOS process technology.**

## I. Introduction

In recent years, research in bio-medical with electronic technique becomes popular. To acquire the signals of human bodies such like ECG, EEG, EMG, and ENG, which can be analyzed to monitor the body conditions of human beings, people use electronic devices. The frequencies of these signals are usually less than 100kHz [1], which is a low speed for electronic. Besides, if we need to make these monitor devices portable, the circuits in the device must be small enough to make the device be portable and low power to maintain the life time of battery. There are also monitor devices such as portable eNose that is used for detecting virulent gas immediately to ensure the safety in the air.

To deal with these signals, we need an analog-to-digital converter (ADC), which is an interface circuit between analog signal and digital signal process. There are many different architecture of ADCs with different characteristics and suitable for different applications. The successive approach register (SAR) ADC has moderate speed, moderate resolution (8-12 bit) and low power because it needs only one comparator, so it is the most suitable ADC for bio-medical application. The sub-circuits of SAR ADC that consumes the most power are comparator and DAC. The most common DAC is binary weighted capacitor DAC, which is easy to control and implement, but the power is directly proportional to the capacitors amount.

There are many researches in low voltage low power SAR ADC [1] - [8]. Different DACs are used in SAR ADC to reduce unnecessary power consumption from charging and discharging capacitors such as splitting capacitor [2] and junction splitting (J.S.) DAC [6]. The least power dissipation DAC is J.S. DAC, because it uses the characteristic of SAR ADC: bit-cyclic to decrease the power dissipation. But in the first bit-cycle of J.S. DAC, only the smallest capacitor is connected to comparator, which will suffer from the comparator kick-back noise and many other side effects. Therefore, the pure J.S. DAC has low signal-to-noise plus distortion ratio (SNDR), which is not suitable enough for implementation.

To increase the SNDR of ADC and maintain the character of low power, we propose a novel hybrid DAC that combine the J.S. DAC with binary weighted capacitor DAC, and we have designed the controller for this DAC. So, this novel SAR ADC successfully maintains low power consumption and high SNDR. The circuit architecture is discussed in Section II, the simulation results are presented in Section III, and the conclusion is in Section IV.

## II. Circuit Architecture

The conventional SAR ADC block diagram usually consists of four sub-circuits: track and hold (T/H), comparator, DAC, and controller, as shown in Figure 1. In our design, the primly modified cell is the DAC. The details of these sub-circuits will be described in the following parts.

### A. Track and hold

The track and hold circuit is illustrated in Figure 2 [8]. Because the supply voltage of ADC is 0.9V, which is half of the normal value, it will affect the turn on resistance of the track and hold switch and the speed of J.S. switch in DAC. To solve the problem, we use a simple boosting circuit to rise the turn on voltage of switches. It will alternately charge the two point "A" and "B" between $V_{DD}$ and $2V_{DD}$, rising the gate turn on voltage of NMOS switch to about $2V_{DD}$ when the "Sample" signal is high.

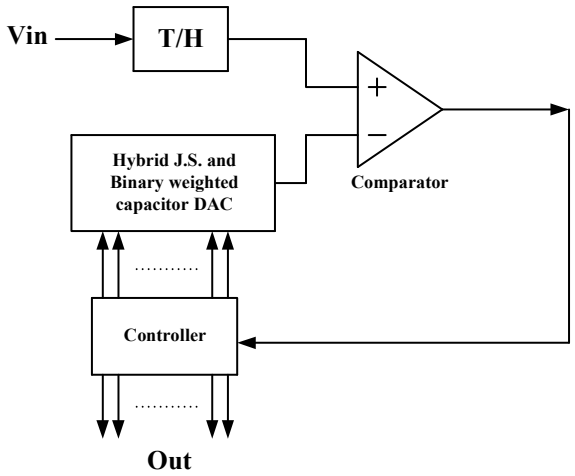


Figure 1. The architecture of proposed SAR ADC

### B. Comparator

The comparator we designed is shown in Figure 3. We use the easiest yet useful method to cover the rail-to-rail input voltage range that combining the NMOS input stage with PMOS input stage in parallel. To reduce the hysteresis, the comparator requires a reset step to make the output voltages of latch start from a common mode voltage, Vss. But the reset signal will cause kick-back noise to the T/H and DAC, especially when the DAC has small capacitors directly connecting to the comparator, so the noise will reduce the accuracy and SNDR hardly. To reduce the kick-back noise, the most common solution is using small size MOSFEF at the input stage, but the small size MOSFET will enlarge the mismatch of comparator, producing large offset voltage to the circuit. To reduce the offset voltage, we use one more stage of current mirror rather than lessening the input MOS to reduce kick-back noise.

### C. DAC

The J.S. DAC is a smart algorithm for binary voltage searching, but the capacitor directly connecting to comparator is too small to resist the noise especially the kick-back noise. To minimize the effect of noise, we combine the J.S. DAC with a binary weighted capacitor DAC. If the hybrid DAC has larger binary weighted capacitor DAC, the accuracy of the DAC is higher and the noise is lower, but it consumes more power, and vice versa. We choose the 7-bit binary weighted capacitor with 3-bit J.S. DAC to achieve the best balance between power consumption and SNDR.

The algorithm of proposed SAR ADC is demonstrated in Figure 4. The denominator represents the total capacitors connecting to comparator, and the numerator is the total capacitors that has been charged to $V_{DD}$ for voltage division.

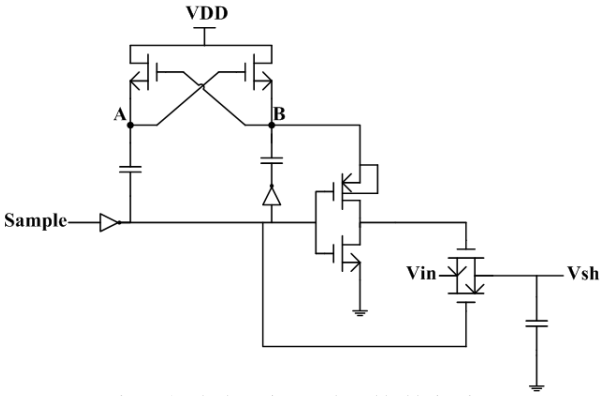


Figure 2. The boosting track and hold circuit

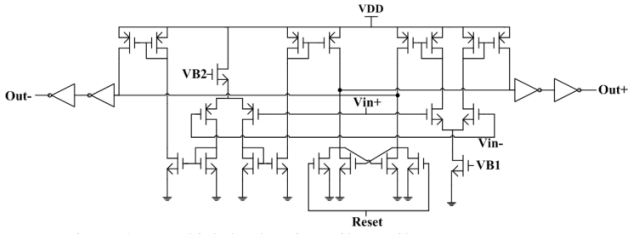


Figure 3. Low kick-back noise rail-to-rail comparator

When the SAR ADC starts to convert the signal, the controller will set the largest capacitor of the first section, binary weighted capacitor DAC, to $V_{DD}$, so the output voltage of DAC is $0.5V_{DD}$. The comparator compares the DAC voltage with input voltage which has been held on capacitor, and save the result of comparison to the controller to decide the voltage of DAC in the next step should be higher or lower. And the process will go on the next steps of voltage search until the last bit of the binary weighted capacitors section.

After all the conversion steps of binary weighted capacitor DAC have been done, the first section of J.S. DAC will connect to the binary weighted DAC through the boosting switch, and the controller of J.S. DAC just begins acting at this step to avoid the unnecessary charging and discharging of capacitors to reduce the power consumption. When the two DACs are connected together, the resolution of whole DAC is higher. It will go on the steps until the last bit of DAC has been done.

The critical number "X" in Figure 4 is always "1" if each bit before this step has been converted to logic 0. When any bit has been converted to logic 1 at step "S" in junction-splitting section, the value "X" will be added values in the order of 2, 2, 4, 8… in each the next bit, the actual value added to "X" depends on the bit conversion after step "S".

Because the two DAC is totally different, when the J.S. section is connected to the binary weighted section, the 7-th bit capacitor of the DAC will be overlapped. In an ideal case, the capacitors of this bit in whole DAC should be 8C (1C in binary weighted), if we directly connect this two section together, the 7-th capacitor will become 9C, so it needs to be modified. We split the capacitor of 7-th bit in the first section of J.S. DAC, 2C, one always connect to Vss, the other still connects to the original way to solve the issue.

The DAC voltage offset will occur because the binary weighted capacitor DAC is always connecting to comparator, while the J.S. is not. To reduce the DAC offset, we connect each part of J.S. DAC to a dummy comparator.

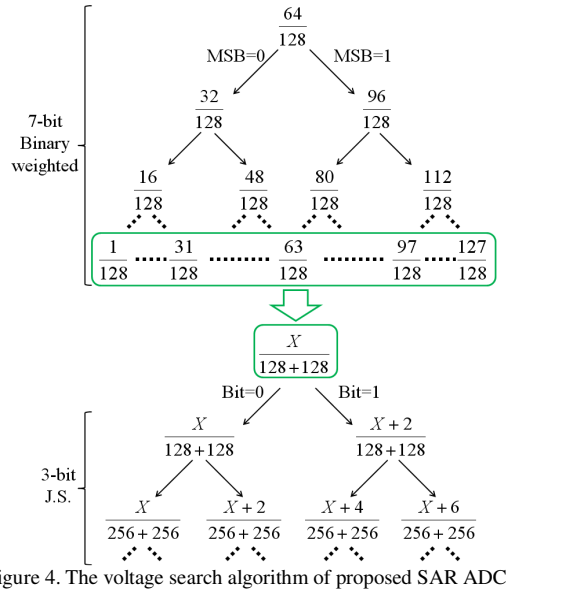


Figure 4. The voltage search algorithm of proposed SAR ADC

### D. Controller

As shown in Figure 6, the controller contains 3 parts from the top to its bottom. The first part is used for deciding the action timing of the other two parts, the second part controls the binary weighted capacitor DAC, and the last part controls the J.S. DAC including the capacitors and the switches. The signal "end of conversion" (EOC) will control another latch series to read and hold the 10-bit signal in a time.

## III. SIMULATION RESULT

Figure 7 shows the differential non-linearity (DNL) and integral non-linearity (INL) result, the DNL is+0.51/-0.49, and the INL is +0.07/-0.58.

We input an 0.9V peak-to-peak analog sine signal to the SAR ADC, and the ADC samples the signal in the rate of 100kS/s. Figure 8 shows the fast fourier transform (FFT) analysis of the output. The SNDR is 59.17dB with 9.53-bit effect number of bit (ENOB) and SFDR is 73.39dB when input signal is 0.34kHz, and the power consumption is 1.72μW.

$$ENOB \cong \frac{SNDR - 1.76}{6.02} \tag{1}$$

The layout of proposed SAR ADC is in Figure 9, the area of the whole chip is 893μm$^2$ with pad, and the core area is 440μm×430μm. We input the different frequency signal to diagram Figure 10, which is the result of SFDR and SNDR in pre-layout simulation versus post-layout simulation.

Table I is the summary of performance. The figure of merit (FOM) is

$$FOM = \frac{Power\ disspation}{Sampling\ \ frequency \times 2^{ENOB}} \tag{2}$$

Table II compares this work with the references in recent years. Our proposed SAR ADC has good FOM, low power, and the sampling rate is high enough for most bio-medical applications.

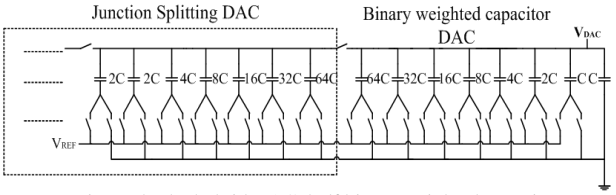


Figure 5. The hybrid DAC, half binary weighted capacitor and half J.S. DAC

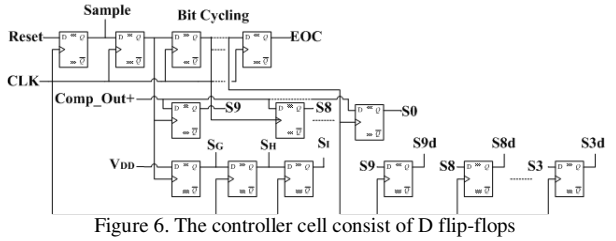


Figure 6. The controller cell consist of D flip-flops

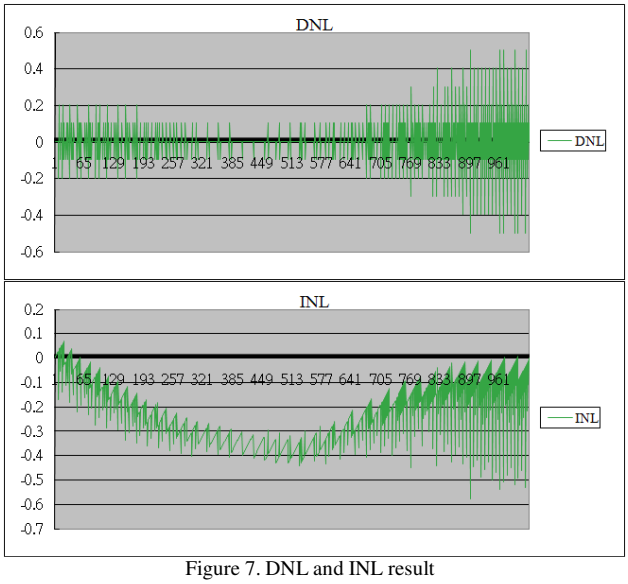


Figure 7. DNL and INL result

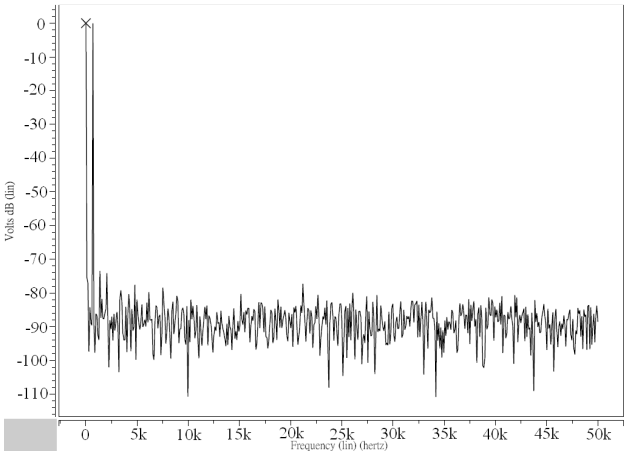


Figure 8. FFT spectrum of the SAR ADC, the input frequency is 0.34kHz

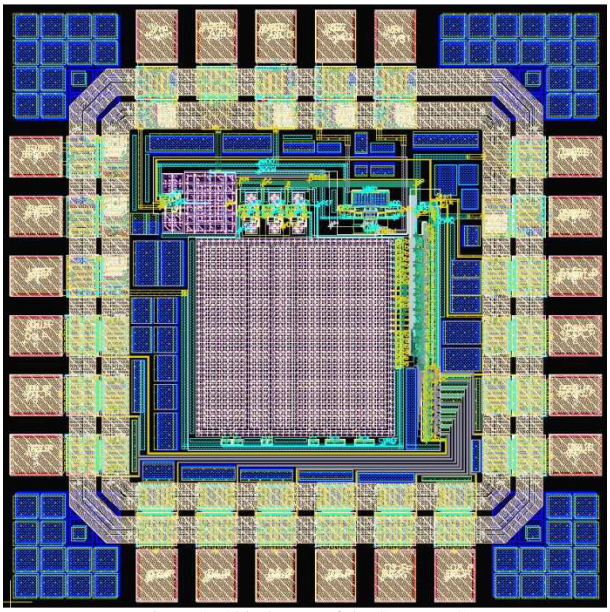

Figure 9. Chip layout of the SAR ADC

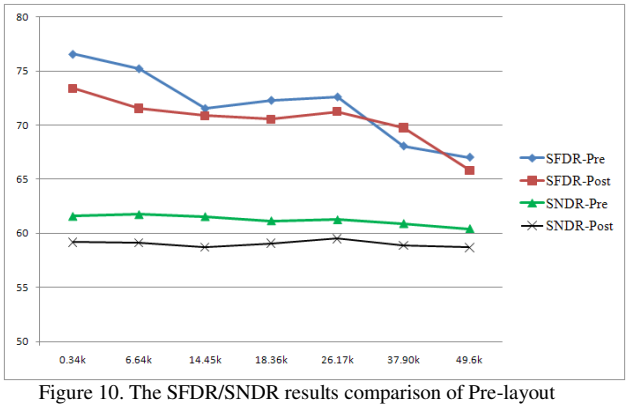


Figure 10. The SFDR/SNDR results comparison of Pre-layout simulation and Post-layout simulation with different input frequencies

Table I.
Simulation results

| | Pre-layout Simulation | Post-layout Simulation |
|---|---|---|
| **Supply Voltage** | 0.9V | 0.9V |
| **Input Range** | 0-0.9V | 0-0.9V |
| **Sampling Rate** | 100kS/s | 100kS/s |
| **SFDR** | 76.57dB | 73.39dB |
| **SNDR** | 61.57dB | 59.17dB |
| **ENOB** | 9.93-bit | 9.53-bit |
| **Power dissipation** | 1.27μW | 1.72μW |
| **FOM (fj/conversion step)** | 13 | 23.2 |

Table II.
Benchmark between this work and references

| | [2] | [3] | [5] | [7] | [8] | This work |
|---|---|---|---|---|---|---|
| **Year** | 2007 | 2007 | 2009 | 2009 | 2007 | 2011 |
| **Supply voltage** | 1V | 1V | 1V | 1V | 0.9V | 0.9V |
| **Process technology** | 0.18μm | 0.18μm | 0.18μm | 0.18μm | 0.18μm | 0.18μm |
| **Sampling rate** | 100kS/s | 10kS/s | 500kS/s | 100kS/s | 200kS/s | 100kS/s |
| **Resolution** | 12-bit | 8-bit | 10-bit | 10-bit | 8-bit | 10-bit |
| **ENOB** | 10.55-bit | 7.4-bit | 9.4-bit | 8.6-bit | 7.58-bit | 9.53-bit |
| **Area** | 900μm×700μm | 220μm×65μm | 470μm×510μm | | $62um^2$ | 440μm×430μm |
| **Power consumption** | 25μW | 1.8μW | 42μW | 8.27μW | 2.47μW | 1.72μW |
| **FOM (fj/conversion step)** | 165 | | 124 | 208 | 65 | 23.2 |

## IV. Conclusion

We present a novel and low power SAR ADC with hybrid DAC: half binary weighted capacitor DAC and half J.S. DAC. This SAR ADC is designed for bio-medical applications. The sampling rate 100kS/s is high enough for most human body signal acquisitions. This proposed SAR ADC has 59.17dB SNDR with 9.53-bit ENOB, the SFDR is 73.39dB, and the power dissipation is 1.72μW, which is very suitable for portable monitor devices like eNose and be applied in bio-medical signal acquisition.

## V. Acknowledgement

The authors would like to thank financial support of the National Science Council of Taiwan, under Contract NSC 100-2220-E-007-011. The authors would like to acknowledge the support of National Chip Implementation Center (CIC), Taiwan for chip fabrication.

## References

[1] Shuenn-Yuh Lee, IEEE Member, Chih-Jen Cheng, Cheng-Pin Wang, and Shyh-Chyang Lee "A 1-V 8-Bit 0.95uW Successive Approximation ADC for Biosignal Acquisition Systems" Ph.D. Research in Microelectronics and Electronics (PRIME), 2010 Conference.pp.649 – 652

[2] Naveen Verma, Student Member, IEEE, and Anantha P. Chandrakasan,Fellow, IEEE "An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes" IEEE JOURNAL OF SOLID-STATE CIRCUITS,VOL. 42, NO. 6, JUNE 2007

[3] Sang-Hyun Cho et al. "Design of a 1-Volt and μ-power SAR ADC for Sensor Network Application." Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on (2007) pp. 3852 - 3855

[4] Gosselin et al. "A Mixed-Signal Multi-Chip Neural Recording Interface with Bandwidth Reduction." Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE (2007) pp. 49-52

[5] Wen-Yi Pang; Chao-Shiun Wang; You-Kuang Chang; Nai-Kuan Chou; Chorng-Kuang Wang."A 10-bit 500-KS/s low power SAR ADC with splitting comparator for bio-medical applications." ASSCC 2009.pp. 149 – 152

[6] Jeong-Sup Lee; In-Cheol Park" Capacitor Array Structure and Switch Control for Energy-Efficient SAR Analog-to-Digital Converters." ISCAC 2008. pp.236 – 239

[7] Yung-Jui Chen; Kea-Tiong Tang; Wai-Chi Fang "An 8μW 100kS/s successive approximation ADC for biomedical applications", Life Science Systems and Applications Workshop, 2009. LiSSA 2009. IEEE/NIH

[8] Hao-Chiao Hong, Member, IEEE, and Guo-Ming Lee "A 65-fJ/Conversion-Step 0.9-V 200-kS/s Rail-to-Rail 8-bit Successive Approximation ADC" IEEE,JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 10, OCTOBER 2007. pp.2161 – 2168