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A 64-Channel Neuron Recording System

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***Abstract*—This paper presents a fully integrated low-power neuron recording front-end system in TSMC 65nm 1p6m CMOS technology. The proposed system is comprised of two recording modules, each containing 32 recording channels with tunable bandwidth and gain, a 32-to-1 multiplexer, one differential successive approximation register (SAR) analog-to-digital converter (ADC) with programmable sampling rate on each channel, and a digital control module to govern the signal digitization as well as to encode and serialize the digitized neuron signal from two ADCs. The recording amplifier presents a low power and low noise merits of 6 μW and input-referred noise of 3.8 μV_{rms}. The ADC digitizes the neural signal at a sampling rate of 40kS/s with 9-bit resolution. The overall power consumption of the entire system is 2.56mW and occupies an area of 3x4mm^2.**

I. Introduction

UNDERSTANDING how the brain functions by recording the electrical activity of brain cells (neurons) has been pursued by neuroscientists and clinicians. The underlying mechanism of how neurons fire and interact can be translated into skilled and precise movements, and understanding the mechanism can be used as a tool for diagnosing brain diseases. It has been shown that recorded neuron activities from the motor cortex can be used to control a robotic device [1]-[2]. Neuroscientists have employed neuron recording from scalp or chronically implanted intracranial electrodes to investigate the electrophysiological activity for epileptic seizure detection and prediction [2]. Those experiments involved recording a large population of neurons and thus stimulated the need for the development of a multi-channel neuron recording system.

Challenges of designing a neuron recording system is highly correlated with the characteristics of the physiological neuron signals. The recording device must be able to record these signal with a large dynamic range in terms of signal amplitude and frequency, and to reject the DC offset occurring at the electrode-electrolyte interface. Power consumption of the system has to be reduced for long-term operation and to avoid elevating the temperature of brain tissue which could cause permanent damages [3]. The electrode impedance and amplifier input impedance form a voltage divider and thus the practical neuron signal shown at amplifier input is smaller than its actual value. The degradation is severe for local field potentials (LFPs) recording because electrode impedance is much higher at 10 Hz than its value at 1-kHz [4]. If the neural signal at the recording amplifier input is seriously attenuated, it is difficult to be differentiated from the background noise. In addition, the next generation of this recording system should have the capability to process an enormous amount of neural information via signal detection, feature extraction, pattern classification and other mechanisms. The future recording system should also have the capability of reducing the amount of data to be transmitted and/or extracting a stable control signal from a large neuron pool in order to control prosthetic devices. The design challenges noted above can be translated into low-voltage and low-power design necessitating an advanced technology node.

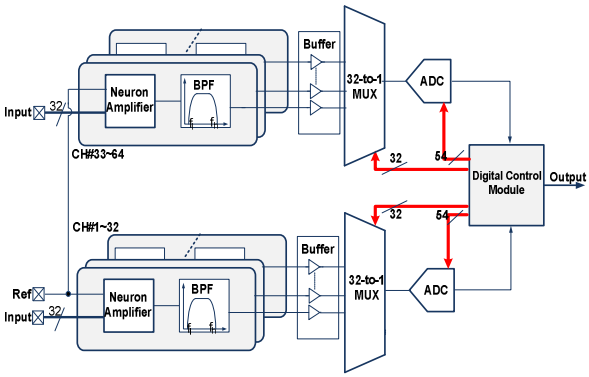

Fig. 1. Architecture of the proposed 64-channel recording system

This paper is organized as follows: Section II describes the system overview, while the circuit design is given in Section III. Section IV reports the simulation results, and finally, a conclusion is given in section V.

II. System Overview

The overall system architecture is shown in Fig. 1. The proposed 64-channel system includes two 32-channel recording units and a shared digital controller module (DCM). Each recording unit contains 32 recording channels, one 32-to-1 multiplexer, and an SAR ADC. Within each channel, the neuron amplifier first magnifies the infinitesimal neuron signal. A programmable gain and bandwidth filter is cascaded and configured based on the signal of interests. Buffer at each channel passes the filtered output to the multiplexer. The ADC then digitizes the signal with a sampling rate of 40kS/s per channel and feeds the output to DCM for data serialization and performing channel-specific processing to identify multi-site components.

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III. CIRCUIT DESIGN

A. Single Recording Channel

The schematic of one neuron recording channel is shown in Fig. 2. The first stage adopted an AC-coupled amplifier and provided a mid-band amplification of 39.6 dB. The high-pass cutoff frequency of this amplifier is set by the MOS-bipolar pseudo-resistor formed by $M_{RA1\text{-}RA12}$ and the feedback capacitor, C_f. The high-pass and low-pass cutoff frequencies of the subsequent bandpass filter can be adjusted by tuning V_{tune} to change R_{HPF} and by altering the value of C_L, where R_{HPF} is formed by PMOS transistors $M_{RB1\text{-}RB11}$ operating in weak inversion and C_L is the load capacitor of the bandpass filter. The recording channel has the capability to adjust its gain from 47 dB to 59 dB. A critical issue rising from using a sub-100nm process is the increased gate-leakage current compared to the less advanced process. A difference of 2Å in the gate oxide thickness can lead to an order of magnitude change in the gate-leakage current [5]. Therefore, in our design $M_{RA1\text{-}RA12}$, $M_{RB1\text{-}RB12}$, and input transistors of amplifier A_1 are implemented with thick-oxide I/O transistors in order to reduce the current flowing into the gate, which would increase the amplifier noise and lower the resistance of the pseudo-resistor.

B. Gain-boosted Amplifier

The mid-band gain of the neuron amplifier can be approximated as

$$\frac{V_{out}}{V_{in}} \approx \frac{C_{in}}{\frac{C_{in}+C_f+C_{par}}{A_1}+C_f} \tag{1}$$

, where C_{par} and A_1 are the parasitic capacitance of the input transistors and the open-loop gain of the amplifier, respectively. C_{in} is expected to be small to achieve high input impedance and small area, while C_f must also be reduced to achieve a reasonable gain. Though gain error is acceptable for neuron amplifier, a high open-loop gain is still desired to suppress the parasitic effect resulting from large size input transistor and capacitors. However, a high gain is difficult to achieve under the constraint of low supply voltage of 1.2V and power limitation. Here we designed a gain-boosted folded-cascode amplifier, as shown in Fig.3, to enhance amplifier's open-loop gain while simultaneously reducing the input-referred noise. The biasing condition of the proposed

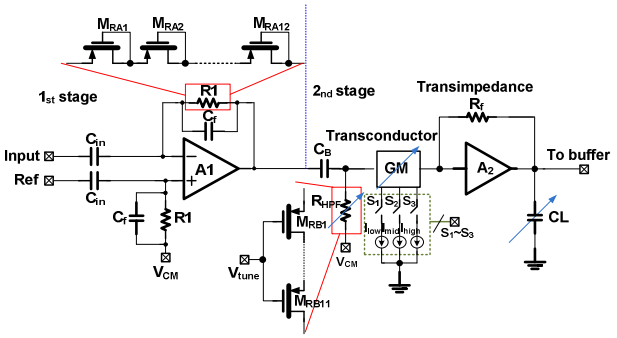

Fig. 2. Schematic of one neuron recording channel

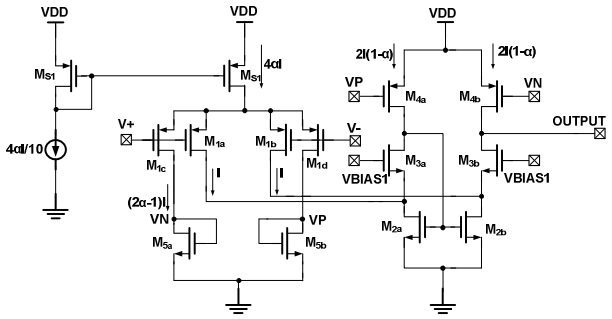

Fig. 3. Schematic of the gain-boosted amplifier

amplifier is similar to the technique used in [4] in which only a small fraction of overall current is flowing into the folded branch of M_3-M_4 reducing its noise contribution. Nonetheless under 1.2V supply voltage, it is impractical in our design to add a source degenerated resistor to lower the noise from M_2. We utilized the fraction of current taken from M_2 to build an auxiliary gain stage formed by $M_{1c\text{-}d}$ and $M_{5a\text{-}b}$. The additional gain stage enhanced the gain of the amplifier to $1+(2\alpha-1)g_{m4}/g_{m5}$) times and simultaneously reduced the noise from M_2. By biasing the input differential transistor M_1 into sub-threshold region, the input-referred noise of the amplifier can be derived as

$$\overline{v^2_{rms,n}} = \frac{4KT}{\kappa}\left(\frac{1}{\left(g_{m1}+g_{m1}(2\alpha-1)\frac{g_{m4}}{g_{m5}}\right)}\right) + \frac{8KT\gamma g_{m2}}{\left(g_{m1}+g_{m1}(2\alpha-1)\frac{g_{m4}}{g_{m5}}\right)^2} + \frac{16KT\gamma g_{m4}}{\left(g_{m1}+g_{m1}(2\alpha-1)\frac{g_{m4}}{g_{m5}}\right)^2} \tag{2}$$

, where K is the Boltsmann constant, κ is the sub-threshold gate coupling coefficient, g_{mi} is the transconductance corresponding to transistor M_i, T is the absolute temperature, α is the current the redistribution ratio in the amplifier, and γ is the thermal noise coefficient. Eq. (2) demonstrates the input-referred noise can be reduced by using the gain-boosted topology. Note that g_{m2} and g_{m4} in (2) are small due to the reduced current flowing through. The value of C_{in} and C_f is chosen as 5pF and 50fF for input impedance, noise, and power tradeoff.

C. Variable Gain Bandpass Filter

The variable gain BPF aims to provide independent tuning capabilities of gain and bandwidth in one single stage in order to reduce the power consumption. This filter is composed of a cascade of a transconductor and a transimpedance amplifier with a load capacitor [6], and an RC first order high pass filter as shown in Fig. 2. The voltage gain of the filter is decided by the product of transductance GM and R_f, which is the feedback resistor of the transimpedance amplifier. Thus, the gain can be adjusted by setting the current flowing in the transconductor. The variable gain bandpass can provide 7dB-19dB gain within a given bandwidth.

A. Neuron Signal Digitization

A differential charge-redistribution SAR ADC is designed to digitize 64-channel neuron signals. The ADC architecture is

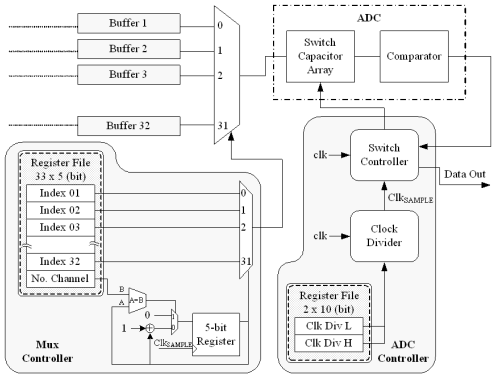

Fig. 4. The schematic of ADC and DCM

based on [7] with unit capacitance of 20fF. An ADC controller and a multiplexer controller are incorporated in the DCM. A 32:1 multiplexer is placed in front of each ADC to select the channel for sampling. Although using a 5-bit counter to sequentially loop from channel 1 to 32 is straightforward, it may not be the most desirable method in all circumstances. For example, not all of the channels have proper input to be sampled at any time, and the user might only be interested in a subset of channels. Therefore, a channel-of-interest feature is implemented in the multiplexer controller. This enables the user to choose an arbitrary subset of channels, and turn off the rest in order to save power. Some of the channels can even have a higher sampling frequency than others.

Fig. 4 shows the architecture of this multiplexer controller. A 33 x 5 register file is employed to store the sampling channel indices as well as the number of channels that will be used. To enable a subset of four specific channels, say ch1, ch10, ch19, and ch28, the register file should be filled with 1, 10, 19, and 28 in the first four entries, and 3 in the last entry. The 5-bit counter will loop from 0-3, thus the desired channel indices will be sent to the channel multiplexer sequentially to enable these channels, and all other channels will not be sampled. If the third entry in the previous example is replaced by ch1, then ch1 will be sampled when the 5-bit counter is either 0 or 2, so it has twice the sampling frequency of ch10 and ch28. Thus, a channel can be filled into multiple entries in the register file to achieve a sampling frequency up to 16 times higher than others.

A programmable 20-bit clock divider is implemented in the ADC controller and serves two purposes: to dissociate the

Fig. 5. The layout of the proposed 64-channel recording system

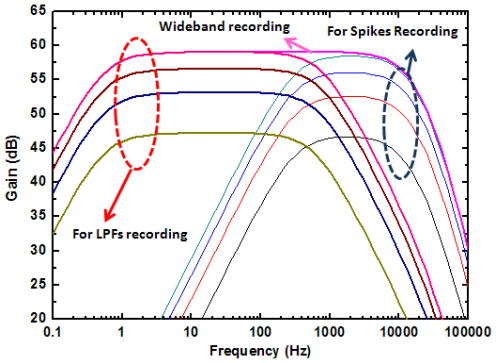

Fig. 6. Frequency response of one recording channel

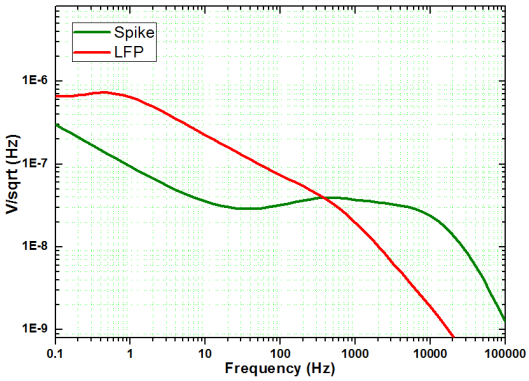

Fig. 7. Simulated input-referred noise of the neuron recording channel for LFPs and spikes recording setting.

sampling frequency and the oscillator frequency; to provide a flexible sampling frequency setting for each ADC. There are two ADCs in this system, so a high frequency oscillator is required for data stream handling. The clock divider can generate appropriate clock frequency for ADC operation no matter what frequency the oscillator is. In addition, since the channel-of-interest feature allows the user to enable a subset of channels, the accumulated frequency is lower in this mode. Thus, the clock divider can be used to set the accumulated sample frequency for each individual ADC based on the number of activated channels and the desired sample frequency per channel.

IV. Simulation Results

The proposed 64-channel neuron recording system was designed and under fabrication in TSMC 65nm CMOS process. The entire system is operated and simulated under 1.2V supply while consuming 40 μW per channel. Note that only 6 μW is consumed by the neuron recording amplifier and BPF. The chip layout occupies an area of 3x4 mm^2, as shown in Fig. 5. The current layout and power consumption are not optimized for testing purpose.

Fig. 6 shows the frequency responses of one neuron recording channel. For recording LFPs, the system exhibits a programmable gain from 47 dB to 59 dB within the bandwidth from 0.5Hz to 500Hz. While with the immediate setting for spike recording, the system provides variable gain from 46.5

dB to 58.5 dB from 300 Hz 12 kHz. Note that the gain of spike recording is slightly lower than that of LFPs because of smaller R_{HPF} value, which lowers the overall output impedance of neuron amplifier. The simulated input-referred noise for both configurations of LFPs and spikes recording is shown in Fig. 7. For LFPs recording, 1/f noise still dominates and thus it is difficult to distinguish the thermal noise level. The overall input-referred noise for both recording settings are 2 μV_{rms} (integrating from 0.1 Hz to 5 kHz) and 3.8 μV_{rms} (integrating from 30 Hz to 100 kHz) under 47 dB gain configuration. Note that the noise integrating bandwidth here is much larger than the signal bandwidth. Since the popular NEF metric [3] only concerns the current of the amplifier, it cannot reflect the power efficiency. Thus we compared both NEF and the modified metric [10]

$$NEF^2 * VDD = \overline{v_{rms,in}^2}\left(\frac{2P}{\pi * kT/q * 4kT * BW}\right) \quad (3)$$

, where P is the power consumption of the amplifier and BW is the signal bandwidth.

The performance of the neuron recording system and comparison with other published works is summarized in Table I. The proposed recording system has high input impedance to mitigate the inevitable signal attenuation at the electrode-amplifier interface. The proposed recording amplifier with bandpass filter presents the lowest NEF^2*VDD product. An ADC with a flexible sampling rate for individual channels further gives the user more flexibility to monitor the neuron signal of interests. The overall power consumption of the entire system is 2.56 mW at a system clock rate of 23 MHz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Reference	[3]	[8]	[9]	This Work
Technology	0.5µm CMOS	0.5µm CMOS	0.18µm CMOS	65 nm CMOS
No. of channels	1	16	16	64
Supply voltage (V)	2.8	3.3	1.8	1.2
Mid-band gain (dB)	40.9	39.6	70	47~59
High-cutoff freq.(Hz)	0.392 ~295	0.2~94	100	0.5~0.3k
Low-cutoff freq. (Hz)	45 ~5.32k	140 ~8.2k	9..2k	500, 12k
Input referred noise (μV_{rms})	3.06	1.94	5.4	3.8[*1], 2.0[*2]
Input impedance @ 1kHz (Mohm)	11.38	7.9	-	31.8
Power consumption of amplifier (µW)	7.56	26.4	8.6	6
NEF	2.37	2.9	4.9	3[3]
NEF^2*VDD	15.7	27.7	43.2	10.8
ADC sampling rate/per channel	-	16k or 500	30k	4k~40k
Resolution (bits)	-	7~12	8	9
Overall power consumption (mW)	-	1.8	0.68	2.56

[1] with noise integrating bandwidth of 30 Hz to 100 kHz
[2] with with noise integrating bandwidth of 0.5 Hz to 5 kHz
[3] for spike recording

V. CONCLUSION

A 64-channle neuron recording system was presented. By using the proposed gain-boosted topology, we can increase the amplifier input impedance while simultaneously reduce the noise. The system can be configured to record LFPs and neuron spikes, respectively, with low-power consumption. With the flexible DCM, any subset of the recording channels can be activated for recording with independent sampling rate at each channel. Our future work will focus on the design of wireless interface to transmit recorded neuron data and the on-chip neuron processor to perform real-time signal processing.

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