33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

A 8.6 µW 3-Bit Programmable Gain Amplifier for Multiplexed-Input Neural Recording Systems

Khaled Al-Ashmouny, *Student Member, IEEE,* Sun-Il Chang*, Student Member, IEEE,* and Euisik Yoon, *Member, IEEE*

***Abstract*—We report a fully-integrated low-power 3-bit programmable-gain amplifier (PGA) that can be used as the second stage amplifier to adjust the gain for multi-channel neural recording systems. The design strategy maximizes energy-efficiency using a technique by optimizing a slew rate, gain and phase margin. The PGA consumes 8.66µW from 1-V single supply. This is an order of magnitude lower than the previous designs reported up to date. Analysis, simulation, and measurement results will be described in detail for a part of a multiplexed 16-channels neural recording system. In this implementation, while giving a full flexibility of gain control, the overhead for each channel is quite negligible: only 0.54µW in power and less than 0.002mm^2 in area.**

I. Introduction

Recording hundreds of neural activities is one of the most critical challenges in order to understand the brain dynamic behavior; however, providing an implantable system that allows the simultaneous access of large number of recording channels is still remained as a crucial barrier. While the state-of-the-art circuits operate with several milli-watts of power to record 32 channels [1], increasing the number of channels by 10X or more requires a significant reduction of power and area by the same factor. Area can be reduced effectively by multiplexing channels into a few leads using time-division multiplexing (TDM) [1-2]; otherwise, it would be hard to implement to access multiple channels as reported in [3], where only one full channel can be processed at a time even though 100 amplifiers are available on chip.

Power reduction, on the other hand, can be effectively optimized by tweaking every individual circuit component to minimize the overhead per channel. Fig. 1 shows a typical architecture of a neural recording analog front-end. Most of power-aware designs have been focused on lowering the power in the front-end low-noise amplifier (LNA) [4-5]. Designers strived to design highly energy-efficient LNA since it is the most critical block to reduce noise, and should be the most power consuming block in the channel. Less attention, however, has been paid to the power overhead of other circuit blocks in the signal chain, especially in the relatively high-speed power-hungry blocks after the TDM.

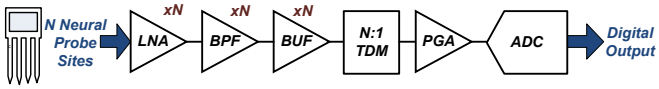


Fig. 1. Example of analog front-end for neural recording. When the number of recording sites is N, it will require N LNAs, N BPFs, and N buffers followed by N:1 TDM, PGA, and ADC.

One example is the 2nd stage gain amplifier for driving an analog-to-digital converter (ADC). More importantly, this block is almost always required since a typical low-noise amplifier provides a gain of only ~40dB [1-2,4-5]. This is not enough to provide a full-scale input to the ADC, thus losing resolution unless the signal is boosted by an additional gain stage.

For the 16-channel analog front-end (AFE) in [2], the 2nd stage amplifier provides an additional gain of 17-20 dB, externally controlled by a capacitor value, and consumes around 134µW, equivalent to power overhead of 8.37µW per channel. Surprisingly, the LNA consumes less power of 6.6µW. This shows that the 2nd stage amplifier adds more power overhead, and thus wasting the overall channel energy efficiency. Some other designs [6] implemented the programming of gain in the first-stage low-noise amplifier; however, this may significantly degrade noise efficiency and increase the implementation area.

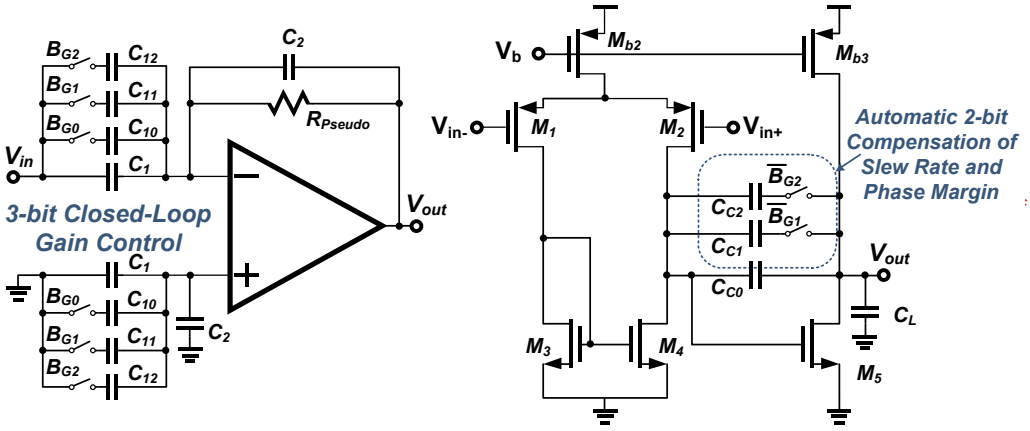
It is also important to provide a wide-range of gain selectivity, such that the full-scale ADC input cannot only accommodate the large-amplitude local field potentials but also the small-amplitude spikes that may be as small as 100µV. Many of the designs [1-3], however, do not provide this feature and thus degrade the effective ADC resolution by 1-2 bits when the maximum input range is only up to 50-25% of the full-scale range.

The objective of this work is to implement an energy-efficient programmable-gain amplifier (PGA) that has a wider range of gain control, consumes an order of magnitude less power, and maximizes energy efficiency. The PGA was designed to operate ideally for a 16-channel multiplexed system for the proof of concept. It was reported in [7] that the optimum area-power product can be achieved when multiplexing 16 channels. Assuming 6kHz bandwidth per channel, driving the ADC would require a minimum of 96kHz bandwidth.

In the next section, the design and analysis of the PGA is described. The design procedue applied in this work can be applied to other circuit blocks as well. Section III shows the

Manuscript received April 9, 2011. This work was supported in part by NSF ECCS-0925441 and Center for Wireless Integrated Microsystems.

K. M. Al-Ashmouny, Sun-Il Chang and E. Yoon are with the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI 48109 USA (email: ashmouny, schang, esyoon@umich.edu)



Device	Size	I_b [µA]	IC
M_1, M_2	400/0.3	2.475	0.016
M_3, M_4	12/1	2.475	0.48
M_5	18/1	3.7	0.49
M_{b1}	10/2	0.495	1
M_{b2}	100/2	4.95	1
M_{b3}	75/2	3.7	1
C_C	0.4-1.8pF	-	-
C_L	1 pF	-	-
C_1= 2xC_2	2x100fF	-	-
C_{10}= 2xC_2	2x100fF	-	-
C_{11}= 8xC_2	8x100fF	-	-
C_{12}= 16xC_2	16x100fF	-	-

Fig.2. Schematic of the proposed 3-bit programmable gain amplifier. In the open-loop OTA, feedback capacitor is automatically adjusted for slew rate/phase margin compensation in 2-bit accuracy.

simulation and measurement results followed by the conclusion.

II. Energy-efficient programmable gain amplifier

Two techniques have been pursued in our design to maximize the energy efficiency. One is to push low supply voltage and the other is to adjust the slew rate according to the gain. Particularly, low supply voltage is critical since the power consumption of digital circuits in the recording/processing blocks is proportional to the square of the supply voltage. In our design, supply voltage was reduced to 1-V and all the transistors are biased in either moderate or weak inversion regions. The supply current can be significantly reduced by optimally allocating bias currents and considering the feedback factor (β) determined by the selected gain. Slew rate can be determined according to the selected gain. The closed-loop PGA (Fig. 2) has a 3-bit (B_G<0..2>) gain programming from 6dB to 29dB (2x to 28x) adjusted by selecting different input capacitors.

A. Low-Power Two-Stage Operational Transconductance Amplifier

In order to achieve a stable closed-loop gain of up to 29dB (28x), a high enough open-loop amplifier (~80dB) is needed to reduce a gain error down to less than 3%. Under the low-voltage operation a two-stage differential-input operational transconductance amplifier (OTA) was adopted (Fig. 2). Reducing the supply voltage while maximizing signal swing has been achieved by biasing all the devices in moderate inversion [8] with the inversion coefficient (IC) between 0.1 and 10. IC is determined by the ratio of the drain current (I_D) to the specific current (I_S) of a particular MOS transistor (MOST). The specific current is given by:

$$I_S = 2n \cdot \beta_{MOS} \cdot U_T^2 \quad \text{.....(1)}$$

where n is the slope (~1.4 in 0.25µm CMOS), U_T is thermal voltage, and β_{MOS} is determined by transistor dimensions, given the carrier mobility and oxide capacitance.

There are many tradeoffs when biasing the transistors in moderate inversion. As compared with the strong inversion, the most compelling feature is that it can significantly reduce the headroom requirement by half. However, there are penalties. The device size and current consumption should be relatively larger in order to achieve the required slew rate and bandwidth. Fig. 2 shows the size and inversion coefficient of the transistors used in our OTA. All of them are biased in moderate inversion except for the input differential pair that is biased in weak inversion to provide a large gain and large output resistance.

The optimization was carefully performed to reduce the current consumption while maintaining the performance of the required slew rate, bandwidth, and phase margin. As shown in Fig. 2, a 2-bit selection of the feedback capacitor automatically adjusts all these parameters for the corresponding gain selection. This novel technique will benefit especially when a large gain (>16x) is selected. The large gain imposes a larger slew rate requirement and most probably the user is recording extracellular action potentials (EAP), where the signal amplitude is 100-500 µV with a bandwidth of ~6kHz. On the contrary, small gains will be selected for recording local field potential (LFP), where the signal amplitude is 1-3 mV (assuming a small electrode < 150µm^2) with a bandwidth of 300Hz. In either cases, the dominant pole location changes automatically according to the selection of feedback capacitors (C_{0C}, C_{1C} and C_{2C}) to guarantee the stability with a minimum phase margin of 60° under any gain and feedback factor (β), where

$$\beta = \frac{C_2}{C_2 + C_1 + B_{G0}.C_{10} + B_{G1}.C_{11} + B_{G2}.C_{12}} \quad \text{.....(2)}$$

The amplifier consumes the total current of 8.66µA, which gives by more than an order of magnitude lower power consumption than the amplifier reported in [2]. The current ratio between the 1st and 2nd stages was chosen to be 10:7.5 in order to accommodate a tradeoff between phase margin and slew rate. Table I summarizes all the parameters (β, gain, phase margin, slew rate (SR), etc.) for each programmable values selected by the 3 bit of B_G<0..2>. The next subsections analyzes the gain and phase responses and shows that this

TABLE I
ANALYSIS OF GAIN AND PHASE RESPONSE PARAMETERS

B_{G2}	B_{G1}	B_{G0}	Gain [V/V]	Gain [dB]	β	C_C [pF]	ω_{p1} [kHz]	ω_{OL_UGF} [MHz]	ω_{LG_UGF} [MHz]	ω_z [MHz]	ω_{eq} [MHz]	Phase Margin	SR [V/µs]
0	0	0	2	6	0.33	1.8	0.44	4.4	1.45	6.6	4.1	70.5	2.75
0	0	1	4	12	0.2	1.8	0.44	4.4	0.88	6.6	4.1	77.9	2.75
0	1	0	10	20	0.091	1.4	0.57	5.7	0.52	8.5	4.8	83.8	3.5
0	1	1	12	21.6	0.077	1.4	0.57	5.7	0.44	8.5	4.8	84.76	3.5
1	0	0	18	25.1	0.053	0.8	1	10	0.53	15	6.3	85.2	6.2
1	0	1	20	26	0.048	0.8	1	10	0.48	15	6.3	85.6	6.2
1	1	0	26	28.3	0.037	0.4	2	20	0.74	30	8	84.7	12.4
1	1	1	28	29	0.034	0.4	2	20	0.68	30	8	85.1	12.4

adaptive scheme can significantly reduce the overall system power consumption, while other appropriate metrics are achieved.

B. Gain Response Analysis

The target open-loop DC gain is set to 80dB and the major amount of current is consumed in the 1st stage to improve slew rate. The gain of 1st and 2nd stages can be expressed as:

$$A_{v1} = g_{m1,2}.R_{out1} \quad \text{.....(3)}$$

$$A_{v2} = g_{m5}.R_{out2} \quad \text{.....(4)}$$

where transconductance can be calculated from EKV model [9] as:

$$g_m = \frac{I_D}{n.U_T}.\frac{2}{1+\sqrt{1+4.IC}} \quad \text{.....(5)}$$

The total output resistance (R_{out1}) from M_2 and M_4 is around 1.2MΩ, and the $g_{m1,2}$ is 68µS. This provides a gain of ~38dB (A_{v1}). In the 2nd stage, g_{m5} is 74.4µS at 3.7µA bias current and output resistance is around 2.24MΩ. This gives a gain of ~44dB (A_{v2}).

For a complete gain response, the systems poles and zeroes need to be calculated. The dominant pole in this OTA is determined by:

$$\omega_{p1} = \frac{1}{(1+A_{v2}).C_C.R_{out1}} \quad \text{.....(6)}$$

Assuming a dominant pole system, there will be a 20dB/decade attenuation for the frequencies higher than ω_{p1}. Therefore, the open-loop gain of 80dB requires a dominant pole location of around 23Hz given the closed-loop gain of 6dB (2V/V) is selected and 160kHz bandwidth is required. For the maximum closed-loop gain of 29dB (28V/V), it should be at 400Hz for the same bandwidth. This indicates the maximum range of C_c should be 2-36pF, and thus the minimum achievable slew rate can be 0.14-2.5V/µs. This slew rate exceeds the minimum requirement of 0.005V/µs for LFP and 0.16V/µs for EAP. To improve the slew rate as well as compensate for any possible process variations, C_C was chosen in the range of 0.4-1.8pF. This will locate the dominant poles at 0.44-2kHz range as summarized in Table I. The output and mirror poles (ω_{p2} and ω_{pm}) are determined by:

$$\omega_{p2} = \frac{g_{m5}}{C_L + C_{gs5} + C_{ds5}} \approx \frac{g_{m5}}{C_L}, \omega_{pm} \approx \frac{g_{m3}}{2.C_{gs3}} \quad \text{.....(7)}$$

Given the load capacitance (C_L) of 1pF, C_{gs3} of 30fF, and g_{m3} of 50µS (from (5)), the output and mirror poles are located at ~12MHz and ~132 MHz, respectively. According to the location of the output and mirror poles, the equivalent high-frequency pole will be at ~12MHz. Finally, a right-half plane zero can be estimated from:

$$\omega_z \approx \frac{g_{m5}}{C_C} \quad \text{.....(8)}$$

The location of zero is about 6.6-30MHz, which does not indicate a need for adding any extra compensation resistors for the given the target closed-loop bandwidth of less than 200kHz.

C. Phase Response and Stability Analysis

For various gains set by the capacitors, C_1 and C_2, a phase margin of more than 60° should be maintained across different feedback configurations. As shown in Fig.2, the transfer function of the closed-loop configuration is:

$$\frac{V_{out}(s)}{V_{in}(s)} = A_{CL}(s) = \frac{A(s)}{1+\beta.A(s)} \quad \text{.....(9)}$$

where the open loop frequency-dependent gain *A(s)* is given by:

$$A(s) = A_0.\frac{(1-s/\omega_z)}{(1+s/\omega_{p1}).(1+s/\omega_{p2}).(1+s/\omega_{pm})} \quad \text{.....(10)}$$

The closed loop may oscillate (be unstable) if the loop gain ($LG = \beta A(s)$) has an amplitude of 1 and a phase shift of 180°. A dominant pole system can be assumed within the bandwidth of interest and we can approximate *A(s)* and loop gain as:

$$A(s) = A_0.\frac{1}{(1+s/\omega_{p1})}, \text{ and } LG = \beta.A_0.\frac{1}{(1+s/\omega_{p1})} \quad \text{....(11)}$$

While the phase responses of *A(s)* and *LG* can be exactly same, the unity gain frequency may not. Ideally, the unity-gain frequency of *A(s)* can be approximated as $\omega_{OL\_UGF}=A_0.\omega_{p1}$. However, the unity-gain frequency of the loop gain will be given by $\omega_{LG\_UGF}=\beta A_0\omega_{p1}$. Substituting (11) into (9), the actual 3dB bandwidth (ω_{3dB}) of the closed-loop system is equal to ω_{LG_UGF}. Thus, ω_{3dB} will be located in the same range of 1.45-0.68MHz, which is high enough to multiplex more than 16 channels of neural signals.

Now let us check the phase margin. All the non-dominant poles and zeros in the system can be grouped as one equivalent high-frequency pole ω_{eq}. Thus A(s) can be expressed as:

$$A(s) = A_0.\frac{1}{(1+s/\omega_{p1}).(1+s/\omega_{eq})} \quad \text{.....(12)}$$

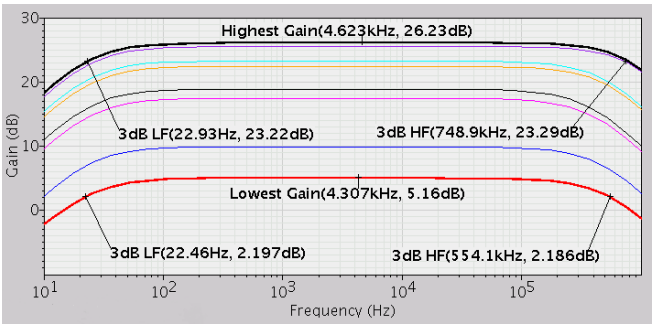
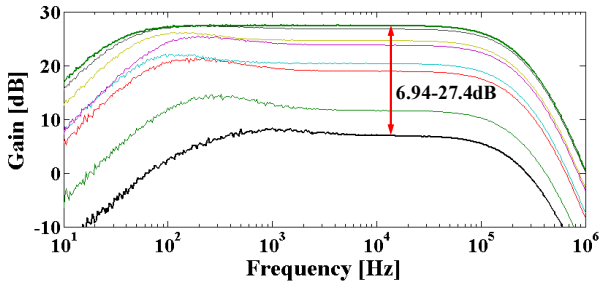


Fig.3. Simulation results of 3-bit gain programming.



Code	Gain [dB]	Input p-p voltage (THD < 1%) [mV]
000	6.94	40
001	11.63	39.6
010	19	39.2
011	20.35	36.9
100	23.82	24.4
101	24.65	22.7
110	26.8	17.9
111	27.4	16.8

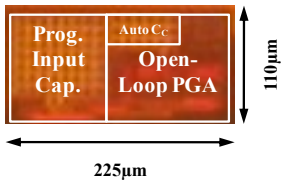


Fig.4. Measured gain response and chip photograph.

At frequencies much higher than ω_{p1}, $A(s)$ can be written as:

$$A(s) = A_0.\omega_{p1}.\frac{1}{s}\frac{1}{(1+s/\omega_{eq})} = \omega_{OL\_UGF}.\frac{1}{s}\frac{1}{(1+s/\omega_{eq})} \quad ...(13)$$

Thus, the loop gain, $\beta A(s)$, has a unity magnitude at ω_{LG_UGF} (or easily ω_{3dB}). In other words, the phase margin (PM) can be calculated as follows:

$$PM = 90^\circ - \tan^{-1}\frac{\omega_{LG\_UGF}}{\omega_{eq}} \quad .....(14)$$

As shown in Table I, the calculated PM based on (14) is more than 70° in the worst case. and this will allow more room for process variations.

III. Simulation and Measurement Results

Fig. 3 shows the simulated gain response with a total current consumption of 8.66µA and indicates acceptable gains and frequency corners for multiplexing neural signals more than 16 channels. The PGA was fabricated and tested in 0.25µm CMOS process and consumes 0.025mm^2 of silicon area. Fig. 4 shows the measured gain response, which shows a good match with the simulations and analysis results to guarantee a bandwidth higher than 160kHz. The chip microphotograph and gain values are also shown in the same figure. The transient response has been tested using a 100kHz sinusoidal wave, as shown in Fig.5. The result confirms the gain programming and the dc offset cancellation of input

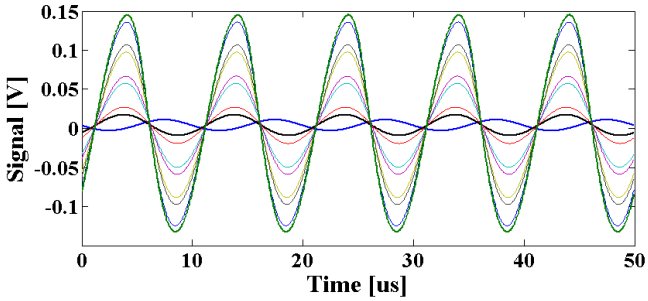


Fig.5. Measured transient responses using 100kHz sinusoidal waveform.

signals, which are critical for multiplexing channels.

IV. Conclusion

A low-power 3-bit programmable-gain amplifier (PGA) has been demonstrated. The proposed PGA utilizes a novel technique of biasing in moderate inversion and adaptively adjusting slew rate and compensation capacitance for different gains to lower the power consumption. The PGA, fabricated in 0.25µm CMOS, operates from 1-V single supply and consumes 8.6µW, which is by an order of magnitude lower than similar PGAs reported up to date. Analysis, simulation, and measurement results indicate that the proposed scheme is applicable for multiplexed 16-channels neural recording systems with negligible power and area overhead per channel.

References

[1] M. Yin and M. Ghovanloo, "A flexible 32-channel simultaneous wireless neural recording system with adjustable resolution", in *IEEE ISSCC 2009 Dig. Tech. Papers*, pp. 432-433.

[2] M. S. Chae, Z. Yang, M. R. Yuce, L. Hoang and W. Liu, "A 128-channel 6 mW wireless neural recording IC with spike feature extraction and UWB transmitter," *IEEE Trans. Neural Syst. Rehab.*, vol. 17, pp. 312-321, 2009

[1] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid State Circuits,* vol. 42, no. 1, pp. 123–133, Jan. 2007.

[3] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, pp. 958–965, June 2003.

[4] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.

[5] G. E. Perlin, A. M. Sodagar and K. D. Wise, "A Neural Amplifier with High Programmable Gain and Tunable Bandwidth," in *Proc. of the IEEE EMBC Conf.*, Vancouver, Canada, 2008, pp. 3154-3157.

[6] M. S. Chae, W. Liu, and M. Sivaprakasam, "Design Optimization for Integrated Neural Recording Systems," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1931–1939, September 2008.

[7] Y. Tsividis, "Moderate inversion in MOS devices," *Solid-State Electronics*, vol. 25, pp. 1099-1104, 1982.

[8] C. C. Enz, F. Krummenacher and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Cir. Signal Proc.*, vol. 8, pp. 83-114, 1995.