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A 1.5V 120nW CMOS Programmable Monolithic Reference Generator for Wireless Implantable System

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***Abstract*— We implement and characterize a 1.5V 120nW CMOS programmable monolithic reference generator for wireless implantable system. The proposed generator is optimized to be tolerable for power supply variation in a small area with programmability to generate various reference voltages and currents. The measured power line sensitivity are 0.02 / 1.1%/V for voltage and current reference, respectively. This reference generator can operate for input voltage ranging from 1.5V to 3.5V and implemented in an area of 0.011 mm^2, which is the smallest monolithic reference generator in 0.25μm technology to the best of our knowledge. The output can vary from 20nA to 33nA for current reference and from 0.71V to 1.03V for voltage reference.**

I. INTRODUCTION

Recnetly, implantable neural interface systems have been extensively developed to enhance the understanding of neuroscience and enable the disabled to interact with external devices [1-3]. In these implantable systems, many functional blocks such as preamplifier, programmable gain amplifier, filters and ADCs are embedded inside the circuit. To ensure a stable and robust operation of these blocks, it is critical to implement an integrated reference generator to supply stable voltages and currents. This on-chip reference block can miniaturize the overall system volume by eliminating required bonding pads and any external components.

An integrated monolithic reference generator for wireless implantable system requires low power, low voltage operation, and wide input range with reliable tolerance for the variations in supply voltage, process, and temperature. Especially, for the wirelessly powered systems, the variation from supply voltage should be effectively rejected due to its huge fluctuation. On the other hand, the temperature dependency is less critical in the implantable system due to the homeothermy of the human or animal body. Programmability of the reference generator can provide multiple reference outputs for various applications as well as compensate for possible variations in device performance. In addition, to minimize the overall system volume, it is crucial to implement the reference generator in a small area and to provide both reference voltages and currents simultaneously.

Previously, low-power low-voltage references have been proposed and implemented using the subthreshold operating MOSFETs [4, 5] and beta multiplier [6, 7]. Extreme low-power voltage references [8, 9] and current references [10, 11] have been reported. However, these reference generators are not optimized for wireless implantable systems where the power is wirelessly transmitted through inductive coupling in which power supply dependency and the implementation area should be minimized.

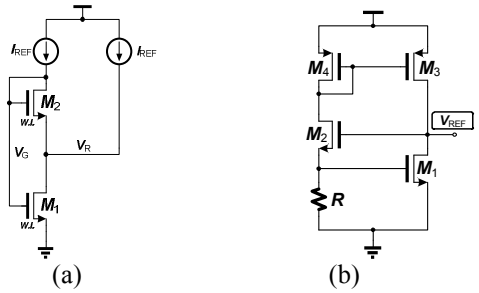

Fig 1. Conventional reference generator: (a) PTAT voltage generator using self-cascode MOSFETs, (b) V_{GS}-based voltage reference.

In this paper, we propose and implement a 1.5V 120nW programmable monolithic CMOS reference generator for wireless implantable system. The proposed generator is optimized to be tolerable for power supply variation in a small area with the programmability to generate various reference voltages and currents. This reference generator is based on self-cascode MOSFET and beta multiplier, and can operate for the input ranges from 1.5V to 3.5V which is suitable for battery operation. The total implemented area is less than 0.011 mm^2, which is the smallest monolithic reference generator realized in 0.25μm technology to the best of our knowledge.

II. OPERATING PRINCIPLES

A. Design Equations using the EKV model

The operation of the PTAP current generator using

$$I_{D1} = 2I_{D2} \tag{1}$$

$$V_P = \frac{V_G - V_{TH0}}{n} \tag{2}$$

$$I_{S1}\exp\left(\frac{V_P}{U_T}\right)\left[1-\exp\left(\frac{-V_R}{U_T}\right)\right] = 2I_{S2}\exp\left(\frac{V_P}{U_T}\right)\exp\left(\frac{-V_R}{U_T}\right) \tag{3}$$

$$\frac{2S_2}{S_1} = \exp\left(\frac{V_R}{U_T}\right) - 1 \tag{4}$$

$$V_R = U_T \ln\left(1 + 2S_2/S_1\right) \tag{5}$$

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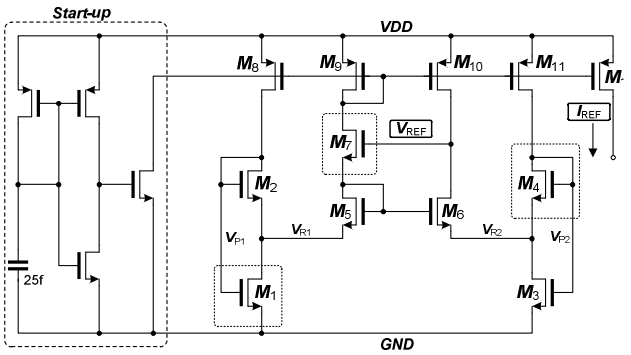

Fig 2. Overall structure of the proposed monolithic reference generator with start-up circuit.

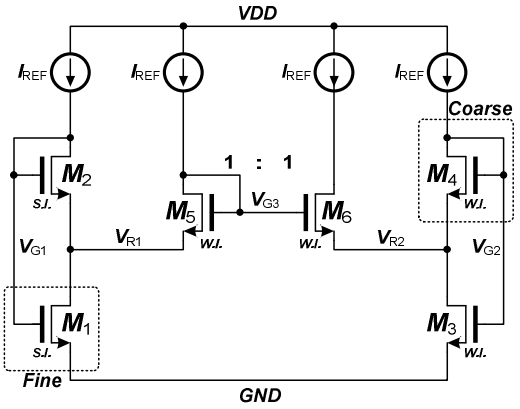

Fig 3. PTAT Reference Current Generator

self-cascode MOSFETs as shown in Fig. 1 (a) can be explained using the EKV model [12]. Due to the self-cascode MOSFET operating in the weak inversion region, the gate voltages of M_1 and M_2 are equal and we can easily derive equation (3). Based on this relationship, we can generate a PTAT reference voltage V_R in equation (5). Using this reference voltage, we can generate a reference current as introduced in [11]

B. Monolithic Voltage/Current Reference Generator

Fig. 2 shows an overall schematic of the proposed reference generator. The reference generator consists of a reference voltage/current generator and a start-up circuit.

1) Reference Current Generation

Reference current can be generated using the self-cascode

$$n\beta_2 (V_P - V_S)^2 = \frac{n\beta_1}{2}\left[{V_P}^2 - (V_P - V_S)^2\right] \tag{6}$$

$$V_{P1} = \frac{\sqrt{1+2S_2/S_1}}{\sqrt{1+2S_2/S_1}-1} V_{R1} \tag{7}$$

$$V_{R1} = V_{R2} = U_T \ln(1+2S_4/S_3) \tag{8}$$

$$I_{REF} = I_{D2} = \frac{n\beta_2 U_T^2}{2}\left(\frac{\ln(1+2S_4/S_3)}{\sqrt{1+2S_2/S_1}-1}\right)^2 = \frac{I_{S2}}{4}\left(\frac{\ln(1+2S_4/S_3)}{\sqrt{1+2S_2/S_1}-1}\right) \tag{9}$$

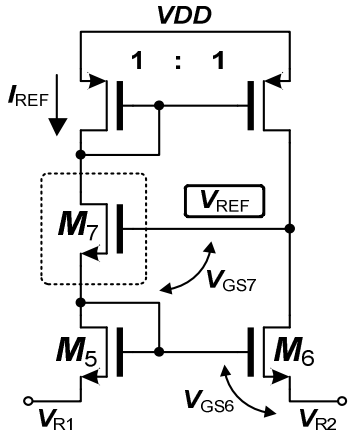

Fig 4. Reference Voltage Generator

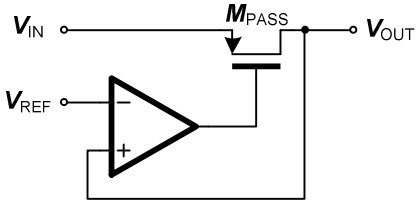

Fig 5. Low-drop-output (LDO) Regulator

MOSFET and the reference voltage generated as shown in equation (5). To minimize the dependency of the reference current on the PTAT reference voltage (V_R), the M_1 and M_2 in Fig. 3 are operated in strong inversion region. The PTAT reference current can be expressed through equation (6-9). Equation (9) implies that the output is a PTAT current reference and can be determined by the size of the transistors ($M_{1\text{-}4}$).

2) Reference Voltage Generation

The reference voltage generator is based on the beta-multiplier. Instead of using an area-consuming resistor (Fig. 1 (b)), V_R from equation (5) is utilized again to generate V_{GS}-referenced voltage as shown in Fig. 4. The reference voltage can be express through the equation (10-12).

$$V_{REF} = V_{R2} + V_{GS6} + V_{GS7} \tag{10}$$

$$V_{GS,SI} = V_{TH} + \sqrt{\frac{2I_D}{n\beta}} \tag{11}$$

$$V_{REF} = V_{TH6} + V_{TH7} + U_T \ln(1+2S_4/S_3) + U_T \ln(IC_6) + \sqrt{\frac{2I_D}{n\beta}} \tag{12}$$

As shown in equation (12), the generated voltage is a combination of the negative temperature coefficient of the threshold voltages and the positive temperature coefficient of U_T. By sizing $S_{3,4}$ properly, we can achieve a zero temperature coefficient voltage reference.

3) Digital Programmability

The proposed generator can be programmed using digital control signals to provide multiple outputs as well as to

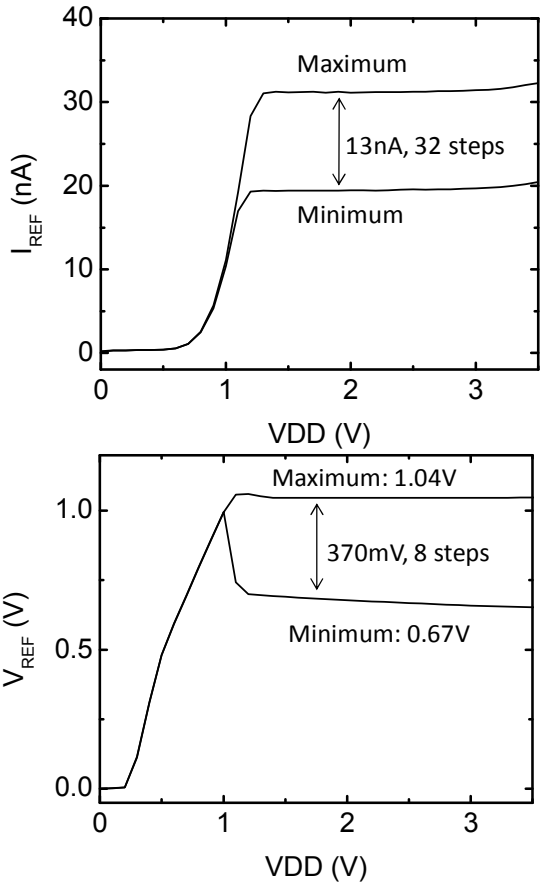

Fig 6: Reference variation as a function of power supply voltage variation in the maximum and minimum ranges: (a) current reference and (b) voltage reference.

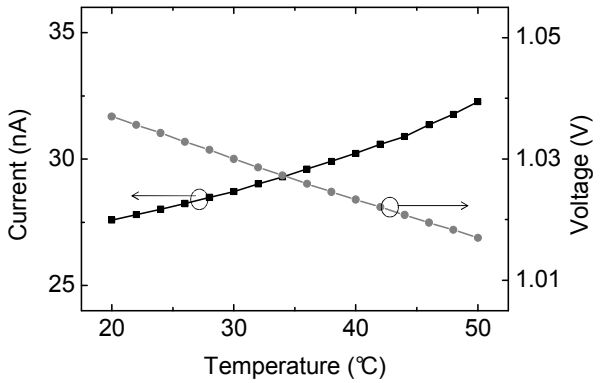

Fig 7: Measured temperature dependency of the reference generator.

compensate any possible variation. By changing the size of the transistors of M_1 and M_4 in Fig. 3, the output current can be controlled. As for the voltage output, we can change the V_{GS} of M_7 by changing the size of the corresponding transistor.

4) Low-drop-out (LDO) Voltage Regulator

In order to supply the functional blocks integrated in the system, the generated output reference voltage can be used to regulate the input voltage to an adequate output voltage level by using a low-drop-output regulator as shown in Fig. 5.

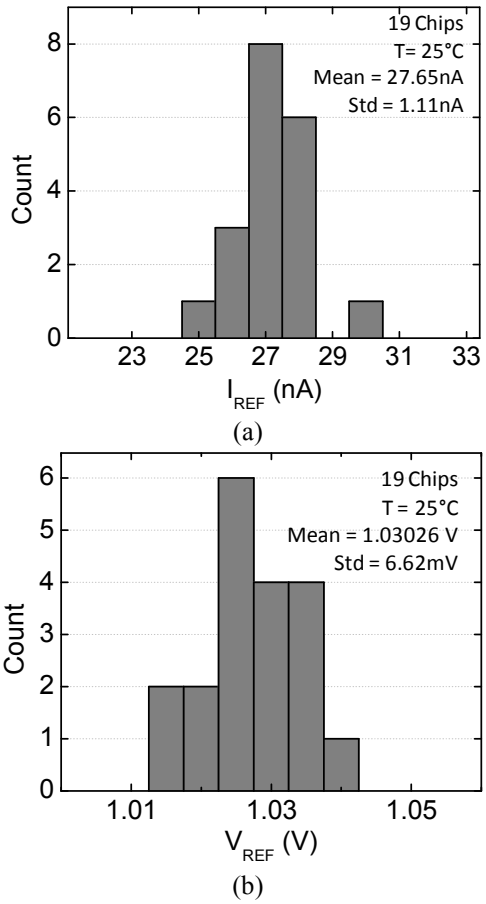

Fig 8: Measured outputs distribution: (a) Current and (b) Voltage

III. Measurement Results

The proposed reference generator is fabricated using 0.25μm 1P5M CMOS process. The overall power consumption is 120 nW (80nA at 1.5V supply). Fig. 6 shows the measured variation of the monolithic reference generator as a function of power supply voltage variation. It shows a line sensitivity of 0.02%/V and 1.1%/V for voltage and current references, respectively at the highest value setting. Fig. 7 shows a temperature dependency of the generator in the range of 20°C ~ 50°C, which is reasonable temperature variation inside the human body. The measured temperature coefficient (TC) is 0.06%/C and 0.4%/C for voltage and current references, respectively. The nineteen chips were tested and the measured offset variations of the references are shown in Fig. 8. The output references can be controlled digitally as shown in Fig. 9. The output can vary from 20nA to 33nA for the current reference, and from 0.71V to 1.03V for the voltage reference, respectively. The measured power supply rejection ratio of the proposed reference generator shows < -50dB at 100 Hz (Fig. 10). The performance of the proposed reference generator is summarized in Table I. The microphotograph of the chip is shown in Fig 11.

IV. Conclusion

In this paper, we report the design and implementation of a low-power low-voltage programmable monolithic CMOS

		This Work	[4]	[9]	[10]	[11]
Technology		0.25 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	1.5 µm CMOS
Temperature Range		20 ~ 50°C	-20 ~ 80°C	0 ~ 80°C	0 ~ 100°C	-20 ~ 70°C
Input Range		1.5 ~ 3.5V	1.4 ~ 3V	0.9 ~ 4V	1 V	1.1 ~ 3V
Reference Type		V / I	V	V	V / I	V / I
Power		120 nW	300 nW	40 nW (@0.9V)	83 µW	2 nW
Line Sensitivity	V	0.02%/V	0.002%/V	0.27%/V	-	1.3 %/V
	I	1.1%/V	-	-	-	6.0 %/V
Temperature Coefficient	V	627 ppm/°C	15 ppm/°C	10 ppm/°C	125 ppm/°C	-
	I	4233 ppm/°C	-	-	185 ppm/°C	2500 %/°C
Reference Output	V	0.71 ~ 1.03V (8steps)	745 mV	670 mV	595 mV	< 100mV
	I	20n ~ 33nA (32steps)	-	-	144 µA	0.4nA
Programmability		Yes	No	No	No	No
PSRR		-51 dB at 100Hz	-45 dB@100Hz	-47 dB@100Hz	-27 dB@10kHz	-
Area		0.011mm²	0.055 mm²	0.045 mm²	0.2 mm²	0.046 mm²

Table I: Performance and comparison

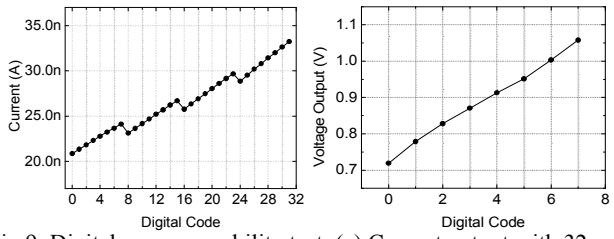

Fig 9. Digital programmability test: (a) Current output with 32 steps and (b) voltage output with 8 steps

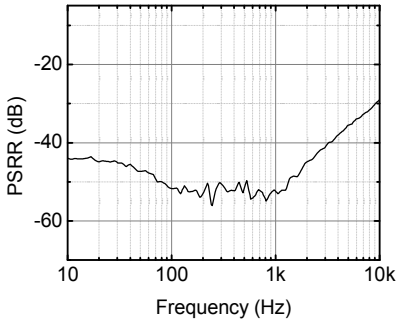

Fig 10: The measured power supply rejection ratio (PSRR)

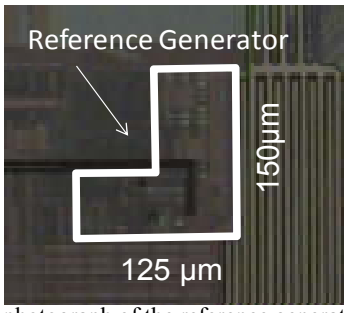

Fig 11: Microphotograph of the reference generator

reference generator in 0.25 µm technology. The fabricated reference generator can operate for input voltage range from 1.5V to 3.5V, which is suitable for battery operation in wireless implantable microsystem. The implemented area is less than 0.011 mm^2, which is the smallest monolithic reference generator in 0.25µm technology to the best of our knowledge. Due to the programmability, the implemented reference generator can provide multiple output levels as well as compensate any possible variations in device performance.

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