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Achievable Peak Electrode Voltage Reduction by Neurostimulators Using Descending Staircase Currents to Deliver Charge

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***Abstract*— This paper considers the achievable reduction in peak voltage across two driving terminals of an RC circuit when delivering charge using a stepped current waveform, comprising a chosen number of steps of equal duration, compared with using a constant current over the total duration. This work has application to the design of neurostimulators giving reduced peak electrode voltage when delivering a given electric charge over a given time duration. Exact solutions for the greatest possible peak voltage reduction using two and three steps are given. Furthermore, it is shown that the achievable peak voltage reduction, for any given number of steps is identical for simple series RC circuits and parallel RC circuits, for appropriate different values of RC. It is conjectured that the maximum peak voltage reduction cannot be improved using a more complicated RC circuit.**

I. INTRODUCTION

Medical devices such as retinal prostheses, for a recent example see [1] and cochlear implants providing electric stimulation of nerves generally use charge-balanced rectangular biphasic current pulses for neural stimulation. Such pulses comprise a constant current stimulating cathodic (negative) phase followed by an interphase gap and a constant current charge-balancing anodic (positive) phase, with the stimulation intensity often considered to correspond with the amount of charge in the stimulation phase.

Recent work [2], [3] has proposed reducing the peak electrode voltage by using regularly sampled stepped current signals for the stimulation phase. The current steps are calculated to minimize the peak electrode voltage while delivering a specified charge over a given number of time steps. Reducing the peak electrode voltage can reduce power consumption, reduce stimulator voltage compliance requirements, and allow more charge delivery without undesirable products forming at the electrodes. The technique is illustrated in Fig. 1 for the simplest case of two current steps. Dividing the total duration into a larger number of steps gives more voltage reduction. For convenience, the stimulation phase is shown as positive in this work. An RC circuit [4] in Fig. 2a was used to model the voltage $\sim$ current relationship between a pair of electrodes in tissue. The circuit model shown in Fig. 2b has been used [5] in the design of a power-efficient neurostimulator.

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Results based on simulation [2] using the RC circuit in Fig. 2a as a model for the electrode-tissue interface, and on *in vitro* saline and *in vivo* tests [3] suggest a peak voltage reduction of $10-20\%$ can be achieved through the approach in that work. This paper tries to analyze the amount of peak voltage reduction that is possible with any RC circuit and to characterize the circuit which gives the best reduction.

The work clarifies the relation between the maximum achievable peak voltage reduction and the number of current steps, the time constants of RC circuits and the sampling interval. For brevity, many results are given without proof.

II. PROBLEM FORMULATION

A. Notation

Voltages and currents which are functions of time t are denoted by lower case letters such as $v(t)$. Samples of $v(t)$ taken at time intervals $t = kT_s$ where $k = 0, 1, 2, \dots$ are denoted v_k, shorthand for $v(kT_s)$. The z-transform of a sequence $h = \{h_k\}_{k=0}^{\infty}$ is denoted $\hat{h}(z)$ and is given by

$$\hat{h}(z) = \sum_{k=0}^{\infty} h_k z^{-k}. \tag{1}$$

With this convention, a stable transfer function has all its poles at values of $z : |z| < 1$. Also the symbol z^{-1} denotes the unit delay. The polynomial comprising the first n terms of $\hat{h}(z)$ is denoted by $\hat{h}^{[n]}(z)$ and is given by

$$\hat{h}^{[n]}(z) = \sum_{k=0}^{n-1} h_k z^{-k}. \tag{2}$$

B. Stepped Stimulation Current Waveform Design

This subsection, based on [2], [3] briefly describes how to obtain the piecewise constant stimulating current which minimizes the peak sampled electrode voltage, given a model of the electrode-tissue interface. As in [2], [3], the stimulation current phase of duration T is parametrized to comprise n steps, each of duration $T_s = T/n$ as follows

$$i(t) = \begin{cases} 0; & t \le 0, \\ i_k; & kT_s < t \le (k+1)T_s;\ k = 0, 1, ..., n-1, \\ 0; & t > nT_s. \end{cases} \tag{3}$$

and is represented by a polynomial $\hat{\imath}(z) = \sum_{k=0}^{n-1} i_k z^{-k}$. The charge Q of the stimulation phase is incorporated by setting

$$\sum_{k=0}^{n-1} i_k = \frac{Q}{T_s}. \tag{4}$$

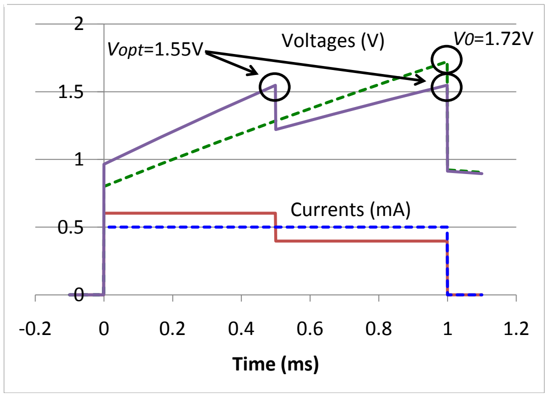

Fig. 1: Simulated voltage and current waveforms for a constant current stimulation phase (dashed lines) and for an optimal two-step descending staircase current (solid lines) giving reduction of the peak voltage from V_0 to V_{opt}, while delivering identical charge over the same total duration.

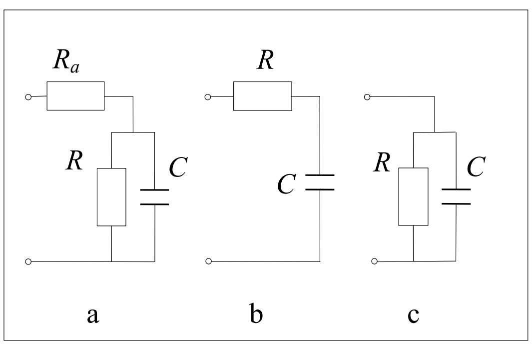

Fig. 2: RC circuits arising in this work; a: series-parallel circuit; b: series circuit; c: parallel circuit.

The impedance of the electrode-tissue interface is modelled by a transfer function $z^{-1}\hat{h}(z) = z^{-1}\sum_{k=0}^{\infty} h_k z^{-k}$ where h_k is the electrode voltage at time $t = (k+1)T_s$ in response to a unit step current applied over one sample time $0 < t \leq T_s$. Then the sampled electrode voltage in response to a current (3) is $\hat{v}(z) = \sum_{k=0}^{\infty} v_k z^{-k}$ where

$$\hat{v}(z) = z^{-1}\hat{h}(z)\hat{\imath}(z). \tag{5}$$

Given n, $\hat{h}^{[n]}(z)$ and Q, the design of $\hat{\imath}(z)$ can be formulated as a linear program and solved numerically. Alternatively, providing the coefficients of $\hat{h}(z)$ satisfy a monotonicity condition,

$$h_0 > h_1 \geq \cdots \geq h_{n-1} \geq h_n \geq \cdots \geq 0, \tag{6}$$
$$h_{n-1} > 0, \tag{7}$$

then the peak sampled voltage is minimized by choosing the current to satisfy (4) and to give $v_1 = v_2 = \cdots = v_n$. We say $\hat{h}(z) \in \mathcal{H}_{Mon}$ if and only if (6) and (7) hold.

It is useful to introduce signal $\hat{x}(z)$ given by

$$\hat{x}(z) = \frac{1}{(1-z^{-1})\,\hat{h}(z)} \tag{8}$$

which for $n \geq 1$ and $\hat{h}(z) \in \mathcal{H}_{Mon}$ satisfies

$$\hat{x}^{[n]}(z)\hat{h}(z) = \sum_{i=0}^{n-1} z^{-i} + z^{-n}\hat{s}(z) \tag{9}$$

where $\hat{s}(z) = \sum_{i=0}^{\infty} s_i z^{-i}$ with $1 > s_0 \geq s_1 \geq \cdots \geq 0$. Polynomial $\hat{x}^{[n]}(z)$ can be understood as the current which maximizes the delivered charge while the peak sampled electrode voltage does not exceed one volt. The coefficients of $\hat{x}^{[n]}(z)$ can easily be found by solving a triangular set of linear equations formed by equating like powers of z from zero to $-(n-1)$ in (9). The desired optimal current $\hat{\imath}_{opt}(z)$ which satisfies the charge constraint (4) is then given by

$$\hat{\imath}_{opt}(z) = \frac{Q}{T_s}\frac{\hat{x}^{[n]}(z)}{\hat{x}^{[n]}(1)}. \tag{10}$$

The corresponding minimized peak sampled voltage, V_{opt}, is

$$V_{opt} = \frac{Q}{T_s \hat{x}^{[n]}(1)}. \tag{11}$$

The example in Fig. 1 is for $n = 2$.

III. Results

This section contains results on the problem of determining the transfer function $\hat{h}(z)$ for which the greatest peak voltage reduction is possible.

A. Parametrization of $\hat{h}(z)$

While the monotonicity condition is sufficient to allow direct calculation of $\hat{\imath}_{opt}(z)$ without solving a numerical optimization, further restriction of the impedance TF is necessary to disallow certain unrealistic $\hat{h}(z)$ which can arise.

Define $\mathcal{H}_{RC}$ to be the set such that

$$\hat{h}(z) \in \mathcal{H}_{RC} \quad \Leftrightarrow \quad \hat{h}(z) = r_0 + \sum_{j=1}^{m} \frac{r_j}{1 - p_j z^{-1}} \tag{12}$$
$$\text{and} \qquad \hat{h}(z) \neq \frac{r_1}{1-z^{-1}},\ \hat{h}(z) \neq r_0 \tag{13}$$

for some finite integer $m \geq 1$ with all $r_j \geq 0$ and $0 < p_1 < p_2 < \cdots < p_m \leq 1$.

Then, since $\mathcal{H}_{RC} \subset \mathcal{H}_{Mon}$,

$$\hat{h}(z) \in \mathcal{H}_{RC} \Rightarrow \hat{h}(z) \in \mathcal{H}_{Mon}. \tag{14}$$

Also, it can be shown from (8)

$$\hat{h}(z) \in \mathcal{H}_{RC} \Rightarrow \hat{x}(z) \in \mathcal{H}_{RC}. \tag{15}$$

Thus for $\hat{h}(z) \in \mathcal{H}_{RC}$, the optimal current waveforms can be described as “descending staircases”.

Simple series RC circuits (Fig. 2b) and parallel RC circuits (Fig. 2c) arise in this work and it is useful to present the relation between the continuous-time parameters R, C, T_s and the coefficients of $\hat{h}(z)$. For a simple series RC circuit

$$\hat{h}(z) = R + \frac{\frac{T_s}{C}}{1 - z^{-1}} \tag{16}$$

so that

$$\frac{T_s}{RC} = \frac{h_1}{h_0 - h_1}. \tag{17}$$

For a simple parallel RC circuit

$$\hat{h}(z) = \frac{R\,(1 - p_1)}{1 - p_1 z^{-1}} \tag{18}$$

where $p_1 = e^{-\frac{T_s}{RC}}$ so that

$$\frac{T_s}{RC} = \ln\left(\frac{h_0}{h_1}\right). \tag{19}$$

B. Figure of Merit M

A figure of merit M that we would like to be as large as possible, and which indicates the amount of peak voltage reduction using a regularly sampled stepped current compared with a constant current stimulation phase is given by

$$M(\hat{h}(z), n) = \frac{V_0}{V_{opt}}, \tag{20}$$

where V_0 is the peak voltage due to a constant current stimulation phase delivering charge Q over duration nT_s and is given by

$$V_0 = \frac{Q}{nT_s}\sum_{i=0}^{n-1} h_i \tag{21}$$

and V_{opt} is the minimized peak voltage from (11). Clearly $M \geq 1$ and the reduction in peak voltage ΔV is

$$\Delta V = V_0 - V_{opt} = \frac{(M-1)\,V_0}{M}. \tag{22}$$

M has the following properties

1) Effect of Scaling $\hat{h}(z)$: For any $\hat{h}(z) \in \mathcal{H}_{Mon}$ and for any $c > 0$, we have

$$M(c\hat{h}(z), n) = M(\hat{h}(z), n). \tag{23}$$

2) Useful Expression for M:

$$M(\hat{h}(z), n) = \frac{\hat{h}^{[n]}(1)\hat{x}^{[n]}(1)}{n} \tag{24}$$

obtained by substituting (21) and (11) into (20).

This paper is concerned with the maximization of M with respect to $\hat{h}(z) \in \mathcal{H}_{RC}$. For given $n \in \{1, 2, 3, \ldots\}$, define the optimal value of M as follows.

Definition 1:

$$M_n^* = \max_{\hat{h}(z)\in\mathcal{H}_{RC}} M\left(\hat{h}(z), n\right) \tag{25}$$

The optimizing $\hat{h}^{[n]}(z)$ is defined as follows.

Definition 2:

$$\hat{h}^{[n]*}(z) = \underset{\hat{h}^{[n]}(z):\hat{h}(z)\in\mathcal{H}_{RC}}{\arg\max} M\left(\hat{h}(z), n\right) \tag{26}$$

C. Greatest peak voltage reduction for $n = 2$

Theorem 1: The maximum value of M_2 with $\hat{h}(z) \in \mathcal{H}_{RC}$ is

$$M_2^* = \frac{9}{8} \tag{27}$$

obtained with

$$\hat{h}^{[2]*}(z) = c\left(1 + \frac{1}{2}z^{-1}\right) \tag{28}$$

for any $c > 0$.

Proof: Set $\hat{h}^{[2]}(z) = 1 + h_1 z^{-1}$ where $0 < h_1 < 1$. Then, from (9), $\hat{x}^{[2]}(z) = 1 + (1 - h_1)\,z^{-1}$. Next using (24)

$$M = \frac{(1 + h_1)\,(2 - h_1)}{2}. \tag{29}$$

Setting the derivative with respect to h_1 to zero yields that M has a maximum value of $9/8$ at $h_1 = 1/2$. ■

With $M = 9/8$, $\Delta V = V_0/9$. The result above for $n = 2$ has several properties which do not hold for all values of n.

Firstly, $M_2^* = \max_{\hat{h}(z)\in\mathcal{H}_{Mon}} M\left(\hat{h}(z), 2\right)$.

Secondly $\hat{h}^{[2]*}(z)$ is proportional to $\hat{\imath}_{opt}(z)$.

Thirdly, many $\hat{h}(z) \in \mathcal{H}_{RC}$ can be found for which $\hat{h}^{[2]}(z) = \hat{h}^{[2]*}(z)$. Examples include

$$\hat{h}(z) = \frac{1}{1 - (1/2)z^{-1}}, \tag{30}$$

$$\frac{1}{3} + \frac{2/3}{1 - (3/4)z^{-1}}, \tag{31}$$

$$\frac{1}{2} + \frac{1/2}{1 - z^{-1}}, \tag{32}$$

$$\frac{1/2}{1 - (3/10)z^{-1}} + \frac{1/2}{1 - (7/10)z^{-1}}. \tag{33}$$

Equation (30) is the transfer function of a simple parallel RC circuit; (31) is for a series-parallel RC circuit and (32) is for a series RC circuit.

Using (19) the relation between T_s, R and C for the optimal parallel circuit for $n = 2$ is

$$\frac{T_s}{RC} = \ln\left(\frac{h_0}{h_1}\right) = \ln 2 \approx 0.693. \tag{34}$$

The corresponding relation for the optimal series circuit for $n = 2$ (32) is, using (17),

$$\frac{T_s}{RC} = \frac{h_1}{h_0 - h_1} = 1. \tag{35}$$

Thus the values of T_s/RC which maximize M_2 are different for the series and parallel circuits.

D. Greatest peak voltage reduction for $n = 3$

This problem is rather more difficult than that for $n = 2$. Applying the technique used above gives

$$\hat{h}(z) = c\left(1 + (1/2)z^{-1} + (3/8)z^{-2}\right), \tag{36}$$

$$\hat{x}(z) = 1/c\left(1 + (1/2)z^{-1} + (3/8)z^{-2}\right) \tag{37}$$

with $M = 75/64 \approx 1.17188$, but this is a saddle point, not a maximum. On the other hand optimizing over $\hat{h}(z) \in \mathcal{H}_{Mon}$ using

$$\hat{h}(z) = 1 + (1 - \epsilon)z^{-1} + \epsilon z^{-2} \tag{38}$$

gives

$$\hat{x}(z) = 1 + \epsilon z^{-1} + (1-\epsilon)^2 z^{-2}. \tag{39}$$

For small positive ϵ, $\hat{h}(z) \in \mathcal{H}_{Mon}$ but $\hat{h}(z) \notin \mathcal{H}_{RC}$ and $\hat{x}(z) \notin \mathcal{H}_{Mon}$. The corresponding M is $M = 4/3 - 2/3\epsilon + 2/3\epsilon^2$ so $lim_{\epsilon\to 0} M = 4/3$. The sought value of M lies between these values and is given next.

Theorem 2: The maximum value of M_3 with $\hat{h}(z) \in \mathcal{H}_{RC}$ is

$$M_3^* = \frac{172 + 7\sqrt{7}}{162} \approx 1.17605 \tag{40}$$

obtained with

$$\hat{h}^{[3]}(z) = c\left(1 + \frac{(1+\sqrt{7})}{6} z^{-1} + \frac{\left(1+\sqrt{7}\right)^2}{36} z^{-2}\right) \tag{41}$$

$$\text{or} \quad c\left(1 + \frac{5-\sqrt{7}}{6} z^{-1} + \frac{5-\sqrt{7}}{6} z^{-2}\right) \tag{42}$$

for any $c > 0$.

With $M = M_3^*$, $\Delta V \approx 0.15 V_0$. The only corresponding $\hat{h}(z) \in \mathcal{H}_{RC}$ are

$$\hat{h}(z) = \frac{c}{\left(1 - \frac{(1+\sqrt{7})}{6} z^{-1}\right)}, \tag{43}$$

$$\text{and} \quad c\left(1 + \frac{\frac{5-\sqrt{7}}{6} z^{-1}}{1 - z^{-1}}\right). \tag{44}$$

Equation (43) is for a parallel circuit with,

$$\frac{T_s}{RC} = \ln\left(\frac{1}{\frac{1+\sqrt{7}}{6}}\right) \approx 0.498. \tag{45}$$

Equation (44) is for a series circuit with,

$$\frac{T_s}{RC} = \sqrt{7} - 2 \approx 0.646. \tag{46}$$

Thus, not only are the values of T_s/RC which maximize M_3 different for the series and parallel circuits, but also the values of T/RC which maximize M_2 and M_3 for each circuit configuration are different.

E. Simple series and parallel circuits

With $\hat{h}(z)$ a parallel RC circuit as in (18), (8) gives

$$\hat{x}(z) = 1 + \frac{z^{-1}(1-p_1)}{1 - z^{-1}}, \tag{47}$$

which has the form of a series RC transfer function as in (16). Since the value of M is symmetric in $\hat{h}^{[n]}(1)$ and $\hat{x}^{[n]}(1)$ by (24), it follows that for any given integer $n > 1$, the achievable set of values of M for series RC circuits and parallel RC circuits are the same. Of particular interest, the maximum value of M achievable for given $n > 1$ is the same for a series or parallel circuit. These identical values of M including maxima are attained at different values of RC according to the circuit configuration.

TABLE I: Values of greatest reduction of peak electrode voltage for a simple series or parallel RC circuit.

n	M_n	$\Delta V/V_0$ (%)
1	1	0
2	9/8	11.11
3	1.17605	15.00
4	1.20386	16.93
5	1.22136	18.12
10	1.25839	20.53
20	1.27801	21.75
50	1.29016	22.49
100	1.29427	22.74
200	1.29635	22.86

The maximization of M for a simple series or parallel RC circuit is considered next. Substituting (18) and (47) into (24), gives

$$M_n = \frac{1}{n}\left(n + \sum_{j=1}^{n-1} p_1^j - (n-1)p_1^n\right). \tag{48}$$

It can be shown that this polynomial expression in p_1 has exactly one maximum in the interval $p_1 \in (0,1)$. This can be found numerically for given n and is tabulated in Table I. We conjecture that the values of M_n cannot be further maximised with a more complicated RC circuit.

IV. Conclusions

The achievable reduction in peak voltage using a regularly sampled stepped current, compared with a fixed current, to deliver a given charge over a given duration into an RC circuit has been investigated. For two-step currents, the best achievable reduction is found to be $V_0/9$ where V_0 is the peak voltage obtained with a fixed current and this can be achieved using many different RC circuits including series-parallel, series and parallel RC circuits. For three-step currents, the best reduction is $0.15V_0$ achieved only with simple series or parallel RC circuits. For any finite number of steps, the achievable voltage reduction using a series RC circuit and a parallel RC circuit are identical, but using different RC values. This work contributes to an understanding of the limitations in achievable peak voltage reduction to be obtained driving an RC circuit with a descending staircase current waveform and has application to the performance achieved by neurostimulators using such waveforms.

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