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Analytical Design Equations for Self-tuned Class-E Power Amplifier

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***Abstract*— For many emerging neural prosthesis designs that are powered by inductive coupling, their small physical size requires large current in the extracorporeal transmitter coil, and the Class-E power amplifier topology is often used for the transmitter design. Tuning of Class-E circuits for efficient operation is difficult and a self-tuned circuit can facilitate the tuning. The coil current is sensed and used to tune the switching of the transistor switch in the Class-E circuit in order to maintain its high-efficiency operation. Although mathematically complex, the analysis and design procedure for the self-tuned Class-E circuit can be simplified due to the current feedback control, which makes the phase angle between the switching pulse and the coil current predetermined. In this paper explicit analytical design equations are derived and a detailed design procedure is presented and compared with the conventional Class-E design approaches.**

I. Introduction

The Class-E power amplifier circuit topology (as shown in Fig. 1) was first described by N. O. Sokal and A. D. Sokal [1]. It has been widely used in applications such as radio transmitters, dc-dc converters. Troyk and Schwan [2] adapted this original technology to provide power and data communication between the transcutaneous implants and the external controller. In their approach, the coil current $i_p(t)$ is sensed and used to automatically tune the Class-E circuit for high-efficiency operation. Exemplary of applications requiring extremely high transmitter coil currents is the recently described implanted myoelectric sensor (IMES) devices [3] which utilize this transmitter technology.

Most often the Class-E circuit is analyzed using a 50% switch duty cycle. However, to design for a self-tuned Class-E circuit, one can not simply apply the conventional 50% duty cycle Class-E design equations. In fact, as pointed out by F. H. Raab [4], the high-efficiency operation of the Class-E circuit is not dependent on that.

F. H. Raab gave an extensive analysis of the Class-E circuit for ideal [4] and non-ideal [5] operations. He started from the voltage on the coil resistor R. Other researchers [6], [7], [8] chose to use the coil current $i_p(t)$ as the starting point. In either case, the current through the shunt capacitor C_{shunt} can be defined as:

$$i_s(t) = i_{\text{dc}} + i_p \sin(\omega t + \phi) \tag{1}$$

Because the phase angle ϕ in (1) is unknown, the analytical derivation [8] for the variables such as $i_p(t)$ and i_{dc} can become very convoluted and unsuitable for a practical circuit design procedure.

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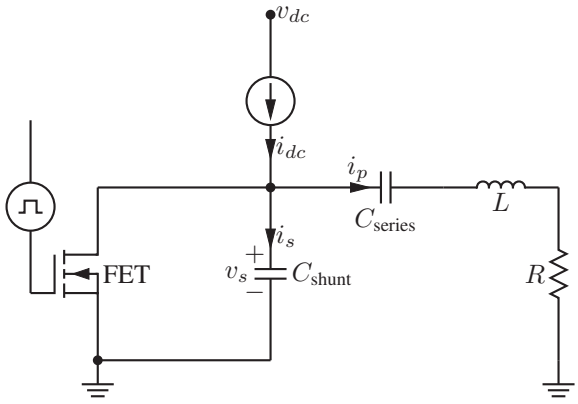

Fig. 1. Class-E Circuit Diagram

In the following discussion, we use i_p to represent the peak value of the coil current $i_p(t)$ as indicated by equation (1). $v_s(t)$ is used to represent both the shunt capacitor voltage and the voltage across the FET switch, as shown in Fig. 1.

As indicated by Raab's analysis, one can apply the high-efficiency operation conditions for Class-E circuits:

- When the FET switch turns on, there is zero voltage on the shunt capacitor C_{shunt}
- When the FET switch turns on, the derivative of $v_s(t)$ is also zero

One can simplify the formulas, using the current ratio α

$$\frac{i_{\text{dc}}}{i_p} = \alpha$$

$$\cos(\phi) = \frac{\alpha y}{\sin(y)} \tag{2}$$

$$\tan(\phi) = \cot(y) - \frac{1}{y} \tag{3}$$

The variable y determines the FET switching duty cycle (as defined by Raab [4]). By setting $y = \pi/2$ in (2) and (3), which corresponds to 50% duty cycle, it simplifies the relationship between the phase angle ϕ and the current ratio α. However, one can also eliminate the phase angle from the above equations and reach an equation between the current ratio α and the duty cycle y directly.

$$\frac{\sqrt{1 - \left(\frac{\alpha y}{\sin(y)}\right)^2}}{\frac{\alpha y}{\sin(y)}} = \pm\left(\cot(y) - \frac{1}{y}\right) \tag{4}$$

Equation (4) indicates that for each current ratio α, one can solve for a duty cycle y such that the Class-E circuit operates at the high-efficiency point.

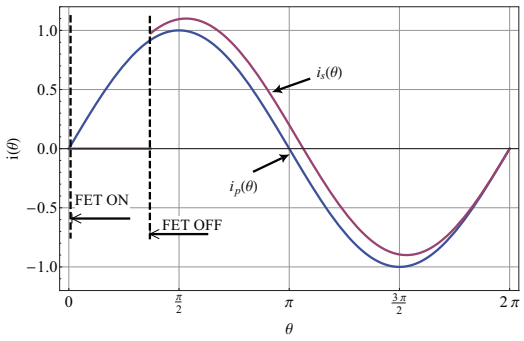

Fig. 2. Self-tuned Class-E Circuit Current Waveforms

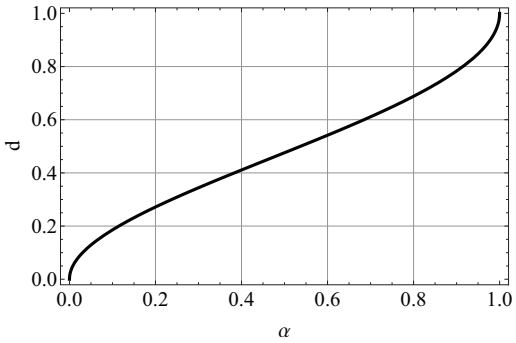

Fig. 3. Current Ratio and Duty Cycle for Class-E High-efficiency Operation

Owing to the high circuit quality factor, the self-tuned Class-E circuit turns on the FET switch when the sinusoidal coil current $i_p(t)$ is at its positive zero-crossing point. It eliminates the need to determine the phase angle ϕ completely. The design objective is to find the values of the circuit elements such that when the FET switch turns on, both $i_s(t)$ and $v_s(t)$ equal zero. Because of the $i_s(t) = c \cdot dv_s(t)/dt$ relationships of the shunt capacitor voltage and current, the self-tuned Class-E circuit operates at the high-efficiency point by design (i.e. zero switching voltage and zero derivative of the switching voltage).

Given a coil with known: L and R, the DC supply voltage v_{dc}, the Class-E circuit operating frequency f, and the peak value of the coil current i_p, one needs to find the values of the series capacitor (C_{series}), the shunt capacitor (C_{shunt}), and the duty cycle (d) such that the Class-E circuit operates with high-efficiency. As shown here, the analysis of the self-tuned Class-E circuit is more concise than the conventional Class-E circuit. A set of explicit design equations can be derived.

II. Self-tuned Class-E Circuit Design Equations

Assuming that the series R-L-C circuit has high enough Q-factor, the coil current $i_p(t)$ is essentially sinusoidal. When the FET switch is off, the current $i_s(t)$ through the shunt capacitor C_{shunt} is the sum of the DC current i_{dc} and the coil current $i_p(t)$ (see Fig. 1). Because the FET switch turns on when $i_p(t)$ crosses zero on the rising zero-crossing, the current $i_s(t)$ can be defined as

$$\frac{i_s(\theta)}{i_p} = \begin{cases} 0 & \text{if } 0 \le \theta \le 2\pi d \\ \alpha + \sin(\theta - \arcsin(\alpha)) & \text{if } 2\pi d \le \theta \le 2\pi \end{cases} \quad (5)$$

with $\theta = \omega \cdot t$ and $\alpha = i_{\text{dc}}/i_p$. d defines the duration that the FET switch turns on.

At $\theta = 0$ and 2π, when the FET switch turns on, equation (5) guarantees that $i_s(\theta) = 0$. Comparing with equation (1), the phase angle ϕ is simply $-\arcsin(\alpha)$ in the case of self-tuned Class-E circuit.

Since the average of $i_s(\theta)$ needs to be zero to ensure that zero charge is left on C_{shunt} when the FET switch turns on,

$$\int_{2\pi d}^{2\pi} (\alpha + \sin(\theta - \arcsin(\alpha)))\, d\theta = 0$$

$$2(1-d)\pi\alpha + \cos(2\,\pi d - \arcsin(\alpha)) - \sqrt{1-\alpha^2} = 0 \quad (6)$$

Thus given a current ratio α, equation (6) can be used to solve for the duty cycle d. The derivation is solely based on the Class-E circuit current waveform under high-efficiency operation conditions. Equation (6), equation (4), and equation (5) in [7] look different, but are derived using the same principle.

Fig. 2 shows $i_s(\theta)$ and $i_p(\theta)$ for $\alpha = 0.1$ and $d = 0.186$. Fig. 3 shows the current ratio between 0 and 1, and the corresponding duty cycle for high-efficiency operation of the Class-E circuit.

To find the current ratio α, one can assume that the energy loss in the circuit is solely caused by the sinusoidal current $i_p(t)$ flowing through the resistor R. By balancing the energy feeding into the circuit from the power supply and the energy consumption on the resistor,

$$\frac{i_p^2}{2} \cdot R = i_{\text{dc}} \cdot v_{\text{dc}}$$

$$\alpha = \frac{i_{\text{dc}}}{i_p} = \frac{i_p \cdot R}{2v_{\text{dc}}} \quad (7)$$

In equation (7), v_{dc}, R, and i_p are known design parameters, from which α can be calculated. As shown below, one can add other losses (e.g. FET switch loss) into (7) for more accurate solutions.

Once α and d are determined, C_{shunt} and C_{series} can be solved by examining the shunt capacitor voltage $v_s(t)$.

In the earlier paper [2], Troyk used a parametric function

$$v_s(\theta) = \begin{cases} 0 & \text{if } 0 \le \theta \le 2\pi d \\ A(1 - \cos(\frac{\theta - 2\pi d}{1-d})) & \text{if } 2\pi d \le \theta \le 2\pi \end{cases}$$

to approximate the shunt capacitor voltage. $v_s(\theta)$ goes to zero at $\theta = 0$ and $\theta = 2\pi$, when the FET switch turns on; and it also goes to zero at $\theta = 2\pi d$, when the FET switch turns off. The parameter A is fitted by Fourier series expansion of the expression $v_s(\theta)$.

We choose the more direct expression for $v_s(\theta)$, but the same Fourier series principle to solve for the capacitor values.

When the FET switch is off, the current $i_s(\theta)$ flows through the shunt capacitor C_{shunt}, $v_s(\theta)$ should be the integral of that capacitor current.

$$v_s(\theta) = \frac{1}{\omega C_{\text{shunt}}} \int_{2\pi d}^{\theta} i_s(x)\, dx$$
$$= \begin{cases} 0 & \text{if } 0 \le \theta \le 2\pi d \\ \frac{i_p}{\omega C_{\text{shunt}}}(\alpha(\theta - 2d\pi) & \\ + \cos(2d\pi - \arcsin(\alpha)) & \\ - \cos(\theta - \arcsin(\alpha))) & \text{if } 2\pi d \le \theta \le 2\pi \end{cases}$$

First the average of $v_s(\theta)$ should equal to v_{dc}

$$v_{\text{dc}} = \frac{1}{2\pi} \int_{2\pi d}^{2\pi} v_s(\theta)\, d\theta$$

Thus the explicit equation for C_{shunt} can be derived

$$K = (2\pi^2(d-1)^2 + 1)\alpha$$
$$- 2(d-1)\pi \cos(2d\pi - \arcsin(\alpha))$$
$$+ \sin(2d\pi - \arcsin(\alpha))$$
$$C_{shunt} = \frac{i_p}{v_{\text{dc}} 4\pi^2 f} K \tag{8}$$

Secondly the fundamental frequency component of $v_s(\theta)$ can be used to solve C_{series}. The reactance part of the voltage waveform is defined as

$$-i_p X = \frac{1}{\pi} \int_{2\pi d}^{2\pi} \cos(\phi) v_s(\phi) d\phi$$
$$X = \omega L - \frac{1}{\omega C_{\text{series}}}$$

So the explicit equation for C_{series} is

$$H = 4\pi\sqrt{1-\alpha^2}d + 3\alpha$$
$$- 4\alpha\cos(2d\pi) + \alpha\cos(4d\pi)$$
$$- \sqrt{1-\alpha^2}\sin(4d\pi) - 4\pi\sqrt{1-\alpha^2}$$
$$C_{\text{series}} = \frac{4\pi C_{\text{shunt}}}{H + 16\pi^3 f^2 L C_{\text{shunt}}} \tag{9}$$

Summarizing the design approach, equation (7) and (6) can be used to find the current ratio α and the duty cycle d. Then the shunt capacitance C_{shunt} can be calculated by (8); the series capacitance C_{series} can be calculated by (9).

III. FET Switch Energy Loss

The energy balance equation (7) is used to solve for the current ratio α, assuming that the total power dissipation is solely caused by the resistor R and $i_p(t)$ at the fundamental frequency.

In the Class-E circuit (Fig. 1), the FET switch also conducts the current $i_s(t)$ during $\theta = 0$ to $2d\pi$. Assuming the FET switch has a on-resistor R_{on}, its power loss can be calculated

$$P_{fet} = \frac{1}{2\pi} \int_0^{2d\pi} i_s(\theta)^2 R_{\text{on}} d\theta$$
$$= \frac{R_{\text{on}} i_p^2}{8\pi}(6\alpha\sqrt{1-\alpha^2} + 4d\pi(1+2\alpha^2)$$
$$-8\alpha\sin(2d\pi + \arccos(\alpha))$$
$$+\sin(2(2d\pi + \arccos(\alpha)))) \tag{10}$$

So the new energy balance equation becomes

$$R \cdot \frac{1}{2} i_p^2 + P_{\text{fet}} = i_{\text{dc}} \cdot v_{\text{dc}} \tag{11}$$

In theory, equation (10) can be put into (11) and combined with (6) to solve for the current ratio α and the duty cycle d. In practice, we use the following design procedure:

1) Assume no FET loss and use (6) and (7) to obtain the tentative α and d.
2) Use these two values to calculate P_{fet} by (10).
3) With P_{fet} known, (6) and (11) are then used to solve for the updated current ratio α and duty cycle d.
4) The new α and d are then used in the explicit equations for C_{shunt} (8) and C_{series} (9).

IV. Experimental Results

Functions in *Mathematica* computational environment were defined to calculate the capacitor values in the self-tuned Class-E circuit, based on the explicit design equations presented above.

$$C_{\text{shunt}} = f(i_p, v_{\text{dc}}, \text{freq}, L, \text{Q}, R_{\text{on}})$$
$$C_{\text{series}} = g(i_p, v_{\text{dc}}, \text{freq}, L, \text{Q}, R_{\text{on}}) \tag{12}$$

The physical circuit implementation used a Sigenics 5800 custom Class-E controller chip.

For the test case presented here, the design objective is to have the circuit output $i_p = 2\ A$ peak sinusoidal current at freq $= 470$ kHz in the transmitter coil.

The transmitter coil was wound with Litz wire to have $L = 25\ \mu H$ inductance and estimated $Q = 155$ at the operating frequency. A $v_{\text{dc}} = 5\ V$ DC voltage source in series with a RF choke was used to supply power to the circuit. The FET on-resistance is assumed to be $R_{\text{on}} = 0.04\ \Omega$, according to the data sheet.

The calculated $C_{\text{shunt}} = 104\ nF$ and $C_{\text{series}} = 4.77\ nF$. In the physical circuit, $4.7\ nF$ was used for C_{shunt} and $100\ nF$ was used for C_{series}.

The coil current was measured with a Tektronix AC current probe connected to an oscilloscope. The FET switch voltage was also monitored on the oscilloscope (shown in Fig. 4).

A potentiometer on the circuit board was used to adjust the duty cycle of the switching pulse, such that $v_s(t)$ reached zero when the FET switch turned on. One can also fine tune the Class-E circuit by looking at the i-v curve, i.e. the X-Y display of the coil current vs. the switch voltage on the oscilloscope.

As shown in Fig. 4, when the Class-E circuit is operating at the high-efficiency point:

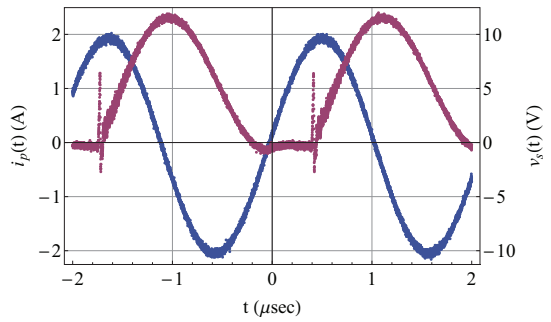

Fig. 4. Switch Voltage and Coil Current Scope Capture

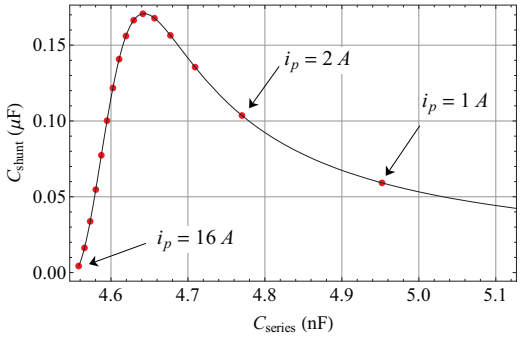

Fig. 5. Parametric Plot of Capacitor Values

- The measured peak coil current reaches our design objective of 2 A.
- The measured coil current frequency is 471 kHz.
- The calculated $i_{dc} = 193\ mA$ and the measured power supply current is 201 mA.
- The calculated switching pulse width $d{\cdot}\text{freq} = 387\ nsec$ and the measured value is 390 $nsec$.

In summary, the calculated values are very close to the measured results.

Assuming high-efficiency operation of the circuit, the power output on the resistor R is

$$P = 2\alpha^2 \frac{v_{dc}^2}{R} \tag{13}$$

So given a coil resistance R, one can determine the maximum peak current, at the expense of current ratio α approaching 1. To see the effect of increasing peak current i_p on the capacitor values, one can perform a numerical experiment: for example, fix all the input parameters in the earlier design functions (12), except for the peak current i_p.

Fig. 5 shows that for a given shunt capacitor value C_{shunt}, there exist two C_{series} values, with significantly different peak currents.

A similar parametric plot can be made for the Class-E frequency, which can be used for designing FSK modulation of the circuit.

V. Conclusions

The design objective for a Class-E circuit used for biomedical implants is often different from the conventional Class-E circuit application, due to the need for extraordinarily large coil currents. In general, the external transmitter/controller needs to drive a predefined inductive link in order to provide power and data communication with the implant.

Earlier design procedures that select the R (in Fig. 1) for 50% duty cycle operation are not relevant. Rather, it is necessary to specify the coil peak current i_p so that sufficient power can be supplied to the implant device, while keeping the current ratio α low enough to save power, especially for battery-powered portable applications. This requires that the Class-E circuit operate in the High-Q high-efficiency mode so that minimal power is wasted on the FET switching.

The self-tuned Class-E circuit is well suited for this purpose. It is easy to implement and tune for high-efficiency operation. As shown in this paper, its analysis and design equations are also concise enough to give the designer both intuitive and numerical results quickly.

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