

Development of a Network FES System for Stroke Rehabilitation

Hongen Qu¹, Ting Wang¹, Manzhao Hao¹, Ping Shi¹, Weifeng Zhang², Guoxing Wang² and Ning Lan¹

Abstract—This paper describes a Functional Electrical Stimulation (FES) system based on the distributed network structure for rehabilitation of stroke patients. This FES system performs surface stimulation to activate the nerve of paretic muscles for training stroke patients to relearn motor functions. The main components of the networked FES system include a master unit (MU), a distributed stimulation-sensor unit (DSSU), and a clinical computer. In this system, the MU can drive a set of DSSUs, which is located at the node on the distributed network structure. The MU also stores the stimulation plan of rehabilitation training prescribed by clinicians. The DSSU serves as a single channel stimulator whose current amplitude, duration and frequency can be modulated by the MU. This system has two distinctive characters. First, since a stimulator is designed as a node on the network, the number of stimulation channels could be expanded according to specific needs. Second, a sensor component can be incorporated in the DSSU to allow monitoring physiological variables. The two features of system design make the networked FES system practical and flexible in clinical applications. We have completed a prototype of system including hardware and software. The evaluation test indicates that the system performance meets design specifications.

Keywords: FES, body area network, wearable devices, stroke, neural rehabilitatio

I. INTRODUCTION

STROKE is caused by blood vehicle rupture or blockage in the brain, which results in damage to cerebral neurons and leads to paresis of motor functions in most survivors. There are more than seven millions of stroke patients in China. Thus, developing training devices that can be deployed for home use will help rehabilitation for a large population of stroke patients. Functional electrical stimulation (FES) is a proven technology for stroke rehabilitation [1-4]. It has been applied to restoring lost motor functions in spinal cord injury patients by directly activating the peripheral nerves that innervate muscles with a low level of electrical current. Electrical stimulation of muscles by surface and implanted electrodes has been developed and implemented successfully in many clinical applications. Clinical studies have been conducted to investigate effective paradigms to reduce motor impairment and restore the mobility with FES [5]. Other studies [6,7]

have reported that stroke patients have shown improved hand opening and close movements after 12 weeks of FES training. But the existing FES systems were mainly designed for specific applications [9]. Some FES systems [8] have also been developed for using with various sensors and stimulators. We aim to develop an FES system that can be flexible with other applications, such as in combined use with robotics [10, 11] and in wearable devices for home use [12, 13].

Our design criteria for a practical FES system include the following features: (I) easy-to-use and reliable, (II) portable for home use in daily life, (III) capable of multi-channel stimulation, and (IV) extendible to include new modality of rehabilitation. In this paper, we present a design of FES system based on distributed body area network that meets the requirements.

II. HARDWARE DESIGN

A. The architecture of the system

To achieve the above features, we have proposed a new architecture of network FES system [14]. In this design (fig.1), the whole system is divided into three parts: (I) the Master Unit (MU) that supervises the whole system operation and decides control methods of stimulation; (II) the communication system with a wired dual bus configuration module and (III) the distributed stimulation and sensor unit (DSSU), which provides stimulation of the neuromuscular system and detection of physiological signals. The DSSU is the most flexible part in the system, and it could be designed for both implantable and surface stimulators. The operation of the networked FES stimulator is shown in Fig.1. The Master Unit sends stimulation parameters to the DSSUs

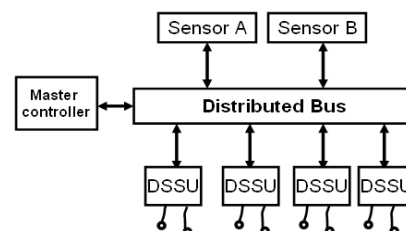


Fig. 1. The architecture of the network FES system.

through a serial bus. Each DSSU acts as one channel of FES stimulation. The DSSUs translate the parameters to the actual stimulation current pulse. After successful transmission of the stimulation parameters, the Master Unit

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sends another command to the DSSUs to execute the stimulation specified by the parameters. For implantable stimulator, the core of the DSSU also includes a module of wireless power transmission and wireless data telemetry, so as to control implanted stimulators and to record physiological signals, such as EMG. In this article, however, we focus on the design and test of the DSSU for surface stimulation, which has a small size, but high and reliable performance. The prototype of the DSSU has been constructed using discrete components. The testing results demonstrated the feasibility of the design. ASIC design of microchip realization is currently under way.

B. The MU Design

The master unit (MU) is the communication and control hub for the network FES system (fig. 2), and has five parts: (I) the LCD that displays the states of system; (II) the CPU controller, which manages the system operation and supervises the state of the system; (III) the keyboard for therapist to set stimulation parameters; (IV) power supply for all the system; and (V) communication protocol that handles communications with the clinic computer and all the DSSUs on the network. In order to fulfill the five tasks and functions with minimum hardware components, we choose the STM32F103ZE as the CPU of the MU, which offers a high speed of data communication rate from DSSU and determines the status of stimulation task at each DSSU at 50Mhz operating frequency. This interface includes two I2Cs, three SPIs, two I2Ss, one SDIO, five USARTs, an USB and a CAN controller.

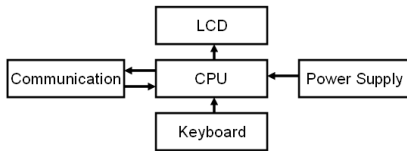


Fig. 2. The core of MU.

C. The Architecture Design of DSSU

The architecture of DSSU is shown in Fig.3. Its core includes the basic modules of stimulator function: (I) a DC-DC boost converter, which steps up the low battery voltage to the high voltage required for stimulation, (II) communication module, which receives control signal and

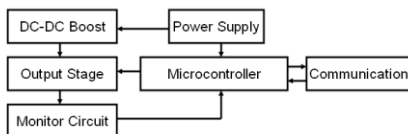


Fig. 3. The core of the DSSU.

sends status data of DSSU to master unit, (III) the output module that produces a bipolar programming current with DAC, and (IV) monitoring circuit, which supervises the

operating status. Our design mainly focuses on the DC-DC boost circuit module, output stage module, and monitor circuit module. They are the most crucial modules to achieve the high performance of design specification. The design concepts of these modules are presented in the following.

1) *DC-DC boost circuit design*: in the surface stimulation system, the required current of stimulation may range from 1mA to 100mA, which is usually much larger than that of the implant stimulator. Assume that the electrical resistance between skin and nerve is about $1K\Omega$ to $2K\Omega$. Thus, the voltage needed for stimulation can go up to 200V ($100mA \times 2K\Omega$). However, the safe limit of voltage in the body network is 36V in patients. In our design, the power supply of the bus is chosen to be 12V, and a DC-DC converter is used to boost the voltage of local power supply at each DSSU to about 100V. The traditional booster circuit often uses a step-up transformer to convert the low DC voltage to the high voltage. The step-up transformer occupies a large area and is often heavy. To meet our requirement, we have designed a light DC-DC boost converter for our system. It uses an inductor-capacitor charging circuit to achieve voltage elevation. The circuit is small in size and light in weight, and can be used in a portable system. The boost converter operates in the discontinuous mode, under which the boost converter follows the formula as

$$\frac{V_{out}}{V_{in}} = 1 + \frac{V_{in} D^2 T}{2LI_{out}} \quad (1)$$

The design parameters for the booster circuit are: $V_{out}=100V$, $V_{in}=12V$, $I_{out}=150mA$, $D=50\%$,

$$T = \frac{1}{f} = \frac{1}{50000}, L \geq 300mH.$$

2) *Design of output stage*: The current output stage is an H-bridge circuit that has four switches (S1-S4) and two Voltage Controlled Current Sources (VCCS). The H-bridge circuit can output a biphasic stimulation current pulse with

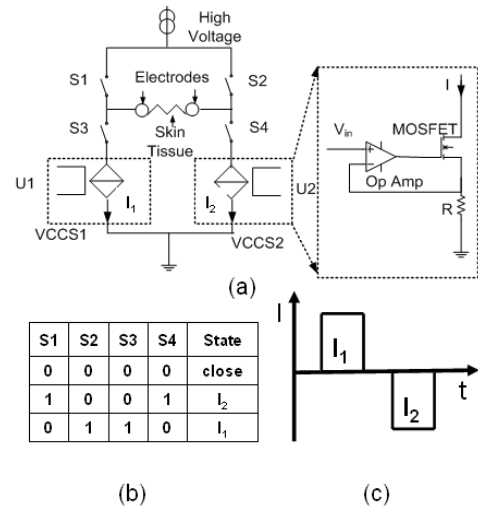


Fig. 4. The output stage circuit and its operation mode. (a) The schematic diagram of the H-bridge output. (b) The logic relation between S1-S4 and I_1 - I_2 . (c) The bipolar stimulation current

high precision of current amplitude. It can also deliver an arbitrary stimulation waveform, and keep the charge injection in two phases balanced (see Fig.4(a)).

The four switches (S1-S4) operate synergistically to realize biphasic stimulation. There are three states in the output operation (Fig. 4(b)). In the first state, all the switches are off to make sure that there is no current flow to the load, i.e. the patient skin tissue, and the output circuit isolates the patients from the high voltage of power supply. In the second state, the S1 and S4 are turned on, while the S2 and S3 are off. The stimulation current I_2 flows from S1 to S4, passing the electrodes and skin tissue, achieving one phase of stimulation. In the third state, the S2 and S3 are turned on, while the S1 and the S4 are off. The current I_1 flows from S2 to S4, passing the electrodes and skin tissue in reverse direction relative to the second state. Thus, a biphasic stimulation pulse can be realized during the second and third states (Fig.4(c)).

The VCCS is a necessary part of the H-bridge circuit for providing regulated output of stimulation current, even if the resistance of electrode-skin interface changes unpredictably. The VCCS circuit is capable of locking its output current at a constant level. It is a versatile and programmable current source composed of op amps and MOSFET transistor (see Fig. 4(a)). The V-I relation can be described by the formula as:

$$I = \frac{V_{in}}{R} \quad (3)$$

With $R=50\Omega$ and the range of V_{in} from 0V to 5V, the current amplitude can be programmed from 0mA to 100mA controlled by input voltage V_{in} . In our design, we use a DAC TLV5626 with 10-bit resolution as the programmable input voltage source for linear control of the constant current. The current resolution obtained is 0.097mA, resulting in a high precision VCCS.

The switches and VCCS could be programmed to produce stimulus waveforms that have a range of frequency, pulse width and amplitude. In addition, the charge-balance in the two phases can be achieved by setting the amplitude and timing of V_{in} to the two VCCSs, such that the multiplication of voltage and pulse width is the same during the second and the third states. This will make sure that the charge injected during the two phases (I_1 and I_2) are balanced.

3) *The design of the communication circuit:* The design of the communication circuit focuses on the reliability. TJA1050 is chosen as the chip of the CAN bus. The TJA1050 provides 1M/s data transfer rate at the max speed, and has high communication reliability with the low error rate. The CAN bus with the photoelectrical isolation, 6N137 guarantees the isolation between the DSSU and other circuits of the system, which can protect the patient from injury. This design satisfies the safety requirements of medical application.

D. ASIC Design of the DSSU

To further reduce the size of the DSSU, we are also designing an application of specific integrated circuits (ASIC) to replace part of the analog circuit in the output stage of the DSSU. The architecture of the ASIC is shown in Fig. 5. The ASIC is divided into two parts: a digital controller and a current driver. The digital controller is used to receive data from the outside components such as microcontroller (MCU), and decode the data to obtain stimulation pattern. The current driver works under high voltage and outputs stimulation

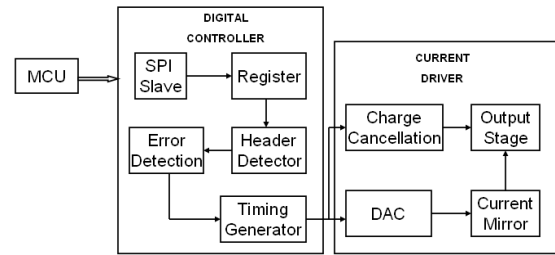


Fig. 5. Architecture of the ASIC

currents according to the received commands. The main challenge of ASIC design for surface stimulation is high output current under high voltage at the interface between the electrode and the skin. A plausible solution is to use multiple current sources, and combine the outputs of current sources to obtain a sum of current output.

III. TEST RESULT

In this development, close attention is paid to the trade-off between portability and high-performance, so that the FES system can be effectively deployed to home use. The boost DC-DC converter is used to lift the low DC voltage to a sufficiently high level for stimulation. In the test, it is found that two problems could impair the DC-DC converter. One is that the input current of the DC-DC converter became too large, when all the DSSUs on the bus are stimulating at the same time. This may increase the burden of power supply.

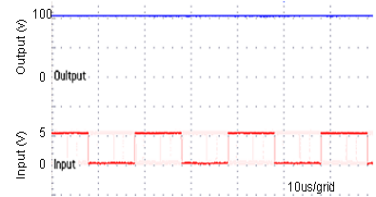


Fig. 6. The output voltage (upper) of the DC-DC converter without current load in the oscilloscope.

Soft-start method with an on-off frequency varying from low to high is also implemented to reduce the current intensity at the onset of system start. Another problem is the ripple of V_{out} of DC-DC convert may be large. The stimulation duration often is 1ms at the max, so the design criterion of V_{out} is that for a 100V output, the ripple should be within 5% of V_{out} . Fig.

6 shows that the DC-DC output is smooth without a load. With a load, we can choose appropriate external capacitor to meet the design requirement.

The performance of the H-bridge architecture at the output stage has also been tested. This architecture not only satisfies the need of a portable FES system, but also provides the high performance requirements. A series of tests have been performed to verify stimulation performance of the DSSU. We measure current intensity, stimulation pulse width and



Fig. 7: This picture shows the waveform of the H-bridge output voltage across the load resistor. In the picture, the stimulator generates a train of bipolar stimulation with the parameters as follow: the stimulation current is 50mA, the stimulation duration is 50 μ s, the stimulation frequency is 1kHz, and delay time is 100 μ s.

delay between the negative and positive pulses (Fig. 7) in the evaluation. First, we test the current intensity with other parameters kept constant and find that the range of current intensity is from 1mA to 58mA. Second, we continue to test the stimulation pulse with a square wave input from 5kHz to 50kHz to the S1 and S4, and a reversed square wave to S2 and

TABLE I
TEST FOR THE STIMULATION DURATION

INPUT PULSE WIDTH (μ S)	Output Pulse Width (μ S)	Standard Deviation (μ S)
10	10.462	0.033
20	19.496	0.043
30	30.012	0.027
40	40.340	0.232
50	49.700	0.671
100	100.800	0.187
200	200.400	0.499
400	399.390	0.393
500	500.860	0.643
1000	999.860	0.535

S3. We measure the stimulation current waveform between electrodes, i.e. voltage drop across the load. There is a discrepancy between the input pulse width and the measured pulse width. This difference remains fairly constant within the full range of pulse width, and is estimated at about 3.2 μ s on the average. We thus conclude that the difference between input and output pulse widths is due to the delay of component operation. This discrepancy in stimulation pulse width is then compensated by software correction. In order to testify the software compensation, we continue to test pulse width at 10 μ s, 20 μ s, 30 μ s, 40 μ s, 50 μ s, 100 μ s, 200 μ s, 500 μ s, 400 μ s, 1000 μ s. At each test value, we repeated 10 times to verify system output of pulse width. The test results are shown in Table I, where the output pulse width is varied from 1 μ s to 1000 μ s with an accuracy less than 1 μ s.

IV. CONCLUSION

In this paper, a network structure has been designed and tested for applications in stroke rehabilitation. A DSSU design in the network FES system is proposed and a prototype has been constructed and tested in laboratory. Future work is to complete integrated circuit implementation according to the prototype to further reduce stimulator size and to improve performance of the network FES system.

ACKNOWLEDGMENT

This work is supported by a key project (project 985 Phase II) from SJTU.

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