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Polymer Substrate Temperature Sensor Array for Brain Interfaces

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***Abstract*—We developed an implantable thin film transistor temperature sensor (TFT-TS) to measure temperature changes in the brain. These changes are assumed to be associated with cerebral metabolism and neuronal activity. Two prototype TFT-TSs were designed and tested *in-vitro*: one with 8 diode-connected single-ended sensors, and the other with 4 pairs of differential-ended sensors in an array configuration. The sensor elements are 25~100 μm in width and 5 μm in length. The TFT-TSs were fabricated based on high-speed ZnO TFT process technology on flexible polyimide substrates (50 μm thick, 500 μm width, 20 mm length). In order to interface external signal electronics, they were directly bonded to a prototype printed circuit board using anisotropic conductive films The prototypes were characterized between 23~38 °C using a commercial temperature sensor and custom-designed temperature controlled oven. The maximum sensitivity of 40 mV/°C was obtained from the TFT-TS.**

I. Introduction

LOCALalterations in cerebral metabolic rate of oxygen consumption, assumed to be correlated with variations in neuronal activity, and cerebral blood flow, can cause changes in local brain temperature. Measurements of temperature variations in a brain could reveal interesting underlying mechanics of several neurological disorders, and thus aid in the development of potential therapies. It has been reported that regional neural activation, for instance during a focal seizure, causes local temperature changes in the brain tissue [1, 2]. Also, imposed temperature variations are currently being investigated for seizure suppression and hypothermia treatment [1, 3]. In the healthy brain, cortical temperature variations on the order of 0.2 ºC have been observed in animal tests with visual and other forms of stimulation [4].

In order to measure local temperature variations in the brain, not only highly accurate micro-sized temperature sensors [5], but also implantable devices that can operate without damaging brain tissue are required. Several approaches have already been explored to measure brain temperature including magnetic resonance techniques (MRI), thermoelectric devices, infrared sensors, and SAW (Surface Acoustic Wave) devices [6], though with significant limitations. The temporal resolution of MRI is too low to detect real-time brain temperature changes. The spatial resolution of standard thermoelectric devices and SAW devices are too low to investigate local brain temperature changes caused by activities of a single or a few neurons since the device dimension (over 250 μm) is too large compared to the regions of activation. Furthermore, two critical drawbacks of these conventional devices are 1) the tissue damage upon insertion and, 2) the requirement of a metal base to be built. Metals intrinsically have a high rate of thermal diffusion, and metal-based temperature sensing devices tend to shunt heat over long distances and smooth the temperature field.

To overcome these challenges, we proposed a new implantable temperature sensor array based on zinc-oxide (ZnO) thin film transistors (TFT) fabricated on a flexible polyimide substrate. The sensor elements were characterized using a surface mounted thermocouple. Temperature characteristics of the prototype sensor array connected to external transduction electronics were investigated between 23~38 ºC using a custom designed temperature controlled oven.

II. Design of the TFT-TS

A. Single-ended TFT-TS

The prototype array with 8 single-ended sensor elements was formed with a distance of 300 μm between each element

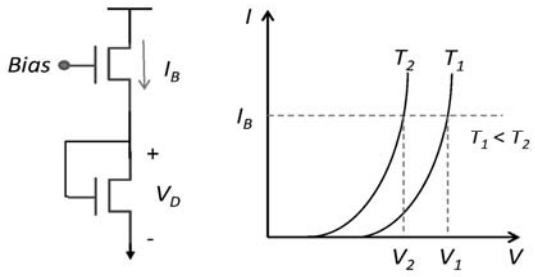

Fig. 1.The circuit schematic diagram of the single-ended TFT-TS and the operation principle of the sensor.

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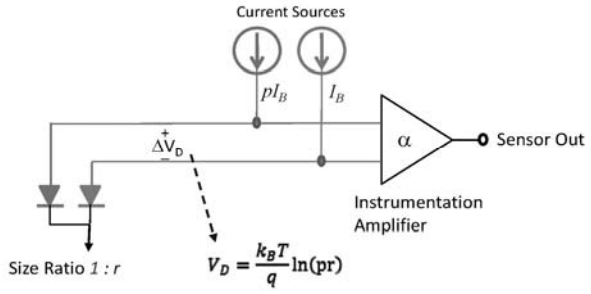


Fig. 2.Conceptual schematic diagram of the differential-ended TFT-TS.

on a 20 mm long, 500μm wide, and 50 μm thick polyimide substrate. As shown in Fig. 1, each sensor consists of two ZnO TFTs (one is for bias and the other is for the sensor) connected in series. The sensor TFT is 100 μm width and 5 μm length, and the bias current is generated using a large width TFT (Width/Length: 200/5 μm). Constant bias current I_B in the figure causes the voltage drop (V_D) that develops across the diode-connected ZnO TFT. If the bias current is properly chosen to prevent self-heating and assumed to be independent of temperature, then the dependence of V_D on temperature is determined by the threshold voltage and mobility in ZnO. It is well known that the voltage drop, as observed also in silicon devices, decreases proportionally to the inverse of the absolute temperature. In practice, the gate bias voltage for the bias TFT is selected slightly less than the threshold voltage level of the TFT, so that the TFT can supply constant current with a wide-range of source-drain voltages. Additionally, the bias TFT is located 15~20 mm from the sensor elements to ensure temperature insensitivity of the bias current

B. Differential-ended TFT-TS

The temperature sensor described above is simple and small in size, but most transistors do not have identical temperature characteristics due to fabrication process variations and power supply fluctuations. A way to circumvent this is to use differential signaling to cancel common-mode noise. As shown in (1), the voltage drop that develops across the diode with a given constant bias current I_B is proportional to the thermal voltage k_BT/q (where k_B is Boltzmann's constant, T is the absolute temperature, and q is the charge of an electron).

$$V_D = \frac{k_B T}{q} \ln\left(\frac{I_B}{I_S}\right), \qquad (1)$$

where I_S is the reverse bias saturation current of the diode. Transduction to temperature utilizes the voltage differences (ΔV_D) between a pair of diodes shown in Fig. 2. Additionally, to increase the temperature sensitivity, two of these diodes have a well-defined bias current ratio p:1 and geometric size ratio 1: r. Thus, ΔV_D can be derived from (1),

$$\Delta V_D = \frac{k_B T}{q} \ln\left(\frac{pI_B}{I_S}\right) - \frac{k_B T}{q} \ln\left(\frac{I_B}{rI_S}\right) = \frac{k_B T}{q} \ln(pr). \qquad (2)$$

This shows that ΔV_D, in principle, only depends on the ratios p and r and is independent of the absolute bias current and saturation current. The voltage difference between the pair is only dependent on the geometric ratio of the pairs and the thermal voltage (k_BT/q). Thus, the sensor outputs are proportional to absolute temperature.

Similar to the design of the single-ended TFT-TS, the constant bias currents are created using single TFTs with a current ratio of 4:1 (200 μm vs. 50 μm widths). The pair of sensors is designed with a geometric ratio of 1:4 and with a distance of 75 μm. The sensor array has four identical differential pairs of diodes. In each pair, one diode is 100 x 5 μm in dimension and the other is 25 x 10 μm.

III. Experiments

A. Array Fabrication

The first generation prototype TFT-TS was designed and fabricated using ZnO TFT fabrication technology on polymer substrates as shown in Fig. 3. The current prototype was designed to be 500 μm wide and 50 μm thick for *in-vitro* measurement and proof of concept. However this prototype can also be used for measuring *in-vivo* temperature changes in the cortex in brain. Furthermore, the design of the next generation TFT-TS includes further size reductions (less than 200 μm wide and 10 μm thick) will be made so that temperature variations can be measured deep in the brain without sacrificing the number of sensor elements in the

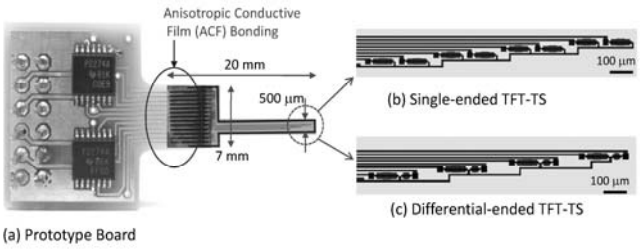


Fig. 3.Photographs of the TFT-TS prototypes.

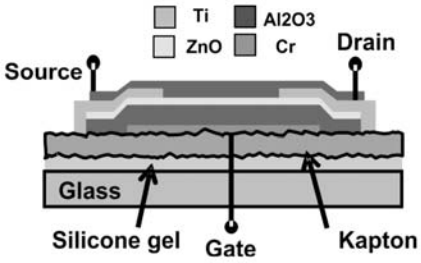


Fig. 4.The cross-sectional view of the ZnO TFT [8]. (Glass substrate is temporarily used for the entire fabrication process.)

arrays.

For the sensor elements (diodes and active loads), we used plasma enhanced atomic layer deposition (PEALD) ZnO thin film transistors (TFTs) because PEALD ZnO TFTs have a linearly decreasing threshold voltage with increasing temperature. We have previously demonstrated that PEALD ZnO TFTs on polyimide substrates worked with field-effect mobility of 20 $cm^2/V{\cdot}s$, excellent bias stress stability, and circuits with propagation delay < 20 ns/stage [7].

Fig. 4 is the cross-sectional view of the ZnO TFT formed on a polyimide substrate. The key process technology is the weak oxidant PEALD, in which an RF-induced plasma is used to enhance reactions that break the weak reactants on the metals and leaves a uniform and high purity oxidized layer on the surface. The plasma component makes PEALD a very flexible deposition technique and assists in depositing conformal high-quality films at low temperatures, which is faster and simpler than conventional atomic layer deposition (ALD) [8].

The full fabrication process for ZnO TFTs includes first distressing the polymer and adhering to a glass substrate with silicon gel. Then, a 100nmthick blanket chromium gate layer was deposited by ion-beam sputtering. The chromium layer was patterned by photolithography and wet etching for forming gate electrodes. A 32nm thick Al_2O_3 (from trimethylaluminum with CO_2 as the oxidant) and a 10nm thick ZnO) layers were then deposited in-situ at 200 °C by PEALD. The Al_2O_3 and ZnO layers were then patterned by photo- lithography and wet etching in H_3PO_4 (80 °C) and dilute HCl. Next, 150 nm thick titanium source and drain contacts were deposited by sputtering and patterned by photolithography and lift-off. Finally, a 30nm passivation layer of ALD Al_2O_3 was deposited from trimethylaluminum and H_2O at 200 °C. The ALD process was selected as a low-energy passivation process and resulted in improvement of stability with a small threshold voltage shift.

B. *In-vitro Test*

The TFT-TS prototypes were tested in a custom designed temperature controlled oven. The roof of the oven is made from an aluminum pad, on which a thermocouple heater/cooler is attached to control the oven's temperature. The oven temperature is measured by a commercial temperature sensor (TMP37, Texas Instruments, Inc.) located inside the oven. To maintain precise temperature control, a commercial PID (proportional–integral–derivative) temperature controller (CNi16D53, OMEGA Engineering, INC.)was used, which provides analog outputs for the thermocouple heater/cooler based on the temperature readout from TMP37. Single-ended TFT-TS's outputs are directly measured using an external data acquisition device (NI USB-6211, National Instruments, Inc.) and a LabVIEW (National Instruments, Inc.) program. The differential-ended TFT-TS's outputs are first amplified by a high-precision instrumentation amplifier (AD8224, Analog Devices, Inc.), and then digitized by NI USB-6211 and a LabVIEW program as well.

IV. Results and Discussion

A. *Characterization and Calibration of the ZnO TFT*

ZnO TFTs fabricated on polyimide substrates typically had field-effect mobility of 10~15 $cm^2/V{\cdot}s$. Temperature dependence of the drain currents in ZnO TFTs was measured from 20 to 70 °C and a reversible linear shift in threshold voltage was observed (Fig. 5), with associated pyroelectric charge coefficient of 1.5 nC/cm^2K and, approximately, 10 mV/°C sensitivity. When measured in the subthreshold regime at constant gate bias, a small change in threshold voltage results in a large change in conductance, and provides good temperature sensitivity. This result was also confirmed by measuring the temperature dependency of the drain voltages in subthreshold regime (the gate voltage = -3V). The drain voltage was measured between 20~35 °C using a surface mounted thermocouple. Sensitivity depends on the bias conditions and in the subthreshold a maximum of 350

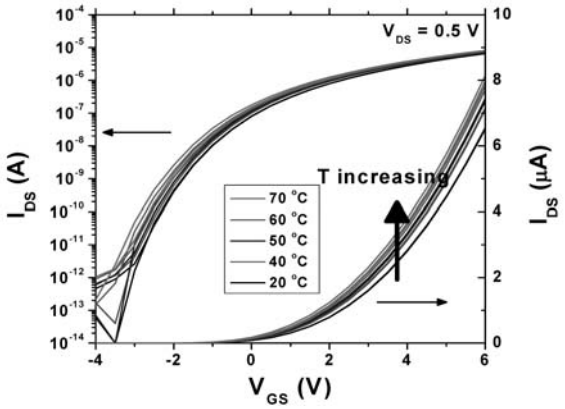


Fig. 5.The temperature dependency of the drain current (V_{DS} = 0.5 V, W/L = 200 μm/5 μm). Change in threshold voltage as a function of temperature for device showing pryoelectric charge coefficient of 1.5 nC/cm^2K

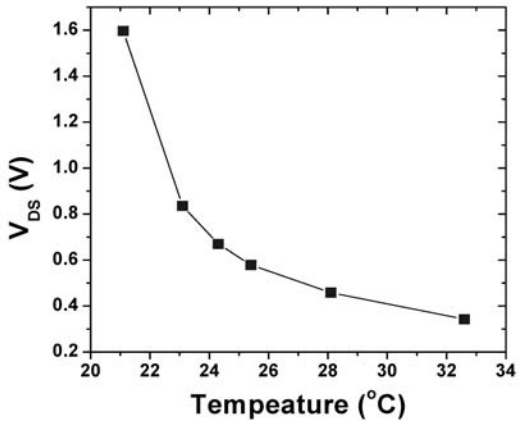
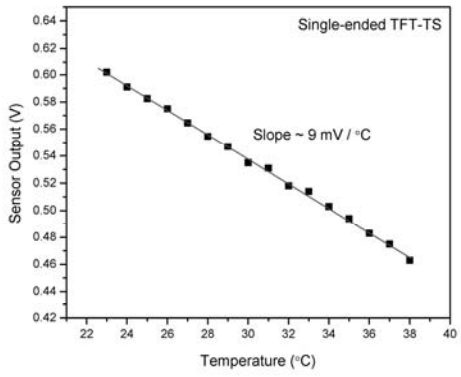
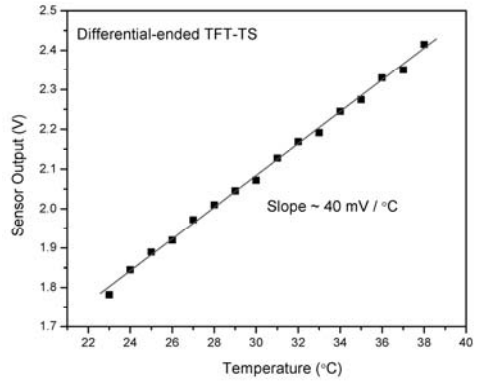


Fig. 6.The temperature dependency of the drain voltage (I_{DS} = 4nA, V_{GS} = -3V). The sensitivity decreases as the shift in threshold voltage moves



(a)



(b)

Fig. 7.(a) Temperature Characteristic of the single-ended TFT-TS. (b) Temperature Characteristic of the differential-ended TFT-TS.

mV/°C is observed (Fig. 6). However, notably, the TFT-TSsoperate in saturation region rather than subthreshold region since the sensor TFT is diode-connected. Therefore, the actual temperature sensitivity of the TFT-TS ismuch less than 350 mV/°C and is dependent on the temperature dependency of threshold voltage in saturation region, the maximum of approximately 10 mV/°C.

B. In-Vitro Measurements of the TFT-TS

The oven temperature is swept from 23~38°C with a ramp-up speed of 1°C/min. The single-ended TFT-TS output decreased as temperature was raised with a slope of 9 mV/°C, as shown in Fig. 7(a), which value is close to the maximum temperature sensitivity of the threshold voltage. Compared to common silicon devices, the temperature sensitivity of TFT-TS is 4.5 times better than that of silicon devices, which is around 2 mV/ºC [9]. Furthermore, the differential-ended TFT-TS outputs show 40 mV/ºC of temperature sensitivity, as shown in Fig. 7(b). This temperature sensitivity is also higher than that of commercial IC temperature sensors (for example, the sensitivity of TMP37 is 20 mV/ºC).

V. CONCLUSION

We have described the design and development of The TFT-TSs, sensor array for measuring brain temperature changes with high spatial and temporal resolution. The two prototypes were fabricated based on low-temperature ZnO TFT process technology on 50 μm thick, 500 μm wide, 20 mm-long polymer substrates. The maximum temperature sensitivities obtained were 9 mV/ºC and 40 mV/ºC for single-ended and differential-ended TFT-TSs, respectively. The sensitivity of these prototypes is at least 4.5 times higher than the sensitivity of conventional silicon based temperature sensors.

So far, we have used commercially available thick polyimide (50 μm) substrates for these devices. But this is far thicker and stiffer than the dimensions desired for neural implants, which could be as thin as 10 μm. As a result, all aspects of handling of these devices have been far easier than it would be with thinner substrates, an advantage in the initial development phase of this project. It is likely that an additional layer of an even softer polymer will improve our ability to handle these devices without incurring damage, and that such layers will further ease the mechanical mismatch between the devices and neural tissue. We therefore will investigate the addition of layers of parylene to the devices for further encapsulation.

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