33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

A Fully Integrated Continuous-Time 50-Hz Notch Filter with Center Frequency Tunability

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***Abstract*—A novel continuous-time notch filter based on current steering technique was described in this paper. The second-order notch filter consisted of two integrators, one unity-gain inverter and two alpha blocks that were fully integrated onto a silicon chip. The circuit was implemented in SMIC mixed-signal 0.18μm 1P6M process with the die area of 0.06 mm^2. Post-annotated simulation indicated the continuous-time notch filter was capable of providing 55.4dB attenuation for the 50 Hz power line interference and its center frequency was tunable against process variations.**

I. Introduction

With the introduction of prevention-oriented healthcare technologies, there is an increasing demand for portable and wearable devices to continuously monitor body physiological signals [1, 2]. Since most of these physiological signals are very weak in amplitude and relatively low Signal-to-Noise ratios (see TABLE I [3, 4]), the filter design is critical for analogue front-end circuits.

It is envisaged that the power line interference (either 50 Hz or 60 Hz) is a significant noise source during physiological signal recording and is ubiquitous in most clinical situations [5]. Power line noise could be easily picked up through electrode cables, electrical devices and the patient being monitored.

Although Twin-T configuration is one of the conventional approaches, it cannot be easily integrated into silicon due to the large resistor or capacitor values prohibitively needed. Typical integrated resistors and capacitors range from 1 ohm to 40 kilo ohms and from 0.5 to 50 pF [6]. For larger components the nonlinearity and parasitic may seriously affect the proper function and the die area of the chip may become impractically large. For example a Twin-T filter with a 50 Hz notch frequency could need 100 kilo ohms resistance and 31.83 nF capacitance, only this 31.83 nF capacitor will cost at least 31.83 mm^2 if fabricated using SMIC 0.18-μm CMOS technology.

Switched-capacitor integrators were extensively employed for low-frequency notch filters [7-10]. However, the MOS transistor switch would introduce error through channel charge injection and clock feed-through mechanisms. Transconductance amplifiers and capacitors (OTA-C) provide another implementation for fully integrated continuous-time filters. Reference [11] described a CMOS OTA-C 5^{th}-order single-ended low-pass 50 Hz notch filter; however, because all the OTAs are operating in weak-inversion region, it is more vulnerable to noise interference and OTA nonlinearity. Bryan [1] brought a new method based on time constant multiplier (TCM) circuit; although this configuration can increase the time constant by one thousand times, it needs ten operational amplifiers that inevitably increase the chip area and power consumptions.

In this paper, a novel configuration, which needs only three ordinary operational amplifiers, was presented. This new notch filter was based on current steering technique, which could be easily fabricated in silicon; besides, all the operational amplifiers were working in conventional saturation region, which lead to reduced design difficulties.

TABLE I
PROPERTIES OF PHYSIOLOGICAL SIGNALS

Physiological Signal	Measurement Range
Electroencephalography (EEG)	25-300 μV
Electroretinogram (ERG)	5-900 μV
Electrogastrogram (EGG)	10-1000 μV
Electrocardiography (ECG)	0.5-4 mV
Electromyography (EMG)	0.1-1.5 mV
Photoplethysmograph (PPG)	5-100 nA

II. Notch Filter Overview

Generally speaking, a notch filter is a special case of a band-stop filter and passes all frequencies except for a narrow range [12]. There are some terms to characterize the performance of notch filter: center rejection frequency (ω_0), quality factor (Q), stop bandwidth (BW). A high Q corresponds to a narrow stop bandwidth while low Q relatively a wide stop bandwidth. The transfer function of a notch filter is generally expressed as

$$H(s) = \frac{s^2+\omega_0^2}{s^2+\frac{\omega_0}{Q}+\omega_0^2}. \quad (1)$$

Fig.1 shows a regular bi-quad notch filter. If we assume $R_0 = R_1 = R_2 = R$, $C_0 = C_2 = C_3 = C$, then the transfer function of this circuit can be written as

$$\frac{V_o(s)}{V_i(s)} = -\frac{1+R^2C^2s^2}{1+RC_1s+R^2C^2s^2} \ . \quad (2)$$

This work was sponsored by Chinese Academy of Science "the 100 Talent People" Program.

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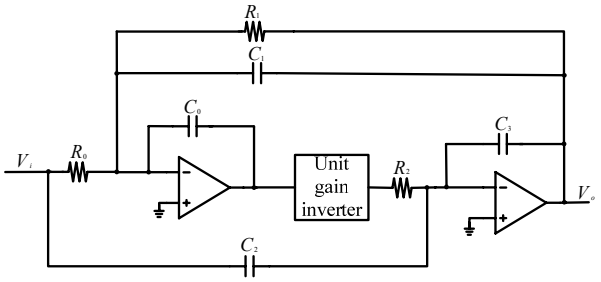

Fig.1. A regular bi-quad notch filter

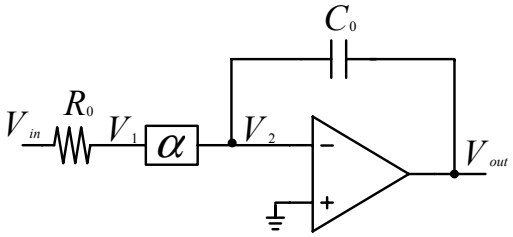

Fig.2. Current steering integrator

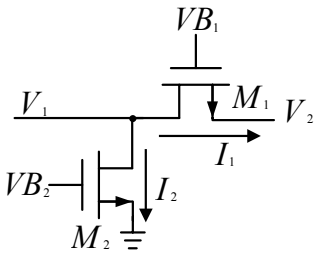

Fig.3. α block

Comparing (2) with (1), we can get

$$\omega_0 = \frac{1}{RC} \qquad Q=\frac{C}{C_1}.$$

As the R and C values cannot be very large, the value of ω_0 is at least 10^5 rad/s, which is far more than the 100π that the 50 Hz notch filters need.

III. Current Steering Integrators

The most straightforward solution of decreasing the value of ω_0 or increasing the integrator's time constants RC is to reduce the capacitor's charging and discharging time while the values of R and C are kept small enough in order to be integrated into silicon. Fig. 2 is the current steering integrator circuit and fig. 3 is the detailed circuits of α block. This architecture is similar to the low-pass filter presented in [13] but the feedback resistor removed. Because α is much less than 1, the voltage of V_1 is almost zero. Thus, the transfer function of this integrator is

$$\frac{V_2}{V_1} = -\frac{1}{\frac{RCs}{\alpha}}.$$

Where

$$\alpha = \frac{I_1}{I_2} \ll 1.$$

Therefore the time constants of this new integrator can increase 1/α times; in other words, the -3-dB frequency can correspondingly decrease α times.

The α block consists of two MMOS transistors operating at the deep triode region. Thus, these two transistors can act as resistors whose values are controlled by the overdrive voltage. Because the source of M1 is connected to the virtual ground, the overdrive voltages of M1 and M2 are VB_1 and VB_2 respectively. So α can be written as

$$\alpha = \frac{I_1}{I_2} = \frac{\left(\frac{W}{L}\right)_1 (VB_1 - V_{th})}{\left(\frac{W}{L}\right)_2 (VB_2 - V_{th})}. \tag{3}$$

By adjusting the value of $(\frac{W}{L})_1$, $(\frac{W}{L})_2$, VB_1 or VB_2,We can change the value of α and consequently change the -3-dB frequency. In this paper, VB_2 is set to be the source voltage V_{dd}, and in order to maximally reduce the channel-length modulation effect, the value of $(\frac{W}{L})_1$ and $(\frac{W}{L})_2$ are set to 1μm/8μm and 17.3μm/8μm respectively. VB_1 is used to adjust the -3-dB frequency.

IV. The Improved Notch Filter

A. The overall circuits

The integrators in Fig. 1 are the basic units of the regular bi-quad notch filters whose center rejection frequency equals to the -3 dB frequency of their integrators. Consequently, if the integrators of regular bi-quad notch filter are substituted by current steering integrators, a novel circuit, which can carry the center rejection frequency from tens of thousands hertz to only a few dozen hertz, will be born.

Fig. 4 shows the architecture of this novel notch filter. The detailed circuits of operational amplifiers and unity-gain inverter are presented in Fig.5 and Fig.6 (d). According to Kirchholff's law, we have

$$\left(\frac{V_i}{R_0} + \frac{V_o}{R_2} + V_o C_2 s\right)\alpha = (0 - V_1)C_0 s, \tag{4}$$

$$\frac{-V_1}{R_1}\alpha + V_i C_3 s = (0 - V_o)C_1 s. \tag{5}$$

Thus

$$\frac{V_o}{V_i} = -\frac{1+\frac{R_0 R_1 C_0 C_3 s^2}{\alpha^2}}{\frac{R_0}{R_2}+R_0 C_2 s+\frac{R_0 R_1 C_0 C_1 s^2}{\alpha^2}}. \tag{6}$$

If $R_2 = R_1 = R_0$, $C_1 = C_2 = C_0$, the transfer function will become

$$\frac{V_{out}}{V_{in}} = -\frac{1+\frac{R_0^2 C_0^2 s^2}{\alpha^2}}{1+R_0 C_1 s+\frac{R_0^2 C_0^2 s^2}{\alpha^2}} \tag{7}$$

Then the center rejection frequency and quality factor correspondingly equal to

$$\omega_0 = \frac{\alpha}{R_0 C_0} \ll \frac{1}{R_0 C_0}.$$

This way, the new notch filter's center rejection frequency can reduce α times than the regular bi-quad notch filter. Here, R_0=297.015kΩ, $C_1 = C_0$=1.42pF. Actually, the value of C_3 should be a little larger than the theoretical value C_0 so that the pass-band gain was able to be closer to 0dB. The SPICE simulation result showed that the pass-band gain can reach -6.52mdB at 1 Hz when C_3 is set to 1.45pF.

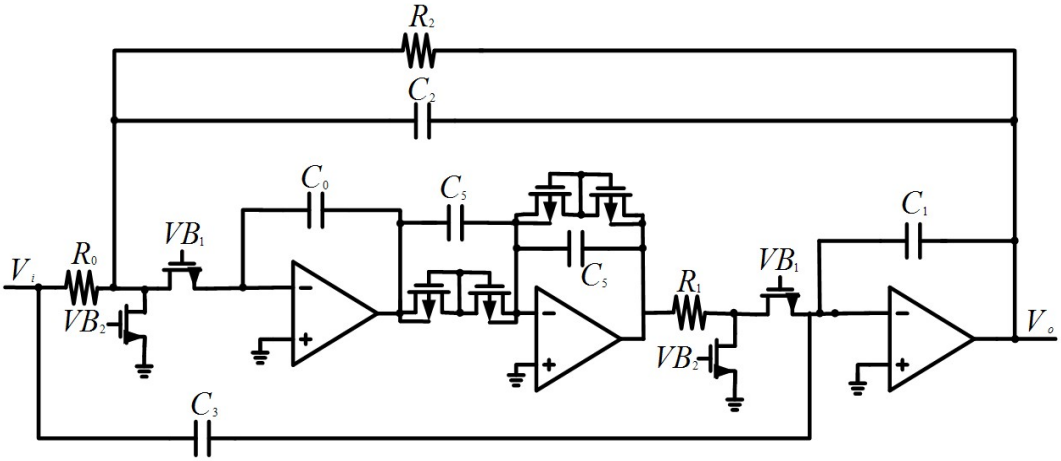

Fig.4. A novel 50Hz notch filter with center rejection tenability.

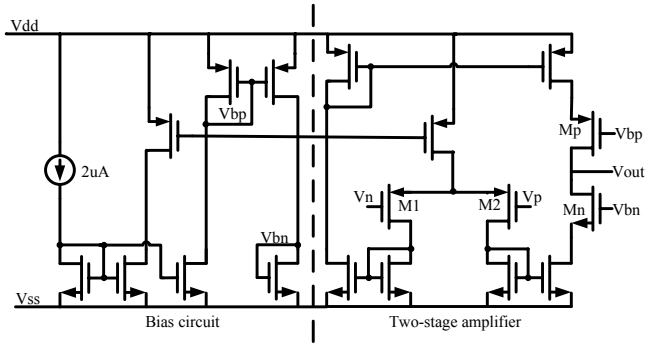

Fig.5. A two-stage Operational amplifier

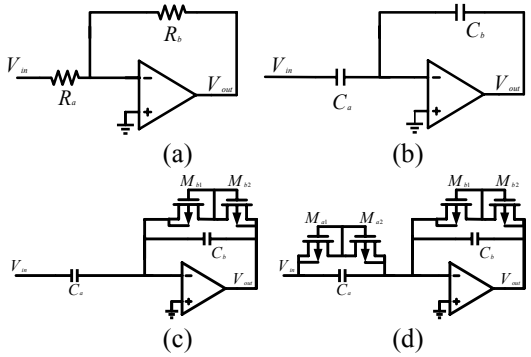

Fig.6. Four type inverters

B. The Operational amplifier design

Fig.5 shows the schematic of the operational amplifier used in the notch filter; the left part is bias circuit and the right part two-stage amplifier. As the flicker noise is inversely proportional to the frequency, we should especially concern it when designing low-frequency filters. What's more, PMOS device exhibits less flicker noise than NMOS transistors because the former carry the holes in a "buried channel"[14], consequently the PMOS transistors is used as input devices (M1 and M2). The transistor Mn and Mp are cascaded to the output stage in order to boost the gain.

C. Unity-gain inverter

The performance of unity-gain inverter will strongly influence the notch attenuation of this notch filters. In order to understand this, let us simply assume the input and output meet the following linear conditions

$$V_{1o} = -kV_{1i} + \Delta V_1,$$

where V_{1i} and V_{1o} represent the input and output voltage of the unity-gain inverter, and ΔV_1 is the offset voltage. Now we can get the new transfer function

$$\frac{V_o}{V_i} = -\frac{1+\frac{R_0^2 C_0^2 s^2}{k\alpha^2}}{1+R_0C_0s+\frac{R_0^2C_0^2s^2}{k\alpha^2}} - \frac{R_0C_0s}{(1+R_0C_0s+\frac{R_0^2C_0^2s^2}{k\alpha^2})}\frac{\Delta V_1}{V_{in}}. \quad (8)$$

Formula (8) indicates that the performance of unity-gain inverter not only effect the notch frequency, but also decreases the notch attenuation.

Fig. 6(a) is a classic inverter amplifier. If $R_a = R_b$, this amplifier will become one unity-gain inverter, however , this cannot be easily implemented in integrated circuits because the integrated small resistors need strong drive capability which will inevitably increase the power consumption. Fig. 6(b) is an inverting charge amplifier often used in switched capacitor circuits. Though this architecture can be integrated into silicon, it cannot invert the input signal whose DC voltage is not equal to the reference voltage and saturated the output voltage. Fig. 6(c) parallels one pseudo-resistor with C_b.The value of this pseudo-resistor can reach as large as several gige ohms so that it will draw little currents from the operational amplifier. Although this circuits improves the shortcomings of Fig. 6(b), unfortunately it introduces nonlinear problems especially when the input is larger than the twice of PMOS's threshold voltage. The inverter in Fig. 6(d) overcomes all the drawbacks of previous circuits. When the value of one pseudo-resistor nonlinearly changes with the input voltage, the other one will change at the same time, hence the magnification can be kept -1 without considering the input voltage. It works as Fig.6 (a) but can be fabricated into silicon without costing much chip area. In this paper, $C_a = C_b = 485.5$ fF, and the width and length of all PMOS transistors used in pseudo-resistors are 0.3 μm and 8 μm respectively.

V. POST-ANNOTATED SIMULATION RESULTS

• This current-steering notch filter was designed using SMIC mixed-signal 0.18μm 1P6M process with metal-insulated-metal (MIM) capacitors. Fig. 7 shows the complete layout which occupies an area of $0.0588\,mm^2$ (0.42mm×0.14mm). Since the MIM capacitor is fabricated between the fifth metal and the sixth metal which have longer distance from the bulk than that of doubly poly process [15], the parasitic capacitor can be greatly reduced. In order to decrease the mismatch of critical devices (such as C_a and C_b in Fig.6(d)), the matched capacitors and resistors are placed as close as possible, just as cap array and resistor array showed in this figure.

We simulated this notch filter using the netlist extracted from the layout. The filter's frequency response is showed in Fig. 8, where VB_1 is set to 1.35V. The upper curve corresponds to the phase response while the lower magnitude response. The notch frequency locates at 50Hz and has an attenuation of 55.4dB.What's more, the upper -3-dB and lower -3-dB frequency are 71.6 Hz and 29Hz respectively.

Varying the controlling voltage VB_1, the frequency response will correspondingly change just as Fig. 9. The center of the five curves is got when VB_1=1.35V. From this figure we can find that the higher VB_1 is, the larger the notch frequency is. To understand why, we can substituting α in (7) with (3) and have

$$\omega_0 = \frac{\left(\frac{W}{L}\right)_1 (VB_1 - V_{th})}{\left(\frac{W}{L}\right)_2 (VB_2 - V_{th})} \frac{1}{R_0 C_0}. \qquad (9)$$

Thus ω_0 will be proportional to VB_1 if the other variables are kept constants, however, the relationship between ω_0 and VB_1 is actually not linear, but more like a parabola. The post-layout simulation results of ω_0 versus VB_1 is presented in Fig. 10. Here, the slope of this curve will become more precipitous as the VB_1 increases.

The input-inferred noise is only $4.12\mu V/\sqrt{Hz}$ at the pass-band frequency 1 kHz. Also the simulation shows that its input amplitude range can vary from 0.8 V to as weak as 10μV, which indicates that the dynamic range is 78dB. The power supply rejection ratio (PSRR) is simulated to be 65dB.

Fig.11 depicts the simulated time-domain response of the proposed notch filter with a 15pF load. The input signal was a $100mV_{pp}$ 1-Hz sine wave mixed with a $50mV_{pp}$ 50-Hz sine wave, and VB_1 was set to 1.35V. The output was about 180 degree delayed due to the inverted signal path from C_3 to C_1 which was clearly presented in Fig. 4. Fig.11 demonstrates that the notch filter can effectively reject the power line noise.

The detailed post-simulation results are summarized in Table II.

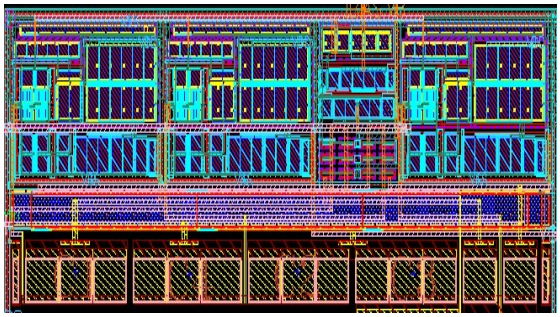

Fig.7. Microphotograph of this novel notch filter

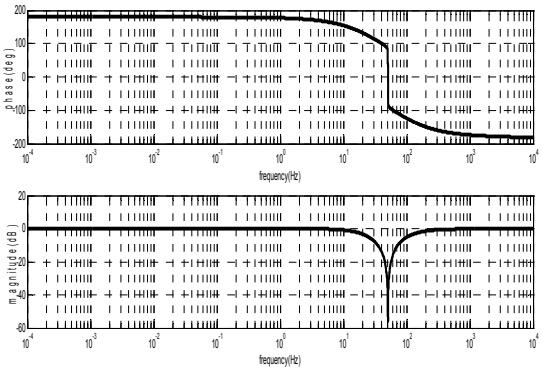

Fig.8. The phase and magnitude's frequency

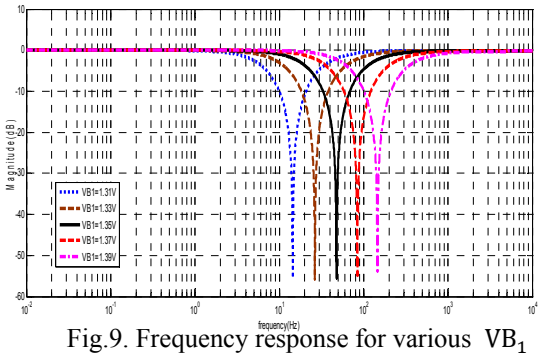

Fig.9. Frequency response for various VB_1

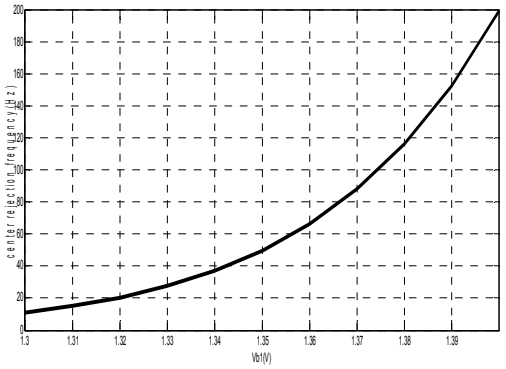

Fig.10. Center rejection frequency versus VB_1

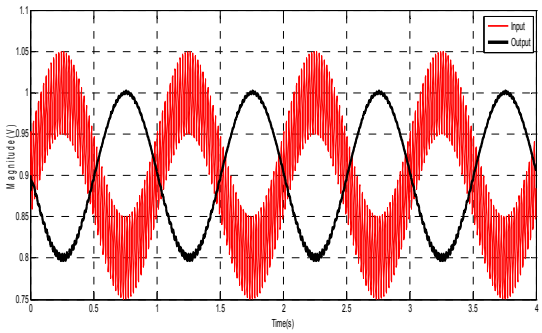

Fig.11.Time-domain response of the proposed notch filter

TABLE II
SIMULATED SPECIFICATIONS OF THE NOTCH FILTER

Power supply voltage	1.8V
Center rejection frequency	50Hz
Center attenuation	55.4dB
Input-referred noise @1kHz	$4.12\mu V/\sqrt{Hz}$
PSRR	65dB
Dynamic range	78dB
Upper -3-dB frequency	71.6Hz
Lower -3-dB frequency	29Hz
Power consumption	25.2μW
Die area	0.42mm×0.14mm

VI. CONCLUSIONS

The notch filter designed by us was fully fabricated into silicon. The key technique in order to decrease the center rejection frequency is by the deployment of the current steering integrators. By using two current-steering NMOS transistors, a continuous-time integrator with ultra large time constant was obtained, with which a low-frequency bi-quad notch filter was designated. Different unity-gain inverters were compared in order to optimize the integration. The post-annotated simulations showed that the integrated circuits occupied approximate 0.06mm^2 die area, which could achieve the notch attenuation of 55.4 dB at 50 Hz.

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