

The Design of CMOS General-Purpose Analog Front-End Circuit with Tunable Gain and Bandwidth for Biopotential Signal Recording Systems

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Abstract— In this paper an 8-channel CMOS general-purpose analog front-end (AFE) circuit with tunable gain and bandwidth for biopotential signal recording systems is presented. The proposed AFE consists of eight chopper stabilized pre-amplifiers, an 8-to-1 analog multiplexer, and a programmable gain amplifier. It can be used to sense and amplify different kinds of biopotential signals, such as electrocorticogram (ECoG), electrocardiogram (ECG) and electromyogram (EMG). The AFE chip is designed and fabricated in 0.18- μm CMOS technology. The measured maximum gain of AFE is 60.8 dB. The low cutoff frequency can achieve as low as 0.8 Hz and high cutoff frequency can be adjusted from 200 Hz to 10 kHz to suit for different kinds of biopotential signals. The measured input-referred noise is 0.9 μV_{rms} , with the power consumption of 18 μW per channel at 1.8-V power supply. And the noise efficiency factor (NEF) is only 1.3 for pre-amplifier.

I. INTRODUCTION

Biopotential signals are electrical potentials that accompany with all biochemical processes and measured between points in living cells, tissues, and organisms. Many organs in human body, such as heart, brain, and muscles, modulate their functions through electric activities [1]. Heart activities produce electrocardiogram (ECG) signals. Brain activity produces electroencephalogram (EEG) or electrocorticogram (ECoG) signals. Muscles' activities, such as contraction and relaxation, produce electromyogram (EMG) signal. Table I shows the frequency and amplitude characteristics of these biopotential signals. They have characteristics of small amplitude, low frequency and variability.

With rapid development in technologies of medical devices recently, biopotential recording system is widely used in health monitoring, brain-machine interface, neural prosthesis, etc. Therefore, plenty of work has been devoted to improving the recording system. An analog front-end, including amplifiers and filters, is the key component of a biopotential signal recording system.

TABLE I. THE ELECTRICAL CHARACTERISTICS OF COMMON BIOPOTENTIAL SIGNALS

Biopotential Signal	Amplitude (mV)	Bandwidth (Hz)
EEG	0.005-0.3	0.5-150
ECoG	0.01-3	0.5-500
ECG	0.5-4	0.01-250
EMG	0.1-5	dc-2K

A biopotential amplifier must meet the low noise requirement since the small amplitudes of the targeting signals. The input impedance should be high so that the signal loss in electrode interface is minimized. Considering the applications of portable and implantable devices or instrumentation, power dissipation must be minimized for long-term recording. Moreover, high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) design are required to reduce the 50/60 Hz interference from power lines and other disturbance source. Another important design issue is the rejection of differential DC offset, which is generated by tissue-electrode interface and may result in saturation of the amplifier. Because the bandwidths of these biopotential signals are from the millihertz range to few kilohertz range, a band-pass filter with extreme low cutoff frequency is required. It is quite a challenge to realize a fully integrated filter with millihertz cutoff frequency in deep submicron technologies.

A MOS-bipolar pseudo-resistor is proposed in [2] to realize a tens millihertz low cutoff frequency. The resistance of the pseudo-resistor is more than 10^{12} ohm when the voltage across this device is between ± 0.2 V. The work achieves the NEF of only 4 by properly designing the operational amplifier to minimized thermal and flicker noise. However, it is realized in 1.5 μm technology, which is not suitable for monolithically integrating with other functional blocks such as digital signal processing or high frequency circuitries.

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The target of this work is to build a multi-channel analog front-end IC for neural recording with a deep submicron technology that can be integrated with other blocks, such as RF and DSP, to a single chip for building an implantable long-term monitoring device. An 8-channel AFE circuit for neural recording is realized with TSMC 0.18- μm CMOS technology. The key components of the front-end circuit are a pre-amplifier, aimed at high CMRR, low noise, DC blocking, and around 40dB mid-band gain with low power consumption, an 8-to-1 analog multiplexer designed to multiplex 8-channel signals, and a programmable gain amplifier that provides various gains for selection. The implementation results show an input-referred noise of 0.9 μV_{rms} , bandwidth up to 10 kHz while only consumes 18 μW at 1.8-V power supply, and the NEF is only 1.3 for the pre-amplifier.

The rest of this paper is organized as following: In Section II the system/circuit design consideration is described. In Section III, the implementation and measurement results are presented. Finally, a concluding remark is made in Session IV.

II. DESIGN CONSIDERATION

A. System operation

Main blocks of the proposed AFE are shown in Fig. 1. The Neural signals that caused by the electrical-chemical reaction in living tissue is sensed at input node of the pre-amplifier which is the first stage of AFE. Because neural signals are small in amplitude, the pre-amplifier must have low noise characteristics, high CMRR, high PSRR. And extreme low cutoff frequency must be designed to eliminate the DC offset voltage between each channel that caused by the electrode-tissue interface. In this paper, high cutoff frequency is designed to be tunable for detecting different neural signals.

In order to reduce area and power of the chip, an 8-to-1 channel analog multiplexer (MUX) is connected after pre-amplifier to multiplex the channels. Once one certain channel is selected, the signal from that pre-amplifier will be further amplified by the following shared programmable gain amplifier (PGA). The PGA not only provides gain but also converts the differential signal to single-ended. It also traces and holds the signal for further analog to digital conversion.

B. Pre-amplifier

Pre-amplifier consists of a negative feedback loop chopper stabilized amplifier (CA) with MOS-bipolar pseudo-resistor and a passive low-pass filter as shown in Fig. 2(a). The chopper stabilized technique reduces the flicker noise. The operation principle of CA is described in the following. The input signal is modulated to the chopping frequency, amplified and demodulated to the baseband. The offset voltage of OTA and low-frequency noises are modulated only once, and their frequencies are shifted to the chopping frequency (f_{chop}). These modulated offsets and noises can easily be filtered by a low-pass filter and only leaves the amplified in-band signal to the next stage [3]. The corner of the flicker noise is around 60 kHz, thus the f_{chop} is set at 125 kHz to eliminate the low-frequency device noise. The negative feedback resistor R_{H} is

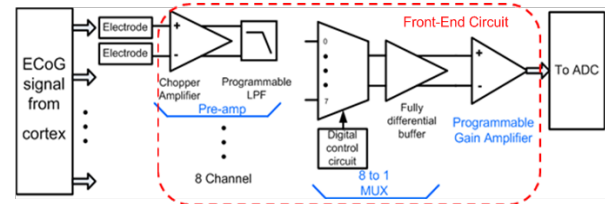


Fig. 1. The structure of the analog front-end circuit

implemented with MOS-bipolar pseudo-resistor to realize high impedance, and low cutoff frequency to block DC offset voltage [4]. R_{H} is implemented using PMOS with source-body connected as shown in Fig. 2(a). The structure of the OTA is a telescopic op-amp with embedded chopper-modulators as illustrated in Fig. 2(b) [5]. The chopper switches are placed at low impedance nodes to avoid affecting the bandwidth of the amplifier. The telescopic amplifier structure is selected as the OTA due to its characteristics of low power consumption and low noise. The transfer function of pre-amplifier is approximately given by

$$H(s) \approx \frac{-s \frac{C_1 A_0}{C_2 A_0 + C_1 + C_2}}{s + \frac{G_{\text{H}}(A_0 + 1)}{C_2 A_0 + C_1 + C_2}} \quad (1)$$

Where A_0 is the DC gain of OTA, and G_{H} is the transconductance of R_{H} . Low cutoff frequency is determined by G_{H} , C_1 , C_2 , and A_0 . It can be tuned by an external voltage V_{B} . Mid-band gain is $C_1 A_0 / (C_2 A_0 + C_1 + C_2)$ which is C_1 / C_2 approximately. This stage is designed to provide a gain of 40dB, with C_1 equaling to 10pF and C_2 equal to 100fF.

A second order MOST-C filter is used to implement the low-pass filter. Compare to other filter architectures, MOST-C filter is chosen according to its low offset voltage and low power consumption.

By adjusting the gate voltage of the pseudo-resistor in the pre-amplifier stage and the control voltage of the MOST-C filter, the low and high cutoff frequency of the AFE can be adjusted respectively to suit for different types of neural signals appropriately without increasing the area of the loading capacitor.

C. Analog Multiplexer

The analog multiplexer includes a single stage CMOS switch array, switch control circuit, and a fully differential buffer with switching rate of 500k channel/sec is shown in Fig. 2(c). The fully differential buffer is composed of a differential difference amplifier (DDA) [6] as shown in Fig. 2(d). The output of DDA is expressed as

$$V_{\text{out}}^+ - V_{\text{out}}^- = A_0 \cdot [(V_{\text{pp}} - V_{\text{pn}}) - (V_{\text{np}} - V_{\text{nn}})]. \quad (2)$$

A_0 is the gain of DDA.

Because the following PGA stage provides additional gain up to 51 V/V of with only 1-V output swing, careful layout is made to ensure the output offset voltage of this stage is limited to prevent signal distortion in the PGA stage.

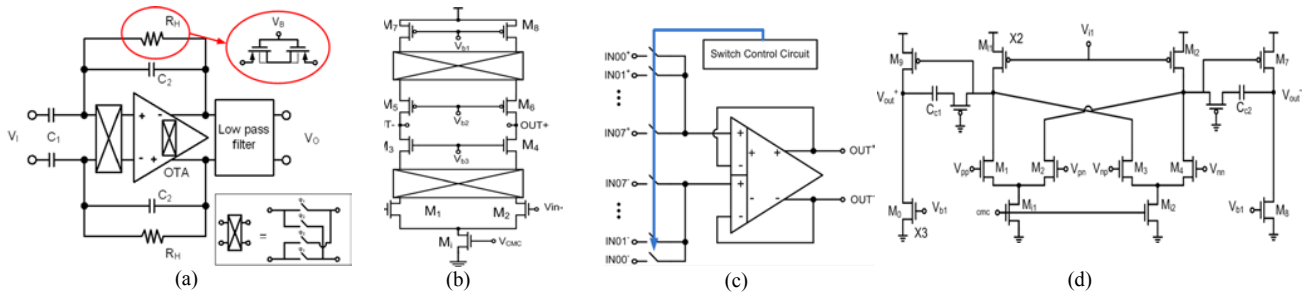


Fig. 2. (a) Architecture of the pre-amplifier. (b) Schematic of OTA used in the pre-amplifier. (c) Structure of analog multiplexer. (d) Schematic of differential difference amplifier.

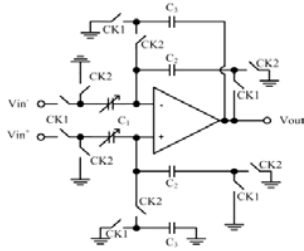


Fig3. Schematic of the PGA stage.



Fig.4. Die photograph of the proposed AFE.

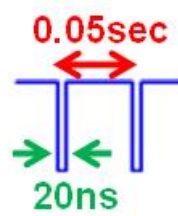


Fig.5. The fast-settle signal.

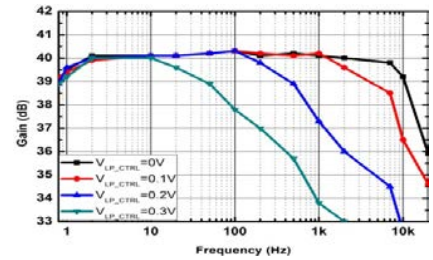


Fig.6. Measurement result of midband gain (PGA gain=1), and tunable bandwidth.

D. Program gain amplifier (PGA)

The final stage of AFE is the PGA. It provides amplification and differential-to-single output conversion. The PGA is realized by a single-ended capacitive-reset gain topology as shown in Fig. 3. It is based on the correlated double sampling (CDS) technique to eliminate the drifting of output common mode voltage that arises from the offset voltage and minimize the $1/f$ noise.

The gain of this stage is the ratio of C_1 to C_2 . The size of C_2 can be adjusted to obtain different gain as shown in Fig. 3. The sampling rate of PGA is chosen at 500k channel/sec to match with the analog multiplexer.

III. MEASUREMENT RESULTS

A. Circuit Performances

The proposed circuit for biopotential signal recording systems is designed and fabricated in TSMC 0.18- μm CMOS 1p6m process. The chip area is $1.5 \times 1.8 \text{ mm}^2$ as shown in Fig. 4, and consumes $18 \mu\text{W}$ for one-channel pre-amplifier. The long time-constant associated with the pre-amplifier leads slow recovery from external large disturbance. Thus, a “fast settle” signal as shown in Fig. 5 is applied to the pseudo-resistors to reset the input common mode voltage of the CA stage occasionally. The frequency of repeat “fast settle” signal limits the low cutoff frequency of AFE. In this case, it is limited to 0.8 Hz. Hence, the frequency response of the AFE is shown in Fig. 6, the mid-band gain is about 40.3 dB (the gain of PGA is set to 1), and the tunable high cutoff frequency can vary from 200 Hz to 10 kHz while the low cutoff frequency can reach below 0.8 Hz. The PGA stage provides further tunable gain of 1, 3, and 11 V/V as shown in Fig.7. Because the limitation of the equipment, the maximum gain of the PGA is obtain from the post-layout simulation and it achieves

51 V/V. Fig. 8 shows the measured input-referred noise spectrum density of the designed AEF. The measured input referred noise level is $0.9 \mu\text{V}_{\text{rms}}$ for one channel pre-amplifier and $5.1 \mu\text{V}_{\text{rms}}$ for whole AFE up to 10 kHz bandwidth. All performances are summarized in Table II. The NEF of the pre-amplifier is only 1.3. The formula of NEF is shown as below:

$$\text{NEF} = V_{\text{ni,rms}} \cdot \sqrt{\frac{2I_{\text{tot}}}{\pi U_T \cdot 4kT \cdot \text{BW}}} \quad (3)$$

B. ECG Measurement

The designed AFE is used to record the ECG signal. By connecting the differential input nodes of two one-channel AFEs to the right and left shoulders as the differential inputs using two electrodes, and connecting the right ankle to the ground, the ECG signal is obtained. The P, Q, R, S, and T waves can be recognized from the measured ECG signal as shown in Fig. 9.

IV. CONCLUSION

This paper presents an 8-channel AFE for biopotential signal recording systems including eight chopper stabilized pre-amplifiers, an 8-to-1 analog multiplexer, and a programmable gain amplifier, which was designed and verified using TSMC 0.18- μm CMOS process. The measurement results show the signal band of the proposed circuitry is from 0.8 Hz to 200 Hz that can also be extend to 10 kHz to suit for different biopotential signals. Due to the signal amplitude limitation of instrumentation, the gain of the AFE is measured from 40.3 dB to 60.8 dB (74.1 dB from post-layout simulation with smaller input signal). The power consumption of one-channel pre-amplifier is only $18 \mu\text{W}$ at 1.8-V power supply. And the NEF of the proposed pre-amplifier is 1.3 which outperforms the comparison circuitries.

TABLE II. THE COMPARISON OF THIS WORK WITH OTHER NEURAL AMPLIFIERS.

Specification	This Work	[7]	[8]	[9]	[2]
Technology	0.18 μ m CMOS	0.5 μ m CMOS	0.8 μ m CMOS	AMI 1.5 μ m	1.5 μ m CMOS
channel	8	1	1	1	1
Chip Area	2.7 mm ²	4.81 mm ²	0.7 mm ² *	0.17 mm ² *	4.84 mm ² **
Supply voltage	1.8V	1.5V	1.8V/3.3V	3V	2.5V
Power consumption	18 μ W (one channel pre-amp) 446 μ W(8-channel AFE)	1.335 mW	1.8 μ W/3.3 μ W	114.8 μ W	80 μ W
DC gain	40.3/49.5/60.8dB 74.1 dB (post layout simulation)	80dB	41/50.5dB	39.3dB	39.5dB
Bandwidth	<0.8 Hz ~200Hz-10 kHz(tunable)	0.3Hz-150 Hz	0.05/0.5/2.5 Hz-180Hz	9.1kHz	0.025-7.2kHz
CMRR	105B	117dB	80dB	-	>83 dB
PSRR	91dB	52dB	-	-	>85 dB
Input-referred noise	0.9 μ V _{rms} (one channel pre-amplifier) 5.1 μ V _{rms} (AFE) (0.5-10 kHz)	0.86 μ V _{rms} (0.3-150Hz)	0.95 μ V _{rms} (0.05-100Hz)	7.8 μ V _{rms} (0.1Hz-10kHz)	2.2 μ V _{rms} (0.5Hz-50kHz)
NEF	1.3/21.8(one channel pre-amplifier/AFE)	56.9	5.4	19.4	4

*w/o PAD, **6 amplifiers .

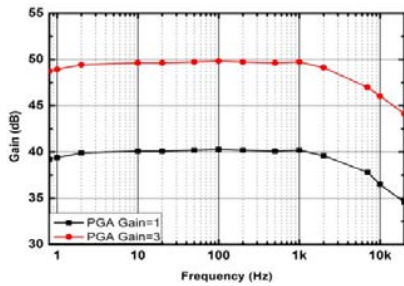


Fig. 7. Frequency response of AFE with tunable gain.

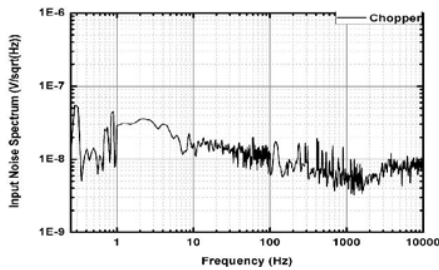


Fig. 8. Measured input-referred noise of the pre-amplifier.

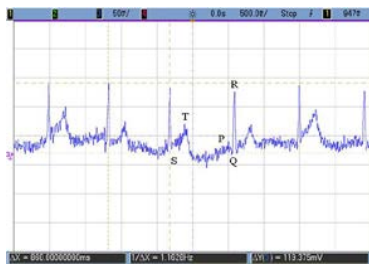


Fig. 9. Measured ECG signal.

REFERENCES

- [1] N. V. Thakor, *Biopotentials and Electrophysiology Measurement*, Baltimore, MD: Johns Hopkins School of Medicine, 1999.
- [2] R. R. Harrison, C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958- 965, 2003.
- [3] C. C. Enz, G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol.84, no.11, pp.1584-1614, Nov. 1996.
- [4] S. Farshchi, A. Pesterev, E. Guenterberg, I. Mody, J.W. Judy; "An Embedded System Architecture for Wireless Neural Recording," *3rd International IEEE/EMBS Conf. on Neural Engineering*, pp. 327-332, May 2007.
- [5] M. Sanduleanu et al., "A low noise, low residual offset, chopped amplifier for mixed level applications," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, vol. 2, pp. 333-336,1998.
- [6] H. Alzahr and M. Ismail, "A CMOS fully balanced differential difference amplifier and its applications," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 48, no. 6, pp. 614-620, Jun. 2001.
- [7] K. A. Ng and P. K. Chan, "A CMOS Analog Front-End IC for Portable EEG/ECG Monitoring Applications," *IEEE Transactions On Circuits And Systems—i: Regular Papers*, Vol. 52, No. 11, November 2005.
- [8] T. Denison, K. Consoer, W. Santa, A. T. Avestruz, J. Cooley, and A.Kelly, "A 2 μ W 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J.Solid-State Circuits*, vol. 42, no. 12, pp. 2934-2945, Dec. 2007.
- [9] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with DC input stabilization," *IEEE Trans. Biomed. En.*, vol. 51, no. 5, pp. 832-837, May 2004.