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Design of a Novel Digital Phantom for EIT System Calibration

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Abstract—**This paper presented the design method of a novel digital phantom for electrical impedance tomography system calibration. By current sensing, voltage generating circuitry and digital processing algorithms implemented in FPGA, the digital phantom can simulate different impedances of tissues. The hardware of the digital phantom mainly consists of current sensing section, voltage generating section, electrodes switching section and a FPGA. Concerning software, the CORDIC algorithm is implemented in the FPGA to realize direct digital synthesis (DDS) technique and related algorithms. Simulation results show that the suggested system exhibits sufficient accuracy in the frequency range 10 Hz to 2 MHz. With the advantages offered by digital techniques, our approach has the potential of speed, accuracy and flexibility of the EIT system calibration process.**

I. Introduction

ELECTRICAL impedance tomography (EIT) is a medical imaging technique which displays the spatial distribution of the complex conductivity inside a body[1]. In a common EIT system, an excitation is applied to electrodes on the body surface, causing an electromagnetic field appearing within the volume. The resulting electrical potentials are measured. Image reconstruction involves the calculation of the conductivity distribution from these potential measurements, and the resulting images can be used for medical diagnosis or treatment.

The problem of image reconstruction from initial measured signals is essentially inverse and ill posed. In essence, even small changes of the measured signals will result in large changes on the reconstructed image[2]. To avoid the images to be influenced by systematic measurement errors, calibration of the hardware is an indispensable process[3].

Standard value calibration (also known as reference value calibration) is a basic method, which is commonly used in measurement system calibration[4]. In EIT applications, saline solution or phantoms (made of biological tissue mimicking material or resistor/capacitor networks) are used for calibration[5]. However, the impedance of these phantoms cannot be changed dynamically to match the requirements of a number of applications. Designers have to construct a number of different phantoms to evaluate system performance under different conditions. To simplify this calibration process, we have designed a digital phantom, which can simulate different impedances of test objects under different frequency conditions.

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II. Principle of Digital Phantom

Our approach is device independent. A simplified circuit model of a typical EIT current injection and voltage measuring system is shown in Fig.1. The current source generates a constant current (I1) injected into the tissue under test. By measuring the voltage (V1) on the electrodes, the impedance of tissue (Z1) can be calculated by Ohm's law.

In order to simulate the impedance Z1, we need to provide an equivalent voltage to the measuring electrodes of the EIT system. The digital phantom can be considered as a Current-Control Voltage Source (CCVS). The output voltage (V2) is controlled by the current (I_2) which is equal to the output of current source (I_1). If V_2 is always equal to V_1, the measured impedance (Z_2) will be the same to that of the actual tissue (Z_1) as in Eq.1:

$$Z_2 = \frac{V_2}{I_2} = \frac{V_1}{I_1} = Z_1 \tag{1}$$

This simulated impedance Z_2 could be considered as a "virtual impedance unit" which has same response with actual tissues under excitation. Therefore, by this CCVS circuit, we could simulate the impedance of human tissues without actual biological sample present.

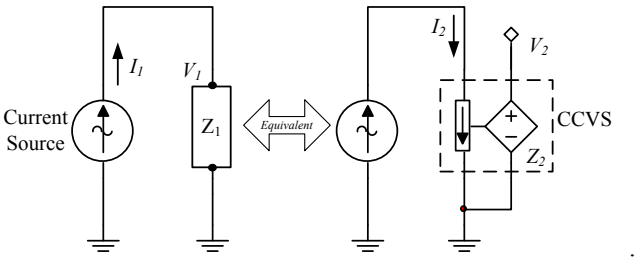

Fig. 1. Principle of Digital Phantom

III. Hardware Design

The digital phantom mainly consists of four parts: current sensing section, voltage generating section, electrodes switching section and field programmable gate array (FPGA). The current sensing section is used for measuring the value of injected current. The voltage generating section generates a voltage equivalent to the resulting voltage across the actual object. The electrode switching section takes charge of

connecting the "virtual impedance unit" to the relevant electrodes, depending on the application, which are under calibration. FPGA is used for signal processing, communication and control. The brief function diagram of the digital phantom is shown in Fig.2.

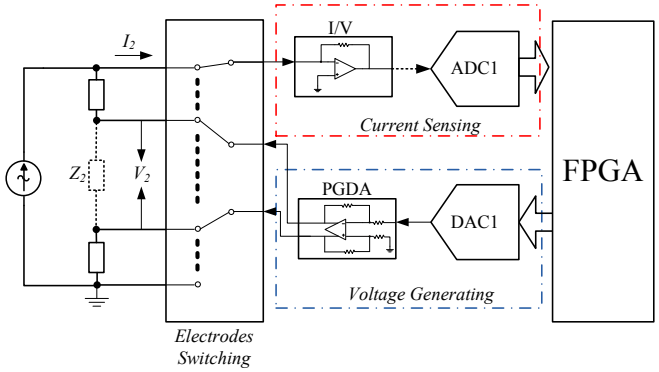

Fig. 2. Hardware Architecture of Digital Phantom

A. *Current Sensing Section*

The function of the current sensing section is measuring the injected current. A convenient way to convert injected current into a measurable voltage is to use a low bias current op amp, configured as a current-to-voltage converter as shown in Fig.3 below. The bias of the current source is maintained at zero by the virtual ground of the op amp, and the short circuit current is converted into voltage. For increasing the sensitivity and dynamic range, the feedback resistor could be selected by switching in different values (e.g. 1k Ohm, 10 k Ohm, 100 k Ohm). The voltage is acquired by a high-speed ADC (14 bit, 100 Msps) for further processing.

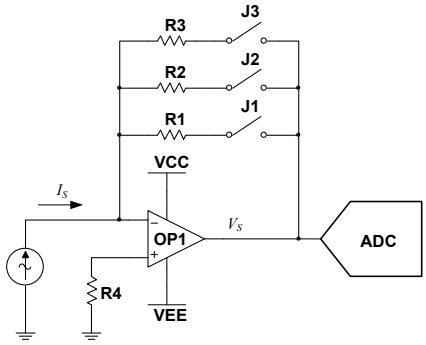

Fig. 3. Diagram of Current-to-Voltage Circuit

B. *Voltage Generating Section*

The voltage generating section includes a digital-to-analog converter and signal conditioning circuits. We used a 14 bit, 500Mhz DAC generate voltage by DDS technique. There are three parts in the signal conditioning circuits: filter section, gain section and buffer section. The filter section is an anti-aliasing filter for our DDS application. It is used for removing the higher harmonics of the DDS output signal. The gain section is realized by a programmable gain amplifier, which is controlled by the FPGA, can significantly extend the dynamic range of system. The last stage is buffer section. By using a high-speed, low noise fully differential amplifier, it sends the differential voltage to the selected electrode pair. The brief diagram of the signal conditioning circuits is shown in Fig.4 below.

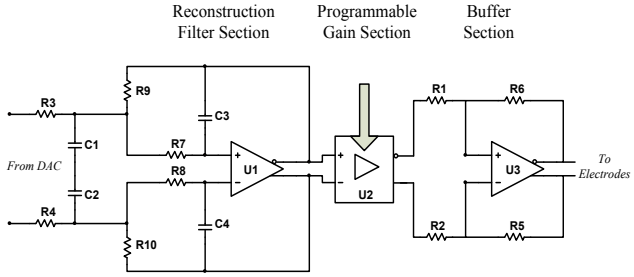

Fig. 4. Diagram of Signal Conditioning Circuits

IV. SOFTWARE DESIGN

The software implemented in the FPGA performs the detection of the injected current from the EIT system and generates a virtual resulting voltage back to the measurement electrodes, making the measurement result equal to an actual impedance object. The functional diagram of the FPGA program is shown in Fig.5.

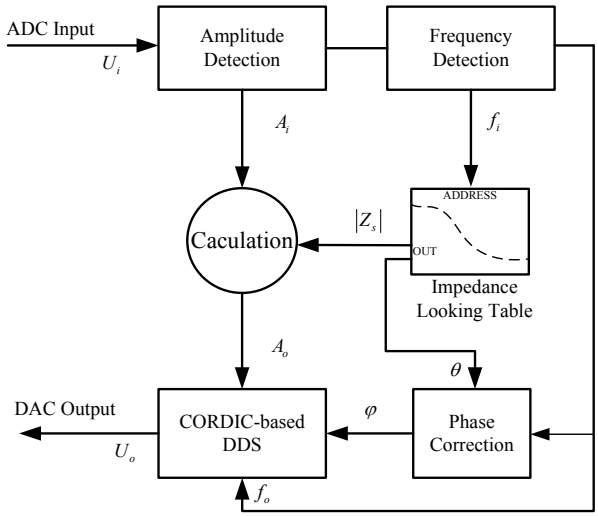

Fig. 5. Software Architecture of Digital Phantom

An amplitude detection module is used to detect the amplitude of the voltage signal (U_i) which is converted directly from the injected current. With the known values of the feedback resistor (R_f) in the I-V circuit discussed above, the amplitude of the injecting current (A_i) can be calculated by Eq.2:

$$A_i = \frac{U_i}{R_f} \tag{2}$$

With the impedance's magnitude equal to that of the simulated object ($|Z_s|$), the amplitude of the output voltage (A_o) can be calculated by Eq.3:

$$A_o = A_i \cdot |Z_s| \tag{3}$$

Because Z_s is a complex impedance value varying with frequency, an accurate value of Z_s is determined by the current excitation frequency (f_i). A frequency detection module is used to measure the frequency of the excitation source. The

detected frequency will be used as an address to read data from a Look-Up-Table structure which contains the complex impedance information of the object being simulated in the frequency domain. The outputs of this table include magnitude and phase angle information of the impedance. The magnitude information is used to calculate the amplitude, and the phase angle (θ) information is sent to the phase correction module to calculate the correct phase of output.

Due to the latency in analog circuits and FPGA, the output voltage could be considered as a delayed response to the input current, which makes the simulated impedance inaccurate. To overcome this drawback, phase correction is a necessary step. Assuming the processing latency time is Δt , the corrected phase angle of output signal could be calculated by Eq.4:

$$\angle U_o = \varphi = \theta + 2\pi f_i \Delta t \quad (4)$$

With the results of amplitude (A_o), phase angle (φ) and frequency (f_o=f_i), the output voltage can be calculated by Eq.5:

$$U_O(t) = A_o \sin(2\pi f_o(t + \Delta t) + \theta) \quad (5)$$

To generate this voltage signal, the amplitude, frequency and phase information is sent to a waveform generating module, which generates signal by using DDS technique. DDS is a method for using digital data processing blocks as a means to generate a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source[6]. Due to the digital nature of the DDS functionality, it offers fast switching between output sine wave frequencies, fine frequency resolution, and operations over a broad frequency range.

In our application, we realized the DDS technique by Coordinate Rotation Digital Computer (CORDIC) algorithm. CORDIC is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. The CORDIC algorithm is based on the concept of complex phasor rotation by multiplication of the phase angle by successively smaller constants[7]. The algorithm can be implemented efficiently by a series of simple binary shifts and additions/subtractions.

In DDS application, the CORDIC algorithm computes the sine and cosine of an input phase value by iteratively shifting the phase angle to approximate the Cartesian coordinate values for the input angle. At the end of the CORDIC iteration, the x and y coordinates for a given angle represent the cosine and sine of that angle, respectively. Since the CORDIC architecture eliminates the sine/cosine looking up table by real-time waveform computation, it can provide higher phase resolution, thus reducing spurious signals caused by phase quantization. Fig.6 shows the CORDIC-based DDS architecture.

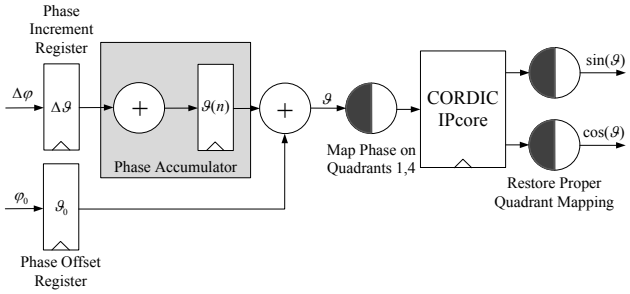

Fig. 6. Architecture of CORDIC-based DDS

The CORDIC algorithm in our system is implemented by Xilinx's LogiCORE IP CORDIC, which supports a fully parallel configuration with single-cycle data throughput at the expense of silicon area. By advanced XtremeDSP DSP48A slices and parallel architecture, the speed of the CORDIC-based DDS can be up to 200 MHz.

V. Performance Evaluation

With the assistance of advanced simulation software in computer, we could evaluate the system performance before implementation. Considering the system's analog-digital mixed architecture, the simulation process is divided into two steps. We firstly simulated the digital processing algorithm in FPGA to evaluate the latency and resource-consuming, and then built a circuit model to interact with PSPICE-based simulation models of other analog devices.

A. Current Sensing Section

The simulation results are shown in Fig.7. The curves show the different frequency response of different feedback resistor of current-to-voltage circuit. From the graph, we can find that the bandwidth of the current sensing circuit will decrease when the value of the feedback resistor increase, meaning there is a trade-off between the magnitude of the simulated impedance and the system bandwidth.

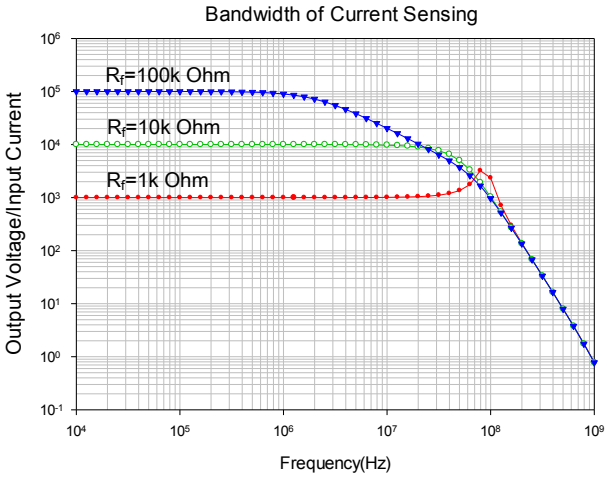

Fig. 7. Bandwidth Evaluation of Current Sensing Section

B. Voltage Generating Section

The simulation results are shown in Fig.8. The curves show the different frequency responses under different gain settings

of voltage output circuit. It can be seen that even in maximum gain, the bandwidth of voltage output circuit is larger than 10 MHz, which can fully satisfy the requirements of most EIT applications.

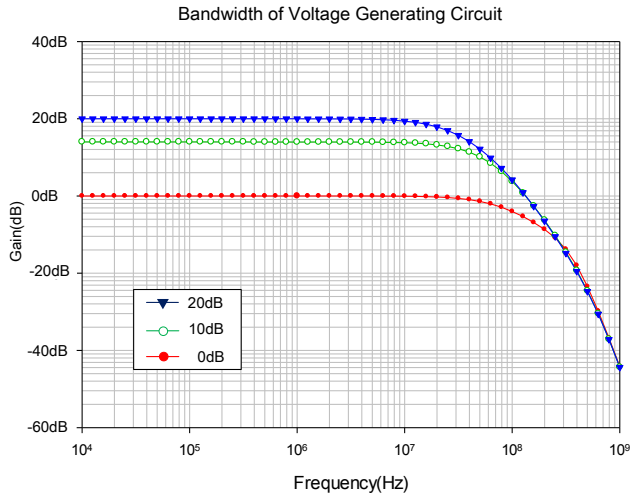

Fig. 8. Bandwidth Evaluation of Voltage Generating Section

C. *Overall Response Speed*

The overall response speed depends on many factors: frequency of excitation signal, delay in analog circuit, algorithm time consuming and so on. We considered these factors and constructed an equivalent simulation circuit to evaluate overall performance of our system.

The result is shown in Fig.9. The red line is the ideal resultant voltage on simulated impedance caused by the excitation current. The green line is the generated voltage. The total latency (t_L) is approximately 170 ns at 10 MHz excitation. Then the phase of the output voltage is corrected and the simulated impedance is available for use in calibration.

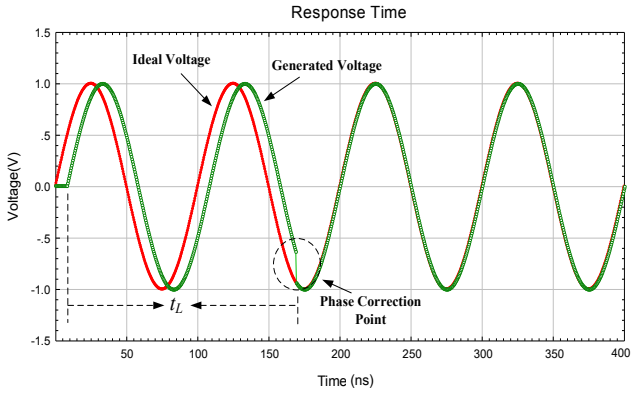

Fig. 9. Evaluation of Response Time

We use a three-component equivalent model to evaluate performance of system accuracy. The simulation results are shown in Fig.10. The red curve is theoretical impedance of the model. The blue curve is our simulated impedance by digital phantom and the green curve is the measuring results by our EIT system. Graphs show that the digital phantom could simulate impedance accurately in frequency range 10 Hz to 2 MHz. At higher frequency, due to the detection errors and the algorithm speed limit, the accuracy of the digital phantom will degrade.

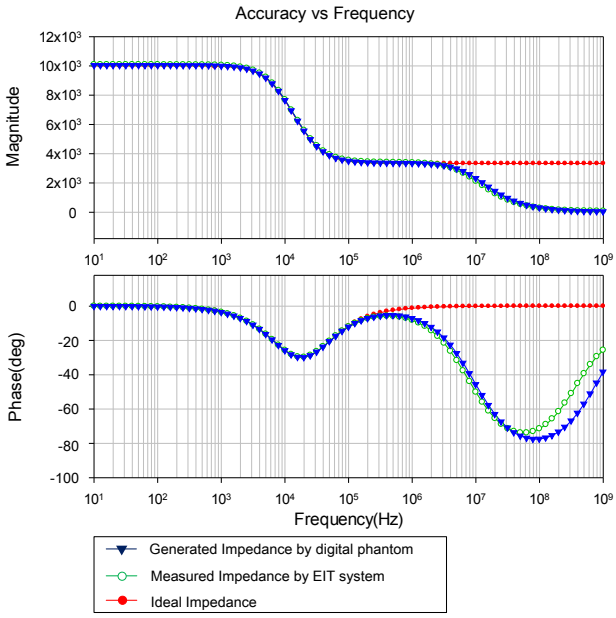

Fig. 10. System Accuracy Evaluation

VI. Conclusion

For improving the speed and flexibility of EIT system calibration, a novel digital phantom has been designed. By using high-speed digital devices and digital algorithms, this phantom can simulate different impedance of tissues with high accuracy. The simulation results reveal that the digital phantom has sufficient accuracy in frequency range 10 Hz to 2 MHz. Our digital phantom is currently under optimization for improved accuracy and frequency response. Additional validation work has been proposed for when this method is used in practice.

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