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A Generic Miniature Multi-feature Programmable Wireless Powering Headstage ASIC for Implantable Biomedical Systems

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***Abstract*—Wireless powering holds immense promise to enable a variety of implantable biomedical measurement systems with different power supply and current budget requirements. Effective power management demands more functionality in the headstage design like power level detection for range estimation and power save modes for sleep-wake operation. This paper proposes a single chip ASIC solution that addresses these problems by incorporating digitally programmable features and thus has the potential to enable wireless powering for many implantable systems. The ASIC includes an RF rectifier which has a peak efficiency of 17.9% at 900MHz and 11.0% at 2.4GHz, a robust 1V bandgap reference and LDO voltage regulator whose output can be programmed in the range of 1V–1.5V, and can drive upto 4mA of load current. The input RF power level detector has a threshold of 1.6V and the power management block can be programmed to give a 6%, 12.5% or 25% duty cycle power line to the transmitter resulting in upto 60% reduction in average power. The ASIC was fabricated using the TSMC 65nm process, occupies 1mm^2 die area and the headstage consumes ~300µA at 1.2V regulated supply.**

***Keywords* – wireless RF powering headstage, implantable biomedical system, programmable ASIC, power gating.**

I. Introduction

RECENT advancements in the semiconductor industry have resulted in an increased thrust towards the design, development, and deployment of implantable biomedical devices for various healthcare applications. Reliable and efficient power supply and management are primary concerns for the successful operation of implantable electronics. Conventional battery powering has several disadvantages. External battery powering, using wires, leads to infections, and mechanical instability. This can be avoided in applications involving superficial implants, e.g., EEG recording, by integrating the battery with the implant system. But, deep implant applications, e.g., internal blood pressure monitoring, have additional issues with battery replacement. Hence, wireless powering proves to be a promising alternative for these applications [1]-[2]. Different near-field and far-field powering methods have been considered to provide wireless power supply for portable systems [1]. Inductive coupling is the most commonly used near-field powering technique, which provides good link efficiency but is bulky, sensitive to orientation and has limited range. These disadvantages make inductive powering unsuitable for long range remote powering.

The Federal Communications Commission (FCC) has allocated ISM (Industrial, Scientific and Medical) band frequencies (900MHz, 2.4GHz) for medical applications [3]. Far-field powering at these frequencies reduces antenna size and increases range of powering. Apart from requiring a reliable regulated supply to ensure desired functionality and acceptable performance, implantable systems demand more flexible features like different operating voltages, power saving options, input power level sensing etc. Furthermore, silicon area is severely limited to allow compact packaging. For the same reason, external passive components and crystal oscillators should be minimal.

In this paper, a generic, miniature, stand-alone, robust wireless powering ASIC module with digitally programmable features that can be used for a variety of applications is presented. The unique set of features offered by this ASIC have been chosen diligently after careful consideration of the requirements for a typical implantable system. This module also has a low-jitter on-chip clock reference which can be used for sampling in low throughput applications like ECG recording. This paper is organized as follows. Section II briefly describes the design considerations for the ASIC component blocks. Section III presents the overall architecture of the headstage, explains the implementation details of each component block and elaborates the silicon measurement results. Section IV considers a case study to demonstrate different systems powered using this headstage. Section V concludes the paper and briefly discusses future scope for improvement.

II. Headstage Design Considerations

Wireless powering headstages have been traditionally used for RFID tags [1]. Typical headstage architecture primarily consists of RF rectifier, which converts the received AC signal to DC voltage, voltage regulator, and voltage limiter –stack of zener diodes, to protect from surges at the rectifier output [4].

In a typical setup, an external powering source radiates high frequency RF power that is received by an antenna and

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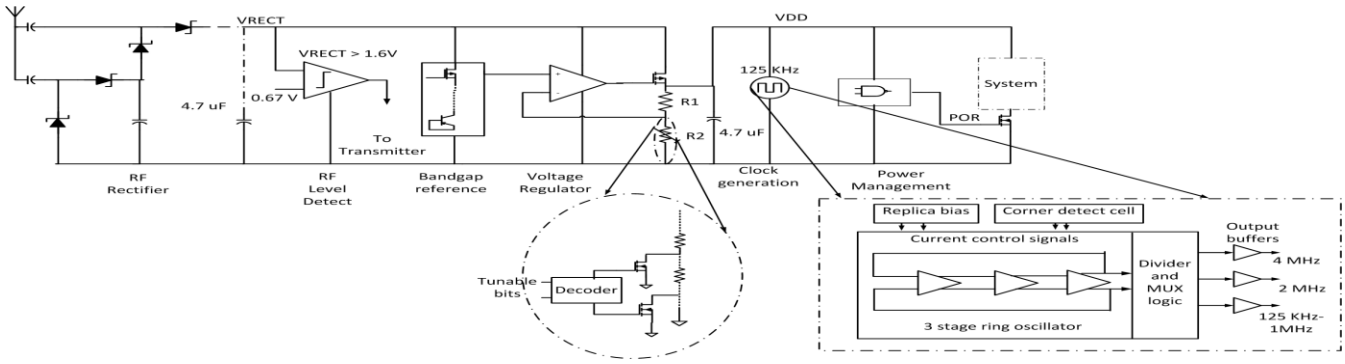

Fig. 1. Wireless powering Headstage Architecture

delivered to the headstage. The overall efficiency of wireless powering depends on the rectification efficiency for a given frequency of powering, input power delivered, resonance and impedance mismatch losses, antenna geometry, and tissue losses. The effective power available at the rectifier input depends on multi path losses (~1-10dB for a range of 1-100cm, assuming a two-ray ground reflection model), skin attenuation based on implant depth (~5dB for 1-3mm below the skin, ~30dB for a depth of 3-5cms), antenna efficiency and matching losses (~5-10dB depending on frequency, antenna size and topology) [5]-[6].

Due to the high losses, implantable applications demand better rectification efficiency which degrades at lower input powers, higher frequencies, and higher load currents, due to substrate coupling and diode losses. Hence, a multistage rectifier has to be carefully designed to maximize efficiency within the given process technology and area limitations.

The design of a robust bandgap reference and voltage regulator is a challenge at high frequencies since the rectifier output will have a low amplitude, high frequency noise component (due to non-idealities in rectification), and a high amplitude, low frequency component due to the dynamic changes in the distance from external source, multipath fading and polarization mismatch from the antenna. These constraints require the circuits to have a good PSRR (Power Supply Rejection Ratio) for a broad range of frequencies, as well as good line and load regulation to minimize transients due to power supply fluctuations and load switching.

In addition to these typical considerations, it is useful to have a feedback mechanism from the headstage to the base station to estimate range and adaptively control the power radiated by the external source. Also, many implantable systems require a reference clock in the range of 10 KHz – 10 MHz for performing different functions (digital system clock, ADC/DAC clocks etc). The clock requirements are not as stringent as in high speed applications but good accuracy and low drift with reasonable jitter are expected.

Reducing average power is extremely critical for implantable systems to increase battery life or increase range for wireless systems. The radio transmitter is generally the most power hungry block in wireless applications. A huge reduction in average power can be achieved by transmitting in bursts using sleep-wake mode of operation while the measurement system continuously records data. For applications that do not require continuous operation, e.g., periodic pressure monitoring, the entire system can be powered periodically to save more power.

III. ASIC ARCHITECTURE

The architecture of the proposed wireless powering headstage ASIC module is shown in Fig. 1. This single chip system consists of a RF rectifier, an input power level detection block, a bandgap reference, a LDO programmable voltage regulator, and a power management block that incorporates a low jitter clock. This section discusses the motivation, design considerations and implementation of each component block in detail.

A. RF Rectifier

The discussion in [2] suggests that beyond an optimal number of stages, Power Conversion Efficiency (PCE) of the rectifier decreases even when the output voltage increases due to current drain in later stages. In the current work, an 8 stage modified Cockroft-Waltron Voltage multiplier topology using diode connected native MOS transistors achieves considerable efficiency. Fig. 2 shows the output voltage and PCE plotted as a function of input power for a 5KΩ load at 900MHz and 2.4GHz.

Zero barrier devices like Schottky diodes, will be the ideal candidate for higher PCE. Due to unavailability of Schottky diodes in most CMOS processes, the native MOS transistor with very low V_{th} (~0.1V) is chosen as an alternative to provide a design that is compatible with different foundries.

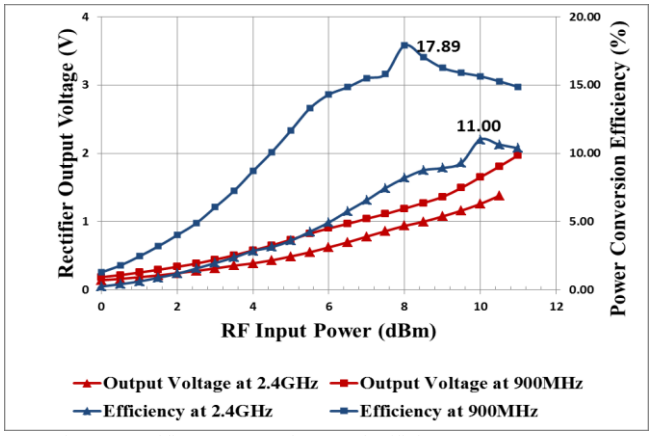

Fig. 2. Rectifier Output Voltage and Efficiency vs. Input Power

B. RF Power level Detection

The rectifier output voltage, V_{RECT}, is an effective indicator of the power delivered to the implant. A simple 1-bit comparator logic can be used to sense the input power level by comparing V_{RECT} to a reference level, V_{REF}, generated using the bandgap reference – see Fig. 1.

In the proposed system, the comparator is designed to trigger when V_{RECT} rises above 1.6V (since nominal supply for bandgap and regulator is 1.5V), using a V_{REF} of 0.67V, and thus producing a digital power level status bit which goes high when sufficient power is delivered to the implant and remains low otherwise. This bit can then be multiplexed along with the measurement data with negligible increase in bandwidth and transmitted to an external receiver, which controls the input RF power [7]. The output of the level detection circuit is shown in Fig. 3.

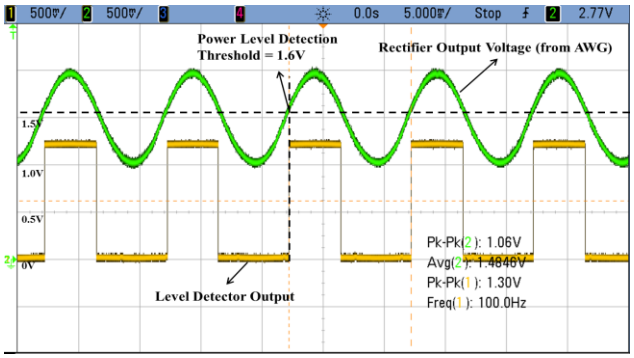

Fig. 3. Output of the Power Level Detection Circuit

C. Bandgap Reference and Voltage Regulator

In order to have a generic headstage that can be used in several applications, a 2-bit programmable Low Drop-Out (LDO) voltage regulator is designed to provide four output voltages – 1V, 1.2V, 1.3V or 1.5V. A cascoded bandgap reference, with good PSRR, is designed to obtain a voltage and temperature independent 0.67V reference for the regulator [4]. To allow sufficient voltage headroom even at supply voltages as low as 1.5V, low-V_{th} devices (~0.2V nominal) are used. 2.5V PMOS transistor is used for the pass-device alone to work at higher voltages. A folded cascode op-amp is used for better loop gain and PSRR. An external 4.7µF capacitor with an ESR of 1ohm is used to suppress load switching transients to below 100mV [4].

Digital programmability is achieved by enabling an NMOS shunt to ground at various resistance tap-points as shown in Fig. 1. The regulated supply for the digital decoder logic, which activates the NMOS shunts, is provided by a 1V reference from the bandgap circuit. Table I encapsulates the performance of the regulator and the bandgap reference.

D. On-chip Clock source

This work integrates a low power, process, voltage and temperature independent clock source that can be programmed to get frequencies from 125 KHz to 4 MHz. The clock generator has a three stage differential ring oscillator with symmetric load Maneates delay cells [8] for better phase noise and low jitter. A replica bias cell [9] uses negative feedback to adjust the bias current in the cell in order to negate changes in supply voltages. This keeps the delay insensitive to supply changes and hence keeps the frequency constant. This block also has a corner detection circuit that uses changes in leakage current of a MOSFET [10] to detect the process corner and set two flag bits accordingly (11 = FAST, 01 = TYPICAL, 00 = SLOW). The clock source uses these two bits to trim the current in the delay cells to account for process variations.

E. Power Management Block

To enable power save modes using periodic sleep-wake operation, a programmable duty cycle waveform, which can be used as the supply voltage for the power hungry blocks, was generated using the on-chip clock source and simple digital logic. A clock frequency of 2MHz was divided using a 15-bit counter and processed using combinational logic to generate an output waveform with a period of 15ms, and a duty cycle of 6.25%, 12.5% or 25% based on the 2 tune bits. The period of the waveform can be tuned using an external trimming resistor. This waveform was given to the gate of an NMOS sleep transistor, which was used for power gating the system. The sleep transistor was sized to drive upto 2mA, with a ground drop of 50mV. A 4:1 multiplexer was used to select three power saving modes or continuous powering mode. The different duty-cycle waveforms generated by the power management block are shown in Fig. 4.

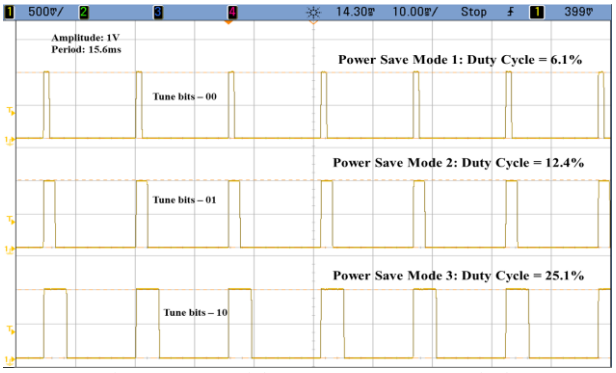

Fig. 4. Output of the Power Management Block

F. ASIC Fabrication Results

The proposed wireless powering headstage ASIC was designed and taped out using the TSMC 65nm process. The micrograph of the silicon die is shown in Fig. 5. The total die area is 910µm x 1060µm. Ten samples of the fabricated ASIC were measured and the silicon characterization results of the component blocks is summarized in Table I.

IV. System Demo: Case Study

To demonstrate the versatility of the proposed ASIC, the fabricated die was prototyped on an FR4 substrate board with a printed square loop antenna designed for 2.4GHz and a ground plane. A snapshot of the prototype system and measurement setup is shown in Fig. 5. This prototype was used to wirelessly power a programmable clock generator, a

capacitive pressure sensing system and a neural recording system for epileptic seizure detection. The maximum range of powering and average current consumption of these systems with/without using the power save mode is tabulated in Table II.

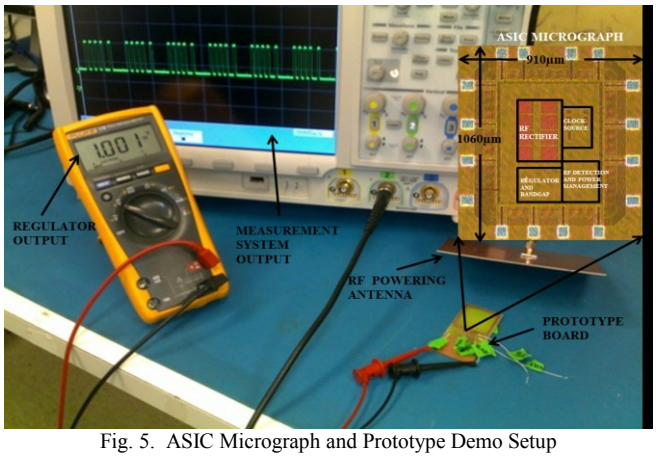

Fig. 5. ASIC Micrograph and Prototype Demo Setup

V. Conclusion

A single chip ASIC solution for a generic wireless powering headstage, with digitally programmable features, and using only 2 external components is presented. The motivation for various design considerations was discussed and the implementation of different component blocks elaborated. The measured results and overall performance of the ASIC was tabulated. Finally, the fabricated headstage was used to wirelessly power two different implantable measurement systems as a proof of concept. The rectifier PCE can be improved at higher frequencies, and lower input powers in order to drive systems with higher load currents, and the external regulator load capacitor can be avoided using an on-chip compensation scheme.

TABLE I
Headstage ASIC Characterization Results

Specification	Value
Voltage Regulator	
Regulation	1.77% (Line), 3.2% (Load)
Quiescent Current	80-120µA
Dropout Voltage	100mV
PSRR	-42dB
Maximum Load Current	4mA
Output Voltage	1V, 1.2V, 1.3V, 1.5V
Input Voltage Range	1.5V – 2.5V
Settling Time	7.5µs
Bandgap Reference	
Current Consumption	38.2µA
Reference Voltages	1V, 0.67V
Power Supply Range	1.5V – 2.5V
PSRR	-46dB
Supply Sensitivity	0.86% for 0.67mV, 5% for 1V
Clock Source	
Nominal Supply Voltage	1V
Current Consumption	107µA for 1V, 125KHz
Output Frequency	120.98KHz
Duty Cycle	47% ± 0.55%
Clock Jitter	0.45µs

TABLE II
Measurement System Demo Results

Specification	Value
Programmable Clock Source (no VCO)	
Supply Voltage	1.2V
Current Consumption – Mode 1*	222µA for 1.2V, 500KHz
Current Consumption – Mode 2*	67µA for 1.2V, 500KHz
Total Power Savings	69.8%
Powering Range (1W output) **	15cm (900MHz), 6cm (2.4GHz)
Single Channel Neural Recording System with VCO	
Supply Voltage	1.5V
Current Consumption – Mode 1*	294µA (System), 1.2mA (VCO)
Current Consumption – Mode 2*	294µA (System), 312µA (VCO)
Total Power Savings	59.4%
Powering Range (1W output) **	11cm (900MHz), 4cm (2.4GHz)
Capacitive Pressure Measurement System with VCO	
Supply Voltage	1V
Current Consumption – Mode 1*	37µA (System), 760µA (VCO)
Current Consumption – Mode 2*	37µA (System), 195µA (VCO)
Total Power Savings	70.9%
Powering Range (1W output) **	22cm (900MHz), 8cm (2.4GHz)

*Mode 1 – Power Saving Mode Disabled – Continuous Supply Voltage
*Mode 2 – Power Saving Mode Enabled – 25% Duty Cycle Supply
**Distance between external powering source and prototype system when the level detector output changes from high to low i.e. when power delivered is just sufficient.

Acknowledgment

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