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A Low-Power High-Sensitivity CMOS Mixed-Signal Seizure-Onset Detector

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Abstract— **In this paper, we present a new seizure detection algorithm and the associated CMOS circuitry implementation. The proposed low-power seizure detector is a good candidate for an implantable epilepsy prosthesis. The device is designed for patient-specific seizure detection with a one variable parameter. The parameter value is extracted from a single seizure that is subsequently excluded from the validation phase. A two-path system is also proposed to minimize the detection delay. The algorithm is first validated using MATLAB® tools and then implemented and validated using circuits designed in a standard 0.18-µm CMOS process with a total power dissipation of 7.08 µW. A total of 13 seizures from two drug-resistant epileptic patients are assessed using the proposed algorithm and resulted in 100% sensitivity and a mean detection delay of 9.7 s after electrical onset.**

I. Introduction

Neural signal recording, automatic signal processing and responsive stimulation are novel approaches for developing new prosthetic devices to treat epilepsy. Implantable devices are an interesting alternative for drug-resistant epileptic patients who are not candidate for (or have failed) epilepsy surgery. Proof-of-concept experiments have demonstrated possible suppression of a seizure in its early phase using focal treatment (i.e. focal electrical stimulation, cooling or drug delivery) [1]. Efficiency of this type of focal treatment which is delivered in response to a seizure depends on high quality intracerebral electroencephalographic (icEEG) acquisitions and accurate seizure onset detection [2].

Electrophysiological patterns vary from patient to patient. The most frequently encountered ones are the low-voltage fast-activity, high-voltage fast-activity and rhythmic spiking patterns [3]. This ictal icEEG changes at onset evolve dramatically in frequency and amplitude, spreading regionally and/or to distant areas with accompanying clinical manifestations. Electrical seizures (i.e. without clinical accompaniment) are frequently encountered in intracerebral recordings of patients with pharmacoresistant partial epilepsy. In some patients, they may warrant intervention if for example they are rare, long and/or frequently degenerate into an electroclinical seizure. In others, it might be preferable to ignore them if they are brief (few seconds only), remain very focal (infrequently evolving into an electroclinical seizure) and so frequent that they would rapidly deplete the battery from 'unnecessary' triggered focal treatment [3]. Seizure detection parameters must adapt to these individual variables.

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In the last decade, there has been a growing interest for developing seizure detection algorithms [1], [4]-[6]. In order to increase detection sensitivity and specificity, these algorithms use heavy mathematical computations on desktop computers. Unfortunately, these algorithms cannot be employed in a low-power implantable device for responsive focal treatment of epilepsy given the complex computational signal processing required. Heavy computations are linked to large power dissipations and as a result, a lower battery lifetime. The RNS system (Neuropace Inc.) is the only responsive device for focal treatment of pharmacoresistant epilepsy which has been submitted for FDA approval. The RNS system employs three detection tools (area, line-length and half-wave) and physicians configure the parameters for early seizure detection or for detection of more subtle changes that occur over several seconds [2].

Several other power-aware algorithms have been reported in the open literature [4][5]. In [4], the algorithm is based on event detection with a CMOS circuit realization that miniaturizes only the post processing blocks, while excluding the front-end amplifier and comparators from the detector integrated circuit and power estimation. In [5], multiple-window detection is used and the circuit is fully miniaturized in a CMOS process. Window detection [5], unlike event detection [4], has the advantage of minimizing missed seizures (false negatives), and/or the declaration of seizure-unrelated spikes/events as seizures (false positives). However, a multi-window signal detection results in additional hardware and complex optimization of the threshold parameters needed for a working device. In this paper, we propose a single-window seizure onset detection algorithm that combines the benefits of window detection and the simplicity of optimizing the threshold parameters of a single window. Additionally, the proposed algorithm will be shown to be totally amenable to miniaturization through monolithic integration of the front-end amplifier and comparators with the rest of the detector circuit blocks. Another advantage of the proposed circuit is that the post processing of the windowed data is done exclusively in the digital domain, making it easily synthesizable, supply scalable, and immune to noise.

This paper is organized as follows: Section II briefly highlights the algorithm and its working principles. Section III presents the hardware realization of the proposed system and discusses its building block circuits in more details. Clinical validation of the algorithm and the hardware are then highlighted in Section IV. Concluding remarks are provided in Section V.

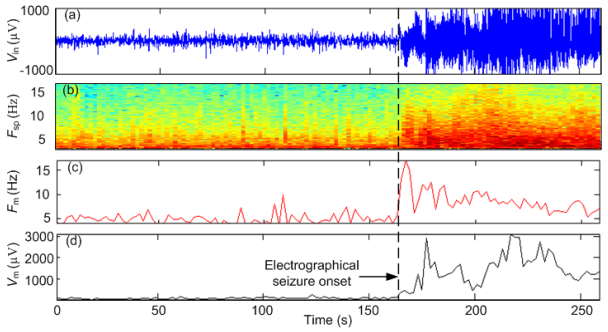

Fig. 1. IcEEG recording analysis: a) neural signal voltage V_{in} recorded by depth electrode, b) spectrogram F_{sp}, c) mean frequency F_m, and d) mean amplitude V_m.

II. Algorithm

The proposed algorithm is designed to detect icEEG seizures characterized by a progressive increase in amplitude and abrupt frequency changes. Fig. 1(a) shows an icEEG recording (V_{in}) from a drug-resistant patient. Time-frequency analysis at seizure onset (165 s) shows a sudden change in the spectrogram F_{sp} (Fig. 1(b)) and the mean signal frequency F_m (Fig. 1(c)). Moreover, the mean amplitude of signal V_m (Fig. 1(d)) incurs a progressive increase in its magnitude.

Previous work specifically use between three [5] and six [6] non-overlapping windows with closely spaced thresholds to track the increasing excitation in the signal amplitude. The optimization of the corresponding six and twelve reference voltages is a challenging estimation task. Additional parameters that also need to be optimized include time-window length and time-based thresholds that are tuned for each patient. In an effort to minimize the number of reference voltages and time threshold optimizations, we focus our efforts on one reference voltage and one constant time window. An illustration of the algorithm flowchart is shown in Fig. 2(a). The voltage window is set by two threshold levels, V_{th1} and V_{th2}. A single 2 min long seizure is used per patient to determine the values of V_{th1} and V_{th2}. V_{th1} is set to the mean of the icEEG signal. Hence only V_{th2} needs to be determined. A progressively increased amplitude (as one would expect shortly after seizure onset) manifests itself as more occurrences of the signal outside, and less inside, the window (i.e. lower count of logic ones). Here we define a parameter C_{th} as the threshold count when the number of occurrences of the signal $C_{s,i}$ inside the defined limits drops. We emphasize on the threshold count as opposed to a threshold voltage for declaring a seizure since the post processing takes place purely in the digital domain. The algorithm output for an example seizure is shown in Fig. 2(b)-(d). The first seizure detection is issued by the algorithm at 172.5 s, i.e. at a delay of 7.5 s with respect to the signal analysis shown in Fig. 1. The signal count $C_{s,i}$ is directly related to the window length chosen (fixed at 5 s in this work). A longer window results in a higher sensitivity at the expense of a larger detection delay. In order to maintain the high sensitivity while reducing the detection delay, we propose relying on a two-path system as described in Section III.

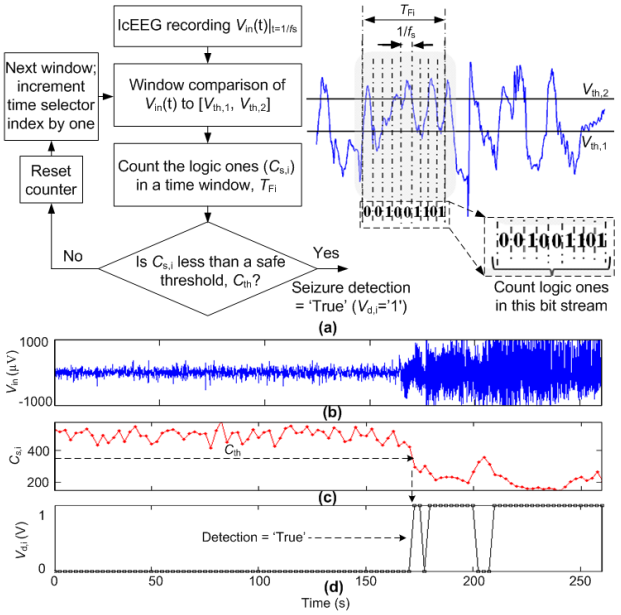

Fig. 2. Illustration of the algorithm: a) flowchart, and evaluation showing the b) icEEG recording $V_{in}(t)$, c) ones or 'true' count $C_{s,i}$ corresponding to the signal $V_{in}(t)$ within the thresholds, and d) detection output $V_{d,i}$.

III. Proposed System and Circuit

A. System design

A system-level block diagram of the seizure detection algorithm is shown in Fig. 3. It consists of a front-end amplifier to amplify the icEEG signal V_{in} from µV to mV levels. It is then followed by window detection realized with two threshold comparators. A third comparator (not shown in Fig. 3 for simplicity) with threshold voltage V_{th3} is needed to account for the negative parts of the signal waveform. Given that the mean of the icEEG recordings is equal to zero, V_{th3} is automatically deduced as the symmetrical value of V_{th2} with respect to ground (V_{th1}). The comparators outputs are then fed serially to an asynchronous counter. The number of bit stream in this work is equal to 1k given that the pre-chosen window is 5 s and the sampling frequency of the icEEG data is f_s = 200 samples/s. The counter counts the number of logic ones $C_{s,i}$ present in the bit stream and compares it to a predefined safe threshold count, C_{th}, using all-digital counter and magnitude comparator. A progressive rise in amplitude results in a transition from 1 to 0 in the digital comparator output at the end of the time frame, and therefore such a transition signal indicates an imminent seizure. The detection decision is evaluated at the end of the time frame since the counter has to finish accumulating/counting the number of logic ones in the time window selected before comparing to C_{th}. As a result, a large window will inevitably correspond to a large latency. To minimize the detection delay, two parallel paths are incorporated in the design, each synchronized to the same clock, f_s, but with time frame windows that have an offset (overlap) of half a window length with respect to each other (T_{F1} and T_{F2} in Fig. 3). The flag that a seizure is imminent is raised when either of the two paths system issues a warning. Each path has its data valid at the end of the

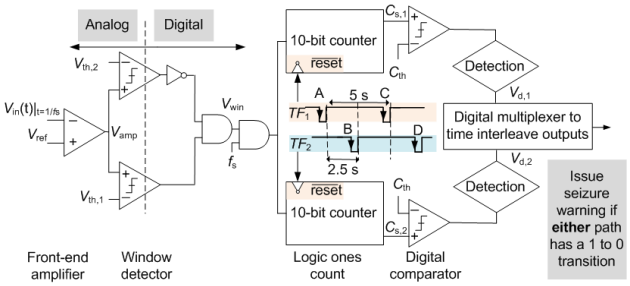

Fig. 3. System level design of the proposed algorithm: amplification, window detection, and a two-path system with 50% time offset between T_{F1} and T_{F2} are illustrated.

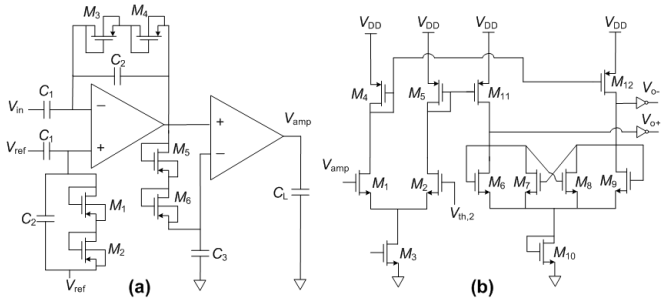

Fig. 4. Schematic diagrams: a) front-end amplifier and b) comparator circuits.

window, i.e., points A and C for T_{F1} and B and D for T_{F2}, as shown in Fig. 3. This corresponds to a worst case detection delay of 5 s per path, but both combined will give a detection delay of 2.5 s given the time multiplexed nature of T_{F1} and T_{F2}. This has the advantage of reducing the latency of the detection algorithm, at the expense of additional hardware. However, this hardware consists of digital counters, a digital comparator, and a detection logic, all of which occupy little area overhead and consume negligible static power (the front-end amplifier and window comparators are shared by both signal paths, and these blocks dominate the static power dissipation). Of course, the case can be generalized to more multiplexed paths to reduce the detection delay even further.

B. Circuit design

The proposed detector, shown in Fig. 3, is designed in a monolithic circuit as described below.

1) Front-end amplifier and comparator

Due to the low-amplitude of the signal recorded by the intracranial electrodes, low-noise amplification precedes the rest of the detection steps of window comparison and seizure decision circuit. In order to suppress DC components, which could saturate the amplifier, and attenuate high-frequency components beyond 50 Hz, a low-noise amplifier with a bandpass frequency response is used. The amplifier is composed of two amplification stages. The first one [7] is designed to achieve a low gain of 10 V/V to keep the capacitor ratio (C_1/C_2) minimal, therefore saving silicon space. The very low-frequency pole (high-pass response) is obtained with a large resistor (~10^{14} Ω) integrated using a pseudo-resistor [7] (Fig. 4 (a)). The second stage consists of another amplifier stage with additional DC rejection based on the feed-forward cancellation technique [8]. The overall amplifier 3-dB bandwidth is ~ 0.5 to 215 Hz and has an overall gain of 62 dB. Although not included in the current design, an additional low-pass filter could be added at the output of the amplifier to decrease the bandwidth from 215 Hz to 50 Hz, which then also serves as an attenuator for the 60 Hz line interference.

The comparator (Fig. 4(b)) is realized using a low-power standard pre-amplifier stage followed by a positive feedback regenerative latch for fast response time.

2) Digital signal processor

The counter and 10-bit digital comparator are integrated using digital blocks from the standard-cell libraries available in the TSMC 0.18-µm CMOS technology. The asynchronous counter consists of ten JK flip flops, and is activated at the beginning, and is reset at the end of the 5 s time frame. Just before resetting the counter output, a digital comparator is activated to generate the comparison decision with respect to C_{th}. The 10-bit digital comparator is realized using 3 cascaded stages of 4-bit logic comparators.

IV. Results

1) Clinical methods and case studies

Two patients (age: 24 and 36) with intractable epilepsy underwent an intracranial study to better delineate the epileptogenic zone for eventual epilepsy surgery. Depth, subdural grid and strip electrodes were implanted in both patients. Following the implantation, a long-term (~2-3 weeks) video-EEG recording was performed on the patients in the epilepsy monitoring unit (Notre-Dame Hospital, Montréal). During this period, several brief electrical seizures and electroclinical seizures were recorded and marked by an epileptologist (DKN). Case 1 had intracranial electrodes implanted in temporal and insular regions. All of his seizures originated from the right medial temporal lobe (hippocampus). Electrographically, seizures were characterized by an initial low-voltage tonic alpha activity evolving into rhythmic spiking. Fig. 5 shows the electrographic seizure as recorded from the electrode contact in the epileptogenic zone. Based on video analysis of the seizure, the patient reported feeling an aura 37 s after electrical onset. Altered consciousness occurred a few seconds later. Case 2 underwent a left frontotemporal craniotomy with insertion of subdural strip and grid electrodes placed over lateral frontal, orbitofrontal and temporal regions. During the evaluation, seizures were found

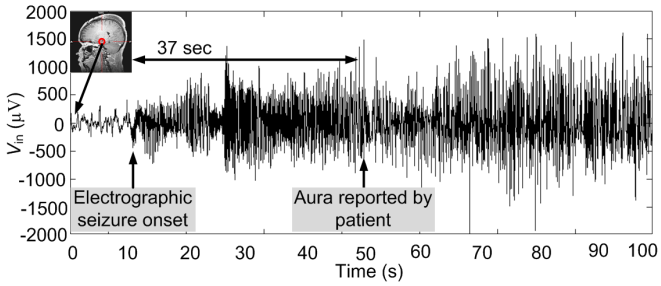

Fig. 5. The icEEG recording from the two electrode contacts positioned over the epileptogenic zone and the corresponding behavioral relation with the electrographical signal for case 1.

TABLE I. PERFORMANCE SUMMARY

Parameter	Value
*Average latency for both patients**	μ= 9.7 s, σ= 4.2 s
*Average sensitivity**	100%
Power Dissipation	7.077 µW
Bio-Amplifier & Biasing	91.95%
Comparators & Biasing	7.91%
Digital Detection	0.14%
Technology (supply)	0.18 µm CMOS (1.8 V)

* Using 13 seizures (2 patients), and 19 non-seizure data sets.

to originate from the left lateral temporal neocortex. Electrographically, seizures were characterized by a diffuse slow wave followed by desynchronization and regional low-voltage high-frequency activity. Video analysis of seizures indicated that first over clinical manifestations generally occurred 30 s after electrical onset.

2) *Validation of the proposed detector*

A total of 32 data sets of short recordings (~1-2 min long) from the contact showing earliest ictal changes during the seizures, 13 of which corresponded to seizures were used in the validation phase. The remaining 19 data sets corresponded to variable patient activities. Of particular interest were brief electric seizures (2-3 s) and sleep patterns that were specifically included to test the algorithm capabilities to rule out false positives. In this particular example, the algorithm was specifically set to ignore brief paroxysmal discharges in order to minimize the need for intervention as the clinician found that a high percentage of them did not necessarily progress into an electroclinical seizure. The selected data sets were imported offline into MATLAB® to validate the algorithm devised, followed by Spectre® simulations (using Cadence®) for circuit verification. Results from both cases combined are illustrated in Fig. 6. A sensitivity of 100% with a mean detection latency of 6.9 s (σ=1.6 s), 14.1 s (σ=2.8 s), and 9.7 s (σ=4.2 s) are achieved for cases 1, 2, and both combined, respectively. The system performance is summarized in TABLE I and compared to [6] in TABLE II.

Given the high speed of operation in advanced submicron CMOS processes, the circuit implementation in 0.18-µm standard CMOS introduces negligible delays (nanoseconds range) compared to the algorithm delay (seconds range). An example illustrating the integrated circuit response from one seizure is shown in Fig. 7. Here, $V_{d,1}$ in Fig. 3 (corresponding to the output at the end of T_{F1}) issues the first 'true' seizure detection output, several seconds before clinical manifestation.

V. CONCLUSIONS

A low-complexity seizure onset detector has been proposed.

TABLE II. PERFORMANCE COMPARISON

Parameter	[6]	This work
Parameters optimized	5 to 7	**1**
Design complexity	High	**Low**
Sensitivity to seizure	**100%**	**100%**
Mean Latency	**6 s**	9.7 s
Power Dissipation	**6.71 µW**	7.08 µW

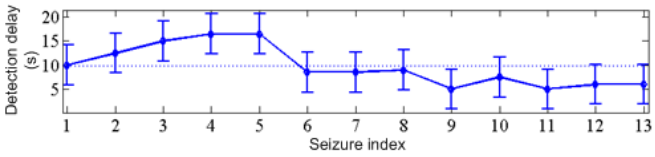

Fig. 6. Algorithm detection latency: the first 5 seizures correspond to case 2, whereas the remaining 8 seizures are for case 1. Superimposed is the error bar for the delay standard deviation and the overall mean delay (dotted line).

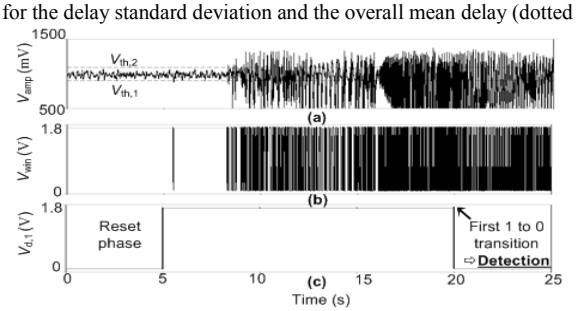

Fig. 7. Circuit simulations for one example seizure showing a) amplified icEEG signal with threshold levels superimposed, b) window comparators output, and c) seizure detector output from path 1 (corresponding to T_{F1}).

Value of one threshold voltage (V_{th2}) is extracted per patient, while other parameters are kept constant (window length, comparison threshold C_{th}), minimizing the overhead and complexity associated with multi-parameter optimization. The mapping to the system level includes multiplexing the detection decisions of two-paths (that share the same bio-amplifier and window comparators) to reduce the detection delay of the proposed algorithm. The algorithm is validated in MATLAB® and the hardware implementation in a 0.18-µm CMOS process is verified using Spectre® simulations. The detector is tested on icEEG recordings from two epileptic patients, and a sensitivity of 100% is achieved with a 9.7 s mean detection delay. Future work includes validating the proposed algorithm on a more elaborate database of patients and implementing the physical hardware.

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