33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

Micro-Watt Building Blocks for Biomedical RF Tranceivers

T. Taris, H. Kraimia, J-B. Begueret and Y. Deval, *IEEE Members*

***Abstract*— The development of Wireless Body Area Network (WBAN) is a key point enabling the mobility health. Among the most critical constrains in WBAN implementation is the power consumption of wireless featuring nodes. This work focuses on the development of ultra low power radio building blocks dedicated to 2.4 GHz ISM band. A novel design approach based on device optimization is first presented. It is then applied to the implementation of a Low Noise Amplifier (LNA) and a mixer in a 0.13 µm CMOS technology.**

The LNA provides a 13.1 dB gain and a 5.3 dB NF for a 60 µW/0.4 V power consumption. The mixer achieves a conversion gain of 17.5 dB and a NF of 12 dB at 0 dBm LO power. It consumes 350 µW for a 0.8 V supply.

I. Introduction

The aging population in many developed countries and the rising costs of health care have triggered the introduction of novel technology-driven enhancements to current health care practices. Recent advances in electronics have enabled the development of small and intelligent (bio-) medical sensors which can be worn on or implanted in the human body enhancing the so called eHealth. These sensors need to send their data to an external medical server where it can be analyzed and stored. Using a wired connection for this purpose turns out to be too cumbersome and involves a high cost for deployment and maintenance. However, the use of a wireless interface enables an easier application and is more cost efficient [1]. The patient experiences a greater physical mobility and is no longer compelled to stay in a hospital. This evolution of eHealth to mobile Health (mHealth) relies on the development of Wireless Body Area Networks, Fig. 1. A personal device collects bio-data from WBAN and broadcasts them for analyzing by a medical staff and database storage.

The WBAN which is expected to go with patients in daily life is the core of mHealth. The current development relies on various points of investigation such as: the energy, the quality of service, the reliability, the usability as well as the privacy and security. But the top priority remains the power consumption of the nodes. Indeed the small form factor of sensors and actuators featuring the body network puts a hard constraint on the energy management.

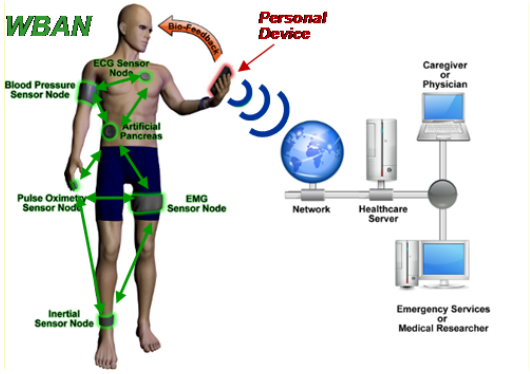


Fig. 1. Data collect and broadcast in mobility Health

The most consuming part in a WBAN node is the radio which provides the communications with the network. As well, extensive research focuses on the design and implementation of Ultra Low Power (ULP) Radio-Frequency Front End (RFFE) in CMOS tehnology. This work investigates the development of ULP building blocks featuring the radio receiver (Rx) part. A Low Noise Amplifier and a mixer implemented in a 0.13 µm CMOS technology are reported. At first a figure of merit (FOM_{RFLP}) suited for ultra low power RF is discussed through the measurement of a single device. Then the circuit designs, based on maximizing FOM_{RFLP}, are detailed. The experimental results are presented and discussed regarding the interest of the proposed design methodology.

II. Device skills and circuit Design

A. Low Power RF metric

An effective way of minimizing power consumption in a MOS transistor is to bias it in weak inversion region where the transconductance to drain current ratio (g_m/I_D) is maximum [5]. This approach is extensively used in analog circuit design whose the operating frequency is far from f_T, the technology cutoff frequency. In RFIC design the effect of parasitics, such as C_{gs} in a MOS transistor, is of major importance. This phenomenon represented by f_T plays a key role in the optimization of RF building blocks. Also, the tradeoff between RF performances and the current consumption is better represented by the FOM_{RFLP} proposed in the eq (1) [2]:

$$FOM_{RFLP} = \frac{g_m \cdot f_T}{I_D} \qquad (1)$$

Fig. 1 depicts FOM_{RFLP} of a low leakage NMOS transistor in a 0.13µm CMOS technology from ST Microelectronics. The device features a 60µm/0.13µm

with 12 fingers and a double gate access. This curve figures out FOM_{RFLP} is maximized when the transistor operates in moderate inversion region. This statement is the starting point of the low power RF design methodology developed in this work.

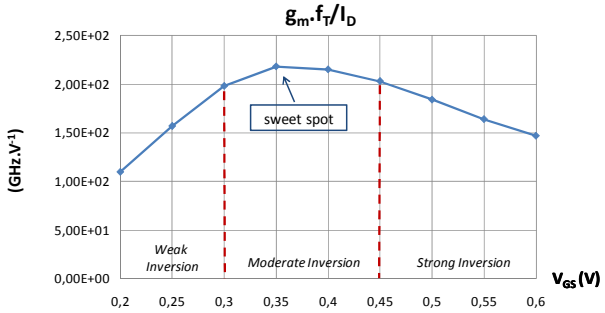


Fig. 1. $g_m f_T$-to-current ratio, FOM_{RFLP}, for a 60/0.13µm 12 fingers low leakage NMOS RF transistor

B. Circuit Design

Low Noise Amplifier

The low transconductance (g_m) performed in moderate inversion mode requires active load topologies to achieve acceptable gain. Among the various configurations based on a single stage amplification, the self biased inverter (SBI) exhibits the largest gain bandwidth product, Fig. 2. It also yields a larger gain since the overall transconductance, g_{mT}, is almost twice the one of a single transistor, g_{mN}.

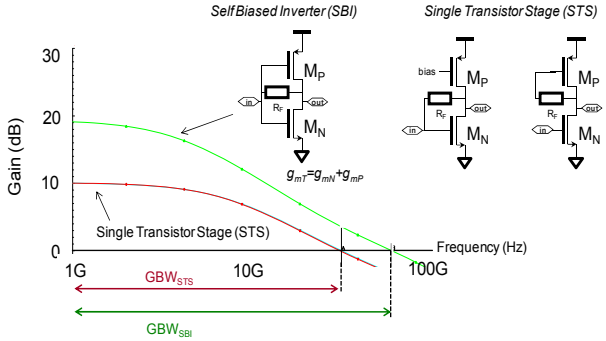


Fig. 2. Gain Bandwidth product (GBW) of single stage configurations with active load

Fig. 3 presents a simplified schematic of the LNA whose device sizes are reported in Fig. 4(a). The core is based on a self biased cell, its supply voltage is controlled by a 3 bits DAC. To further reduce VCC, the decoupling capacitor C_1 is introduced between the gate of M_1 and M_2. The buffer provides a 50Ω output matching through (C_{m1}, C_{m2}, L_{pk}) and holds on the LNA gain in measurement.

The input impedance is expressed in eq (2). The real part is supported by R_F and the capacitive divider sets by C_{gsT} and C_L. The imaginary part can be cancelled out through L_g.

$$Z_{in} = \frac{C_L.R_F}{C_{gsT}+C_L} + j\frac{g_{mT}.R_F.C_L}{(C_{gsT}+C_L).\omega^2} \quad (2)$$

With $C_{gsT}= C_{gs1} + C_{gs2}$ $g_{mT}= g_{m1} + g_{m2}$ $C_L= C_{gs3} + C_{tune}$

The minimum noise figure, derived in eq (3), is lowered for a maximum value of R_F. This one remains limited by the input matching conditions according eq (2).

$$F_{min} = 1+\frac{4\gamma}{\alpha} g_{mT} R_s (\frac{\omega}{\omega_T})^2 + \frac{R_s}{4R_F} \quad (3)$$

Where $\alpha=g_m/g_{d0}$ and γ is the thermal noise coefficient

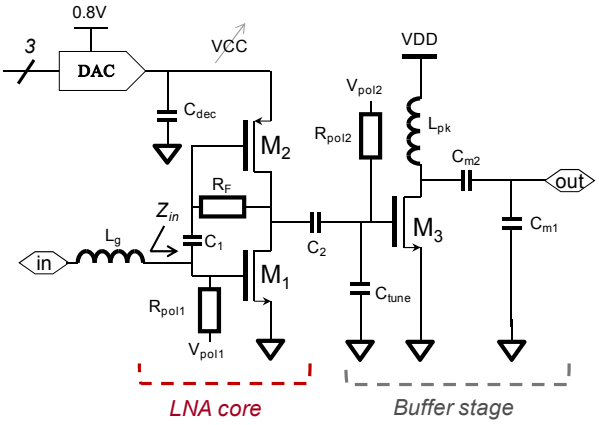
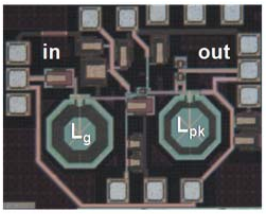


Fig. 3. Simplified schematic of the circuit

The circuit takes place within a 0.63 mm² silicon area, Fig. 4 (b). The input and inter-stage matching based on capacitive dividers are very sensitive to the circuit routing. The fine tuning of the circuit has been performed with a customized model of MIM capacitors including the parasitic capacitor formed with the substrate and the bottom plate.

$(W/L)_1$	(20/0.13) µm
$(W/L)_2$	(30/0.13) µm
$(W/L)_3$	(50/0.13) µm
C_{tune}	220 fF
L_{pk}	3.6 nF
L_g	10 nH
R_F	4 KΩ



(a) *(b)*

Fig. 4. Device sizes *(a)* Chip Micrograph *(b)* of the LNA.

Mixer

The conventional architecture of a single balanced mixer is depicted in Fig. 5(a). It uses a single NMOS transistor, M_{RF}, in the transductor stage. This configuration implies a tradeoff for I_{mix}. A large DC current is mandated to lower the noise figure and to increase the transconductance of M_{RF}. Whereas M_{LOi} need a small value of I_{mix} to achieve perfect switching and so reduce their noise contribution.

To break this compromise a technique namely current bleeding [3] stacks a transistor above M_{RF} to current supply the input stage. I_{mix} is no longer shared between

switching and transductor stages, the sizing of M_{LOi} becomes independent. In the circuit reported in Fig. 5(b), M_{RF2} provides the bleeding current. It also contributes to the RF signal amplification since it is SBI connected. It is a novel approach of the technique that is applied to the mixer reported in this work. The transistors M_{RFi} are biased in moderate inversion to maximize FOM_{LPRF}.

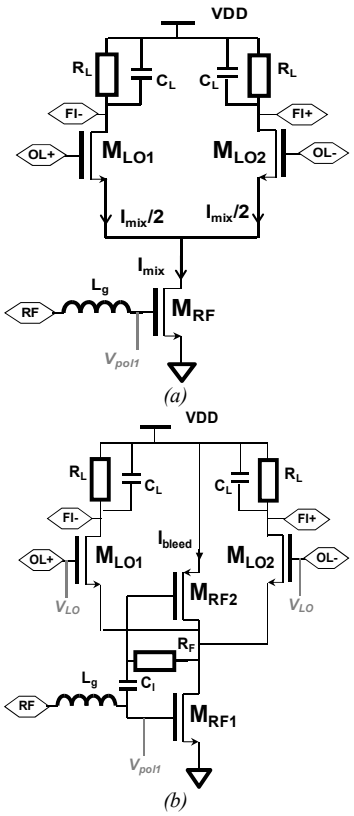
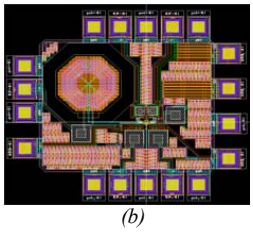


Fig. 5. Single balanced mixer (a) Bleeding current reuse mixer (b)

The values of the components featuring the mixer are summarized in Fig. 6(a). A snapshot of the layout is presented in the Fig. 6(b). The circuit also implemented in 0.13µm CMOS takes place within a 0.745 mm².

$(W/L)_{RF1}$	(14/0.13) µm
$(W/L)_{RF2}$	(24/0.13) µm
$(W/L)_{LOi}$	(6/0.13) µm
R_L	5 KΩ
C_L	2 pF
L_g	12 nH
R_F	5 KΩ

(a)



(b)

Fig. 6. Device sizes (a) layout (b) of the bleeding current reuse mixer

III. Experimental Results

The LNA has been measured with a GSG probe test bench. V_{pol1} is fixed to 320 mV and VCC, controlled by the 3 bits DAC, varies from 400 to 600 mV. These biasing conditions ensure that the LNA core operates in the region of moderate inversion close to the sweet spot. The buffer providing a 0.6 dB gain consumes 1.8mA under 0.8V, though its contribution has been de-embedded from the reported results which only concern the LNA core.

First are reported the input matching and gain in Fig. 7. From 2.45 to 2.55 GHz, the S_{11} is kept lower than −10dB for any value of VCC.

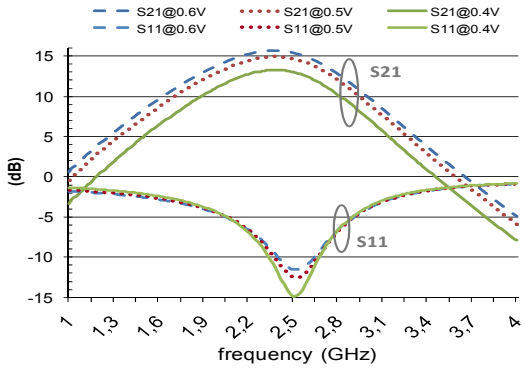


Fig. 7. S_{21} and S_{11} for various VCC

The circuit is unconditionally stable in a 0.5 to 10 GHz band. The stability factor K, calculated with S parameter results, is higher than 2.2 over the entire frequency range.

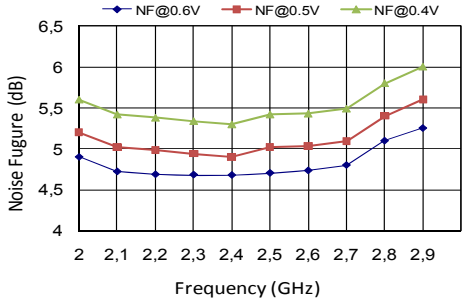


Fig. 8. NF for various VCC

The gain represented by S_{21}, Fig. 7, reaches a maximum of 15.7 dB when VCC is 0.6 V. It is reduced to 15 dB@0.5V and 13.1 dB@0.4V. Hence the self inverter topology performs a large voltage gain under low voltage supply. For VCC lower than 0.4V the S_{21} drops below 10dB. So it is defined as the lower supply providing acceptable amplification.

The Noise Figure (NF) presented in Fig. 8 has been measured with a HP 8970B NF meter. To enhance the accuracy of the measurement, the span is limited to 1 GHz centered at 2.5 GHz. The flat band response of the NF is a typical behavior of resistive feedback topologies. The minimum obtained at 2.4 GHz is 4.6dB@0.6V, 4.9dB@0.5V and 5.3dB@0.4V.

The power consumption of the mixer is 350µW excluding the buffer. VDD and V_{pol1} are fixed to 800mV and 380mV, respectively, to operate the transductor stage in moderate inversion region. V_{LO} sets the V_{GS} of switching transistors, M_{LOi}, to their threshold voltage V_{th}, around 280mV.

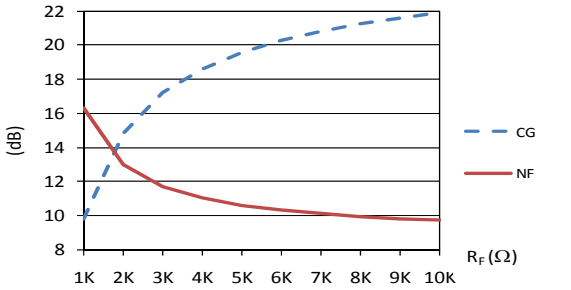


Fig. 9. Mixer NF and conversion gain versus R_F at 10 MHz IF. P_{OL} is 2 dBm

The fine tuning of the circuit has been performed through post layout simulations. Fig. 9 figures out the conversion gain and noise figure for various values of the feedback resistance R_F. Both characteristics improve increasing R_F. According eq. (2) R_F also contributes to tune the input matching in SBI configuration. As well a tradeoff needs to be set to achieve a good input matching, a large CG and a low NF. The S_{11} of the mixer is drawn in Fig. 10 versus R_F. Accounting for the technology drift and packaging mismatch, the targeted S_{11} should not exceed -20 dB at 2.4GHz. R_F has been so fixed to 5 kΩ in the implemented circuit.

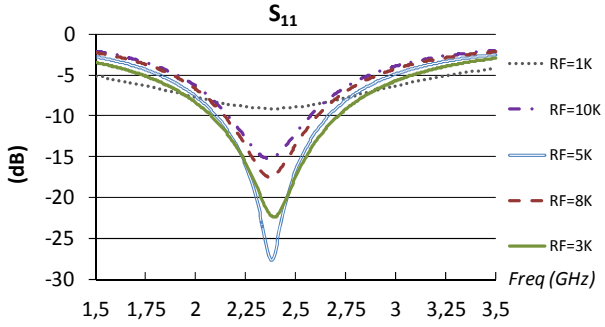


Fig. 10. Mixer input matching S11 for various R_F

The maximum of conversion gain (CG), 21 dB, and minimum noise figure (NF), 9.5 dB, are obtained for a LO power of 5 dBm, Fig. 11. Considering the Ultra Low Power context of WBAN, we assume that the nominal operating conditions of the mixer rather correspond to a 0 dBm LO power. Under this assumption the CG and NF are 17.5 dB and 12 dB respectively

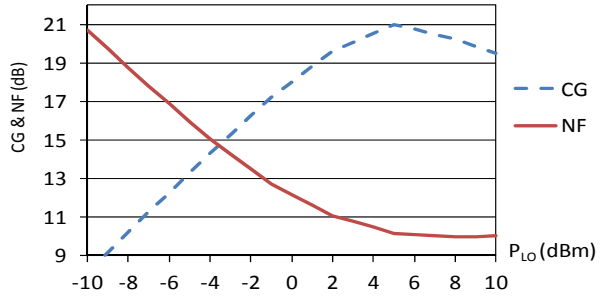


Fig. 11. Mixer NF and conversion gain versus OL power at 10 MHz IF R_F is 5KΩ and f_{RF} is 2.4 GHz

The overall characteristics of the mixer and the LNA are summarized in Table I. They are consistent with RF requirements for wireless short links [7]. It even avoids the need of a LNA for some cases reducing the power consumption of the RFFE to only 350 µW. A post layout simulation of the RFFE, combining the LNA and the mixer, demonstrates a 30 dB gain and a NF of 6.1 dB for a power budget of 410 µW.

TABLE I
PERFORMANCES OF BLEEDING CURRENT REUSE MIXER

LNA	
P_{cons}/VDD	60µW/0.4 V
S_{21}	13 dB
NF	5.3 dB
ICP1/IIP3	-19/-12 dBm
Mixer	
P_{cons}/VDD	350 µW/0.8 V
Conv. Gain	17.5 dB
NF	12 dB
ICP1/IIP3	-18/-12 dBm
P_{OL}/f_{OL}	0 dBm/2.41 GHz
f_{FI}	10 MHz

IV. CONCLUSION

Addressing the challenge of very low power RF, this work proposes a novel approach to develop optimized key building blocks. The critical step aims maximizing the $g_m f_T$-to-current ratio in MOS transistor to yield the best tradeoff between RF performances and current consumption. A LNA and a mixer dedicated to 2.4 GHz ISM band has been implemented so. For a 0.4 V supply, the LNA achieves a gain and a NF of 13.1 dB and 5.3 dB. The mixer supplied by a 0.8 V provides a 17.5 dB gain and a 12 dB NF for a LO power of 0 dBm. The power consumptions, 60 µW and 350 µW of the LNA and Mixer, respectively, enable the "micro-Watt radio" expected in WBAN development.

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