33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

Approaches for the Efficient Extraction and Processing of Biopotentials in Implantable Neural Interfacing Microsystems

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Abstract—**The accelerating pace of research in neurosciences and rehabilitation engineering has created a considerable demand for implantable microsystems capable of interfacing with large groups of neurons. Such microsystems must provide multiple recording channels incorporating low-noise amplifiers, filters, data converters, neural signal processing circuitry, power management units and low-power transmitters to extract and wirelessly transfer the relevant neural data outside the body for computing and storage. This paper is reviewing several electronic recording strategies to address the challenge of operating large numbers of channels to gather the neural information from several neurons within very low-power constraints.**

I. Introduction

NOWADAYS, neural interfacing microsystems capable of continuously monitoring large groups of neurons are being actively researched by leveraging the recent advancements in neurosciences, microelectronics, communications and microfabrication. Implantable neural microdevices are pursuing two critical objectives: 1) replacing hardwired connections with a wireless link to eliminate cable tethering and infections, 2) enabling the local processing of neural signals on a chronic basis to improve signal integrity.

A suitable interface to the cortex must enable chronic utilization and high-resolution through the simultaneous sampling of the activity of hundreds of neurons. But, the requirement of implantability places severe limitations on size, weight, and power consumption of implants in order to limit invasiveness and heat dissipation in surrounding tissues. A major effort has recently been directed towards designing neural recording circuitry consuming very few microwatts per channel by leveraging several approaches including low-power circuit techniques and smart data/power management. Indeed, low-power sensory circuits, energy-efficient system-level architectures and dedicated on-chip management strategies are fundamental for achieving high-resolution neural recordings while addressing the stringent requirements for implantability.

In this paper, we review the state-of-the-art approaches to achieve high-efficiency in multi-channel neural interfacing microsystems. We present system-level architectures for the efficient handling of multiple recording channels. We cover system-level-based strategies for the smart power management of such multi-channel arrangements. We review low-power sensory circuits topologies for extracting and separating multiple biopotential signal modalities. Finally, we present practical implementations of low-power system-level approaches and dedicated sensory circuit topologies achieving high-power efficiency.

This work was supported in part by the Natural Sciences and Engineering Research Council of Canada.

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II. Multi-channel recording system architectures

Dedicated multi-channel system architectures must be employed in order to gather the sampled activity from several channels, digitize it and send it wirelessly to the outside world in an efficient fashion. Fig. 1 is presenting three system-level configurations that are addressing such challenge differently. A straightforward approach consists in sharing a fast digitizer between several sensory channels (Fig. 1a). In such scheme, the sensory channels are directed toward an analog-to-digital converter (ADC) by employing time-division multiplexing (TDM) in the analog domain. The challenge with such an approach consists in minimizing power consumption from the high-speed unity gain buffers, sample-and-hold (SHA) circuit and ADC. Indeed, unity gain buffers presenting wide bandwidth, much higher than the incoming signal bandwidth itself (f_{max}), are needed to drive the SHA circuit or the ADC within the small TDM time intervals, which requirement results in high power consumption. According to [1], the buffers and the SHA circuit must feature a low-pass f_{-3dB} of at least 5 times as wide as f_{max} in order to obtain a tracking error of less than 1/2 LSB with a 10-bit representation. Moreover, analog multiplexers must be designed carefully in order to avoid excessive crosstalk and distortion. Examples of such system-level configurations are presented in [2, 3].

Another approach consists in providing one low-power low-rate ADC for each sensory channel and performing TDM in the digital domain (Fig. 1b). Such an approach has the benefits of avoiding the need for several power-consuming unity gain buffers, and eliminating inter-channel crosstalk. However, great care must be taken in the design of the ADC in order to minimize the chip area. Such type of implementation is presented in [4]. A third approach consists in performing digitization off the chip to save power and chip area (Fig. 1c). Digitization is performed in two phases: A first phase consists of converting the multiplexed analog sensory output into time duration, which operation is known as analog-to-time conversion (ATC). Then, after transmitting the ATC signal outside the body where power and size are not highly constrained, a second phase consists

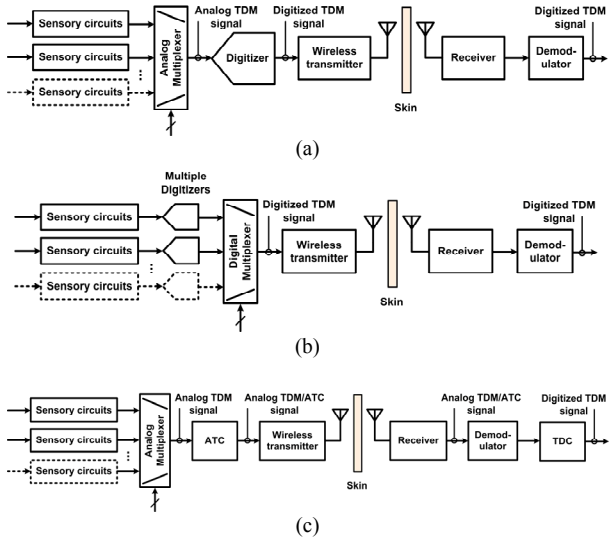

Fig. 1. Three multi-channel recording architectures. (a) Analog TDM is employed to share a fast ADC across channels. (b) Digital TDM is enabled by providing one low-power ADC/channel. (c) Analog TDM and ATC are employed in the implanted part followed by TDC in the external part to transferring digitization on the remote station side.

in performing time-to-digital conversion (TDC). In addition to save power, this approach is not requiring any clock signal. However, TDM must be performed in the analog domain, which prompts for crosstalk. Such an approach is presented in [5].

III. LOW-POWER SYSTEM-LEVEL STRATEGIES

The need for a parallel arrangement comprising several power hungry modules, like low-noise sensory circuits, high-speed data converters and wireless transmitters, command the implementation of dedicated system-level approaches for addressing excessive power consumption in such highly constrained microsystems. Power scheduling consists in powering up the recording circuits only when necessary. Specifically, current-supply modulation [5, 6] and duty cycling [5, 7, 8] are power scheduling techniques consisting in switching specific building blocks between an active and an idle state with low duty cycle. The shorter the duty cycling period, the lower the power dissipation in the circuits. The difference between both techniques is that the former uses low-level bias current in the idle state, whereas the latter has zero current in such state for further increasing power savings. However, a duty cycle period that is too short can potentially degrade in the reading accuracy of a neural recording channel because fast intermittent monitoring requires circuits featuring larger bandwidth, thus letting more noise entering. The battery-powered sensor interface presented in [8] addresses this tradeoff by providing different levels of accuracy and lifetime through the utilization of a programmable low-pass filter. Such filter allows selecting between different input-referred noise levels and duty cycle lengths, which determines the overall accuracy and power consumption. The power-scheduling mechanism employed in [5] consists in putting most of the neural amplifiers that are not being sampled in sleep mode with a fraction of their active current consumption (0.5μA). Indeed, not turning the neural amplifiers completely off lets time for the neural amplifiers to reach their active state faster ahead of each sampling. This scheme allows to decrease power consumption by 18% in the multi-channel front-end block. Besides, the multiplexing of several electrodes towards one low-noise amplifier (LNA) has been demonstrated to save power and silicon area. Time division multiplexing of four channels towards a single neural amplifier is achieved in [9]. Such topology is sharing a single LNA between four independent input electrodes for decreasing the power consumption per channel by one fourth. A frequency-division multiplexing scheme is implemented in [10] where the amplitude of the neural activity seen at several individual electrodes is modulated and directed towards a single wideband neural amplifier. It is shown in [10] that the maximum number of electrodes that can be multiplexed towards one single amplifier is limited by the summation of the thermal noise from each electrode at the input node of the wideband neural amplifier, and it is in the range of 5 to 10 for typical cases.

On the other hand, activity-based schemes are exploiting the transient characteristics of neural signals to maximize efficiency. Adaptive sampling [11] is an activity-based technique that allows to significantly decreasing the data rate by dynamically varying the sampling rate of an ADC, based on the input signal activity. Reduction factors of 7 are reported with this scheme. The algorithm requires the implementation of the 2^{nd} derivative of the signal within dedicated circuits to measure the rate of change of the input. Other activity-based schemes exploit the intermittent nature of neural recordings along with their low duty cycles by powering up the recording building blocks only when neural events occur. Such strategy requires the utilization of accurate biopotential detectors along with power scheduling. In such schemes, most recording building blocks remain in an idle state, draining practically no current until neural events occur. In [12], a low-overhead analog detector is employed to locate neural events and triggering up the recording electronics. Indeed, the approach proposed in [13] is using low-overhead analog delay elements that are implemented within ultralow-power linear-delay filters to waking up the recording circuits "ahead" of biopotential occurrences, which functionality is critical to avoid truncated waveforms.

Adaptive mechanisms have also been proposed for achieving high-power efficiency. In such approaches, the DC operating points of a circuit are optimally adjusted by employing feedback. A neural amplifier using adaptive biasing is demonstrated in [14]. Such closed-loop scheme is directly adjusting the signal-to-noise ratio of an LNA by changing its bias current in order to set the input referred-noise of the amplifier right above the noise floor of the input electrode, for avoiding any waste of energy.

IV. Low-power sensory circuits

The low-noise amplifier is the main building block of an analog front-end. The LNA must amplify and filter the neural waveforms in order to removing any input DC offset seen across a pair of differential electrodes, and maximizing the dynamic range in the recording channel. Indeed, it must provide sufficient gain, appropriate bandwidth, high signal-to-noise ratio (SNR), excellent linearity, high common mode and high power supply rejection ratios (CMRR and PSRR) to provide the expected signal quality. In the case of a multi-channel interface, one such sensory circuit is needed for each electrode. Therefore, the LNA must present low-power and small size, and be scalable to multiple parallel channels. Furthermore, it is essential to optimize the design of the LNA for very low-power through a dedicated circuit design methodology, like in [15]. The noise efficiency factor (NEF) has been widely adopted as a main figure of merit to assess the performance of LNAs and compare the several existing topologies together.

Besides, designing sensory circuits that can capture multi-modal neural information is critical to gather as much neural information as possible. Such amplifiers can discriminate among multiple types of biopotentials by accommodating different frequency ranges [5, 16, 17]. They can provide different bandwidth settings by 1) tuning resistive values in a filter, 2) selecting different capacitors values from an array, or 3) changing the operating points of a circuit. In several designs, the high-pass cutoff is changed by varying the gate voltage of a pseudo-resistor [16, 18], or that of a weakly inverted MOSFET [19]. In contrast, the low-pass cutoff is changed by varying the operating point of the LNA directly [15], or by changing its capacitive load through the selection of different output capacitors [7].

However, tunable circuits can present significant distortion and exhibit excessive process-dependent variations. Indeed, the resistance of the MOS devices is highly dependent on the voltage level of the output signal [18]. Dedicated linearization circuits have been proposed for performing appropriate biasing of the gate of a MOS device and linearize the MOS resistor [1, 18]. Such approaches have been extended further in [8] by replacing any inaccurate current mirrors and source followers by precise closed-loop opamps, which allow reaching high-linearity above 74 dB within ±200 mV, and enabling process-independent frequency cutoff values. This proposed strategy is linearizing a pseudo-resistor by reporting any variations in the input voltage right at the gates of its constituting pMOS devices with unity gain. This is maintaining the gate to source voltage of the MOSFETs at constant value, for cancelling any non-linearity, while providing adequate DC biasing to set the desired cut-off frequency.

A switched-capacitor neural amplifier with tunable characteristics was recently demonstrated in [20] as an alternate mean to conventional continuous-time circuits. In addition to providing low-noise and satisfactory gain, this amplifier can accommodate local field potentials (LFP) and action potentials (AP) through tuning of its clocking frequency, implementing different low- and high-pass cutoff frequencies in a straightforward fashion.

V. Practical Recording Channel Implementations

Effective implementations of the presented system-level approaches (section 3) require the utilization of compatible circuit topologies. This section is presenting sensory circuits topologies dedicated to the implementation of low-power multi-channel arrangements employing system-level-based power management strategies, along with corresponding simulation results. The presented systems have been simulated in a 0.35-µm CMOS 4M/2P process.

The schematic of a low-power neural action potential recording channel employing duty cycling is presented in Fig. 2. In this scheme, a LNA providing a gain of 100 is powered-up only for brief time intervals to reduce power consumption. The output of the LNA is sampled with a low-power low-speed switched-capacitor SHA circuit featuring an embedded low-pass cutoff frequency for limiting the Johnson noise in the channel. Such SHA circuit is efficiently combining sampling action along with low-pass filtering in a compact building block. The low-pass cutoff frequency of the filter is approximately given by $f_{-3dB}=(1/2\pi)\cdot(C_1/C_2)\cdot f_{clk}$. One challenge in the implementation of such duty cycling strategy is designing an LNA which output can rapidly settle within a short time duration in order to provide high signal quality along with low-power. Indeed, wide-bandwidth must be achieved in the LNA to allow fast settling, but this must be done without bringing too much power overhead.

The schematic of a wideband low-power LNA along with its common mode feedback (CMFB) circuit is presented in Fig. 4. This design is naturally featuring wide bandwidth, which makes the overall power consumption of the LNA to be solely bounded by the required input-referred noise level. A trans conductor (made of M1-M2, M5-M6 and R_1) converts v_{in+}-v_{in-} into a current, which is deflected in part in a transimpedance amplifier (made of M3-M4 and R_2), and then translated into an amplified output voltage v_{out+}-v_{out-}. Assuming $\alpha R_2 << R_{out}$, the gain of the LNA can be expressed by the resistor ratio R_2/R_1 [21], where

$$\alpha = (1 + 1/gm_{M1}R_1) \cdot (1 + 1/gm_{M2}R_2), \quad (1)$$

and the low-pass frequency is given by

$$f_{LP} \cong (1/2\pi) \cdot (1/\alpha R_2 C_c). \quad (2)$$

This design is using source degeneration resistors R_{d1}-R_{d2} in the active load M5-M6 to decrease the contributed noise from these MOS devices, like in [16]. Moreover, split resistors R_1-R_2 are used along with a single current source in both diff-pairs to efficiently cancel the 2nd harmonic terms and achieve high linearity. The total current consumption of this optimized design is 1.13 µA, including the CMFB circuit. The input referred noise is 31 nV/√Hz and the

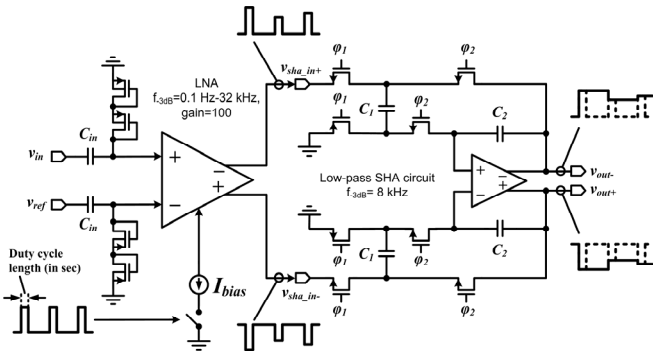

Fig. 2. An analog front-end circuit employing duty cycling. The LNA is allowing fast settling to enable high signal quality. A low-pass switched capacitors SHA circuit is filtering the noise above f_{max}.

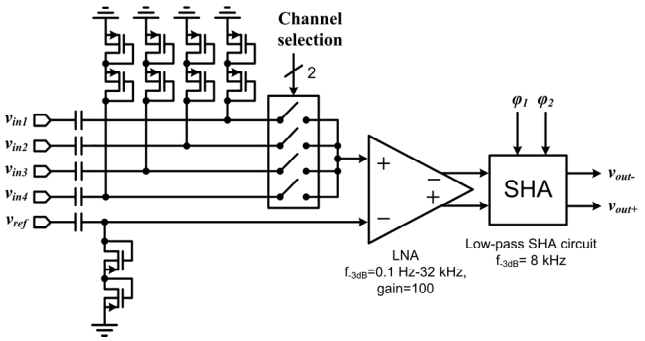

Fig. 3. Schematic of an analog front-end circuit employing time-division multiplexing in the LNA as a mean to increase power efficiency. The same wideband LNA as in Fig. 2 is employed for this system.

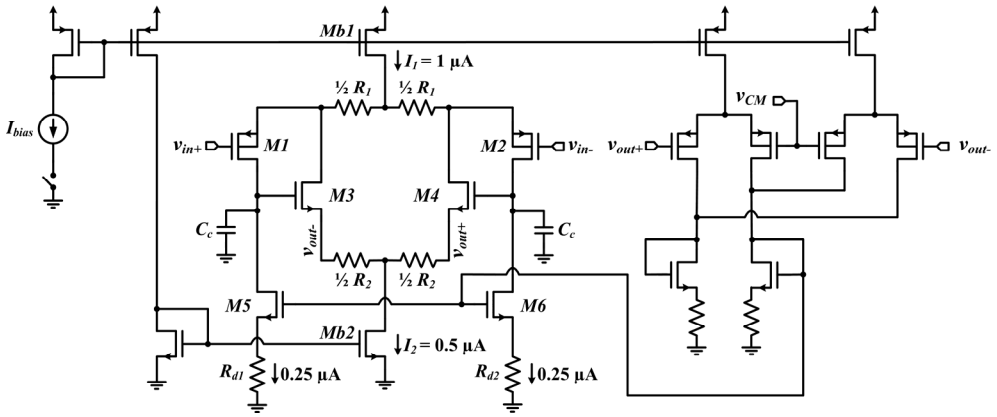

Fig. 4. Schematic of a low-noise amplifier dedicated to utilization in a duty cycling-based implementation. This design is naturally featuring wide bandwidth, which makes the overall power consumption of the LNA to be solely bounded by the required input-referred noise level.

bandwidth is 32 kHz, which gives a NEF of 1.3. Such very low NEF results from the utilization of source degeneration resistors, which are significantly lowering the overall input referred noise. The SHA circuit is consuming 0.25 µA. Using a duty cycle of 25% reduces the power consumption of the LNA by a factor of 4. Table I is summarizing the performance of the LNA. The same wideband LNA can be incorporated in a TDM strategy as depicted in Fig. 3. Similarly to a duty cycling arrangement, the multiplexing of several electrodes towards a common LNA (section 3) requires wideband in order for the output of such an amplifier to rapidly settling within short interleaving time-intervals. In such configuration, the LNA must roughly providing four times the signal bandwidth $f_{max} \approx 8$ kHz in order to process four TDM electrodes. Moreover, the same SHA circuit is handling 4 channels, which is reducing the power consumption of the entire channel by a factor of 4.

Besides, in addition to duty-cycling circuits, optimized low-power continuous-time implementations are also of great interest. Fig. 5 is presenting a low-power continuous-time multimodal amplifier enabling the simultaneous extraction of LFPs and APs. A high-frequency (HF) readout (100 Hz – 10 kHz) is measured at V_{1+}-V_{1-} with a gain of 100, while a low-frequency (LF) readout is measured at V_{2+}-V_{2-} with a gain of 10. AC coupling networks are implementing a high-pass cutoff frequency that is within mHz for removing

TABLE I
SIMULATED PERFORMANCE SUMMARY OF THE LNA

Process technology (Std. CMOS)	TSMC 0.35-µm
Voltage supply (V)	1.8
Current consumption (w/o duty cycling) (µA)	1.13
Current consumption (25% duty cycling) (µA)	0.28
Gain (V/V)	100
Input-referred noise density (nV/√Hz)	31
HD3 (1-mV 1-kHz input sinewave) (dBc)	-70.2
Low-pass cutoff frequency (kHz)	32
High-pass cutoff frequency (Hz)	$\approx 1 \times 10^{-3}$
NEF (with degeneration resistors R_{d1}-R_{d2})	1.3

any input DC offset and preventing the amplifiers from saturation. Fig. 6 is presenting the superimposed frequency responses measured at both readouts. The transfer function of the HF readout is given by

$$\frac{V_{1+}-V_{1-}}{V_{in}-V_{ref}} = \frac{C_1}{C_2} \cdot \frac{j\omega R_{e-h} C_3 \frac{C_2}{C_4}}{j\omega R_{e-h} C_3 \frac{C_2}{C_4}+1} \cdot \frac{j\omega R_{a-d} C_1}{j\omega R_{a-d} C_1+1}, \quad (3)$$

and the transfer function of the LF readout is given by

$$\frac{V_{2+}-V_{2-}}{V_{in}-V_{ref}} = \frac{-1}{j\omega R_{e-h} C_3} \cdot \frac{V_{1+}-V_{1-}}{V_{in}-V_{ref}}, \quad (4)$$

where R_{a-d} and R_{e-h} are the resistances of the corresponding

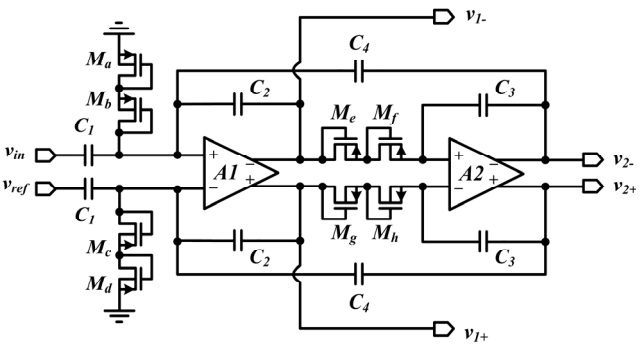

Fig. 5. Schematic of a low-noise multimodal amplifier which is simultaneously extracting low-frequency and high-frequency biopotential modalities. The high-frequency readout is measured at v_{1+} - v_{1-}, and the low-frequency readout is measured at v_{2+} - v_{2-}.

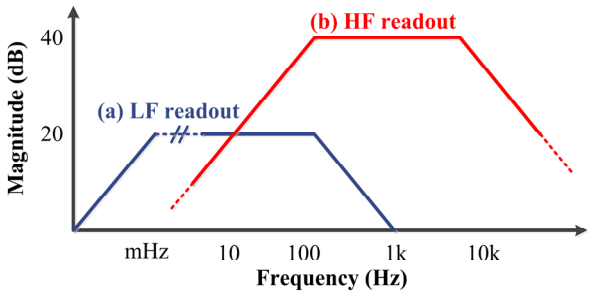

Fig. 6. Frequency responses (a) measured at the low-frequency readout, and (b) at the high-frequency readout.

pseudo-resistors. In addition to operating within a small power budget, such continuous-time circuit presents several advantages over separate mono-mode readout circuits: 1) Sharing the same AC coupling networks (M_a-M_d and capacitors C_1) in both readouts allows practically cutting silicon area by half, since integrated capacitors C_1 must usually be on the order of tens of pico-farad to enable low input noise [15, 16]. 2) Using a pseudo-resistor that is not in the feedback path of a closed-loop opamp, like in [15, 16], prompts for high linearity. 3) Continuous-time operation is relaxing requirements on settling time and gain-bandwidth product in opamps compared to other types of implementations, like switched-capacitors, for instance. 4) The gain of both readouts depends on independent ratios of integrated capacitors (poly or metal-to-metal), which are very linear. The simulated amplifier is featuring a current consumption of 1.3 µA, and a strongest harmonic below -70 dBc for a 1-mV 1-kHz input sine wave.

VI. Conclusion

We have reviewed energy-efficient system-level architectures, smart power management strategies and low-power sensory circuit topologies that are improving efficiency in power constrained multi-channel recording arrangements. Moreover, duty cycling and TDM-based strategies along with the design of a compatible LNA were presented and explained. Finally, the design of a continuous-time multimodal amplifier has been presented.

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