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Low-Power SoC Design for Ligament Balance Measuring System in Total Knee Arthroplasty

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***Abstract* — A design of a low-power wireless System-on-Chip (SoC) for the Ligament Balance Measuring System (LBMS) in Total Knee Arthroplasty (TKA) is presented in this paper. It includes a signal conditioning circuit that can support up to 15 force sensors, a 433MHz RF front-end for data transmission, an 8-bit low-power microprocessor, and a FIFO with a digital filter. Idle and wake-up modes are well designed to reduce the power consumption since the device should be used for the whole surgical procedure. Test results show that the signal conditioning circuit with 16-bit single line output can operate under a wide voltage range, which is from 1.2V to 3.6V. The minimal power consumption is 139μW@1.2V with a 200KHz clock. Experimental results demonstrated in static and body tests are given in the paper also. The chip will be used in an aided monitoring system for Total Knee Arthroplasty in the future work.**

I. Introduction

In Total Knee Arthroplasty (TKA) for the patient with femoral head necrosis is to replace its the damaged knee joint by an artificial knee implant. The artificial knee implant may fail because of attrition, loosening or misalignment, etc. As a result, the mostly choice for patients is the recover surgery which will bring more pain. Therefore, it is more critical to ensure the first-operation success to minimize the probabilities of revision surgery.

Many efforts have been made to design implantable systems for monitoring the biomedical implants[1][2][3][4]. In [4], in-vivo strain gauges have been used in distal femoral replacements and in hip implants. However, most of these experiments focus on logging data during short duration, and the power is typically derived through inductive or ultrasonic coupling or through external leads in skin. In [5], temporary implants containing four load cells were used to harvest power and to measure knee joint forces. A method for long-term, battery-less fatigue monitoring by integrating piezoelectric transduction with hot-electron injection on a floating-gate transistor array was presented in [6].

In this paper, a low-power wireless SoC design for Ligament Balance Measuring System (LBMS) in TKA is presented. The goal of the LBMS is to monitor the force balance between two parts of the replacement device implanted in the femur and tibia to improve the quality of surgery. The SoC includes a conditioning circuit that can support up to15 force sensors，a 433MHz RF front-end for data transmission ， an ultra-low-power microprocessor, and a FIFO with a digital filter.

The rest of the paper is organized as follows. Section II presents the LBMS design. SoC implementation is introduced in section III. Section IV shows the experiment results, including static and in-vivo experiments. Future work and conclusion is described in section V.

II. Design of LBMS

There are two basic requirements by TKA. One is to better recover the motor properties of the knee joint and another one is to reduce the stress and attrition between the contact surfaces of joint prosthesis. As shown in Fig.1, the tibia insert is between femoral component and tibia component. Normally there are two force focal areas A and B on the contact surface of the tibia insert. The unbalance of them will lead to the knee joint that doesn't function properly and acceleration of attrition. Therefore, the force balance of the two areas is important for surgery in TKA. To provide more accurate force information for aiding surgery, LBMS is designed to measure the contact force and displays them on the screen.

The LBMS includes two parts. The first part is the device as shown in Fig.1 which contains force sensors and the SoC. The device is powered by batteries. Figure.1 shows the device is inserted between femoral and tibia component.

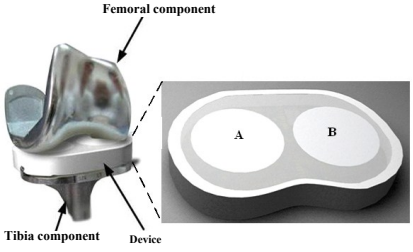

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Fig.1 The sketch map of the joints prothesis and force focal areas

The another part of LBMS is comprised of the receiver which is designed as a USB device that can be easily connected to the PC or medical PAD, and the terminal that displays the force curves of A&B in real time.

The device contains eight to ten sensors that are divided into a couple of parts equally. Each part can detect the pressure of area A or B. The linear force range of the sensor is 0~1.5Kg and the maximal overburden force is 4.5Kg. Consequently, the total linear measure range of the device for each area is 0~7.5Kg.

The SoC is composed of a sensor-interface, an 8-bit MCU and a 433MHz RF transceiver for implanted medical device. The SoC senses the outputs of force sensors and sends measured results to the transceiver wirelessly.

The transceiver is designed with the form of a USB device and can be connected to a notebook or others. The computer with the transceiver is the base station of the system. The base station controls the device by sending commands wirelessly, processes the data from implanted device and displays the dynamical curves on screen.

III. SOC IMPLEMENTATION

A. System Design of the SoC

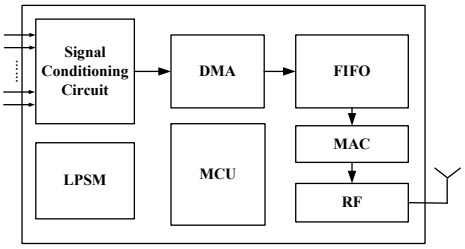


Fig.2 Architecture of the SoC

The architecture of the SoC is illustrated in Fig.2. A 16-bit signal conditioning circuit that can support 8 differential inputs has been designed as the resistive transducer interface, which converts the differential inputs into digital signals. The SoC provides additional three control signals to support up to 15 differential inputs. This function is very useful for multi-sensor systems. The core of the chip is a high efficiency 8-bit microprocessor that can execute one instruction per cycle.

The DMA (Direct Memory Access) is implemented to accelerate the data stream and lower the power consumption. The transceiver module contains three modules. The first one is a low-power 433MHz RF front-end that consumes 1.5nJ/bit during the transmitting. The second one is the MAC (Media Access Control) that packs data and sends the modulated data to the front-end. The final one is a data FIFO (First In First Out) that stores the converted data and provides optional data filtering methods. A LPSM (Low-Power Strategy Management) module handles the low-power methods, for example the sleep/wake-up mode.

The embedded MCU provides the systemic flexibility. The main data processing is carried by base station for lowering the power consumption and the complexity of SoC. Therefore, the SoC is designed as a low-power, lost-cost sensor node for medical purpose.

B. Resistive Transducer Interface Implementation

The signal conditioning circuit is designed for the resistive bridge sensors with a single-line digital output. Figure.3 is the block diagram of the complete system. It consists of a gain-programmable front-end and a voltage-pulse interval convertor, which offers low power, high resolution, high linearity, high power and offset rejection. The supply voltage is from 1.2 to 3.6V for single battery applications.

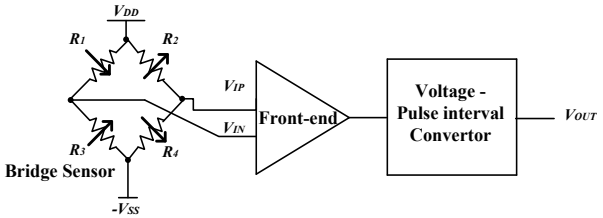


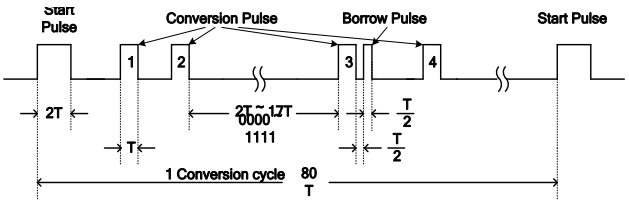
Fig.3 The block diagram of the signal conditioning circuit

The bridge R_1-R_4 operates under the same-level voltage supply of conditioning circuit. The bridge unbalance voltage is sampled and amplified by the front-end. The voltage-pulse interval convertor produces a series of pulses dependent on the input voltage. The single-line output structure of one complete measurement-cycle is shown in Fig.4(a) and measured outputs are shown in Fig.4(b). There are three kinds of pulses in one cycle, start-pulse, conversion-pulses and borrow-pulses. The interval time between two conversion-pulses (or the start-pulse and the first conversion-pulse) is from 2 to 17 clock periods, which represents a 4-bit digital signal. Every cycle has 4 conversion-pulses. Therefore, a 16-bit digital output code can be carried by the intervals in one complete measurement-cycle. Borrow-pulse is used for auto-calibration. When a borrow-pulse occurs in any conversion interval, the previous interval should be corrected with minus 1 clock period.

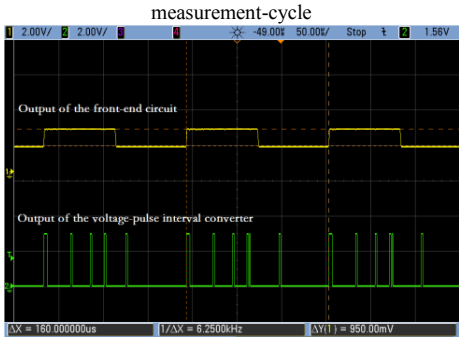
The front-end circuit with a programmable gain (2/9, 8/9, 32/9 and 128/9) is designed for the sample-and-hold and amplification. The maximum bridge imbalance can be set from 15.625mV/V to 1V/V. A differential-inputs structure is introduced for optimizing the common-mode and power-supply rejection. For offset cancellation, a chopper switch-capacitor (SC) network is used.

Many conditioning circuits for low-frequency sensor interface with single-line digital output are based on a relaxation oscillator and provide a frequency/period-modulated output [7]. To obtain an n-bit resolution, the analog input would be integrated or de-integrated to the reference level for 2^n clock periods (the maximum conversion cycles). As a result, the tradeoff between conversion time and resolution is inherent in this kind of implementation.

Considering the limit of oscillator-based conditioning circuits, this paper introduces a novel 16-bit voltage-pulse interval convertor in Fig.5. It consists of a 4-bit ramp-down converter and a residue amplifier with gain of 2^4. During the start-pulse of one measurement cycle, V_{IN} is sampled by C_s. Then we discharge C_{INT}, V_{INT} ramps down. A conversion-pulse, which represents first 4-bit digital code, will be generated when the trip of V_{INT} beyond *GND*. Then we amplify the residue by 2^4 and discharge C_{INT} again in the second interval, and then repeat this procedure until the fourth interval is completed. If the residues are correctly amplified (i.e., charge injection and other errors are small), this method can be quite powerful in increasing the resolution and reducing the conversion time.



(a) Output signal of the conditioning circuit for one complete measurement-cycle



(b) Measured output of the conditioning circuit

Fig.4 Output signal of the conditioning circuit and measured results

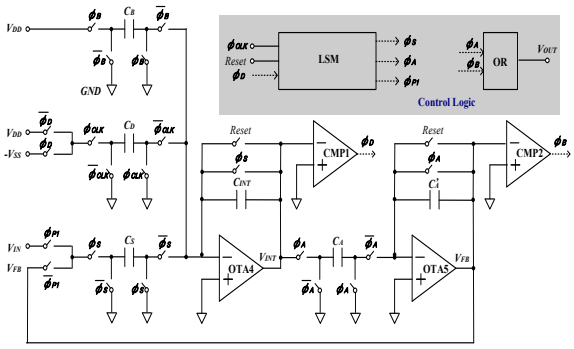


Fig.5 The detailed schematic of voltage-pulse interval convertor

Due to the risk of comparator CMP1's wrong toggle, the output of residue amplifier V_{FB} might be lower than *GND*, which is not allowed for further conversion. Therefore, another comparator CMP2 is used to monitor the residue amplifier's output V_{FB}. If V_{FB} is lower than *GND*, a charge will be injected into C_{INT} for calibration, and a borrow-pulse will be generated.

The circuit has been fabricated in 0.18μm CMOS process with active area of 775μm*550μm. From test results, the signal conditioning circuit with 16-bit single line output can operate from 1.2V to 3.6V that is suitable for battery application. The update rate is no less than 0.16ms with a 500Hz clock. The minimal power consumption is about 139μW@ 1.2V with a 200KHz.

C. *Low Power Strategies in SoC*

There are three low-power strategies used in SoC design.

Firstly, the DMA transfers the converted data to FIFO directly. When a conversion-cycle is finished, an interrupt signal is generated, and the DMA executes the data storage instead of the MCU. Secondly, the wake-up and sleep mode is a common method for low-power application. If the base-station finds the data doesn't change for a specific term, it will send a sleep command to the device. Then the device comes into sleep. The device will sleep for a programmable term and afterwards wake up for a short period to receive the wake-up command from base-station. Finally, the digital filter is a common data processing method for the sensor system to suppress the random noise and smooth the curve.

A straightforward FIFO with filtering mechanism is implemented. The data can be saved into the FIFO and then sent to the MAC. Besides, The FIFO supports two optional methods of data process. The first method is to calculate the arithmetic mean value of the data. The input data will be added to the data saved and then the result replaces the old one. After N times, the sum is intercepted by log_2N and sent out.

Another method of data process is to calculate the weighted mean that listed in (1).

$$D_w = \sum_{n=1}^{N} \frac{D_n}{2^{N-n+1}} \quad (1)$$

where D_w is the weight mean and N is times.

There are two advantages of the FIFO integrated with data filter. The data processing is accelerated by hardware. The averaging method will reduce the data amount to be sent out wirelessly. As a result, the power consumption will be reduced.

IV. Experiments

A. Static Test

A device is designed to verify the function of the proposed system. The whole device contains sensors, two multi-channel ADCs and one 8-bit MCU. Equiponderant weights were used to exert force on the areas of A and B of the tibia insert. The measurement results were plotted in Fig.6. The X-axis represents actual weight and Y-axis represents the outputs of the device. The linearity of the force versus weight is quite good and the slopes of curves A&B are almost equal.

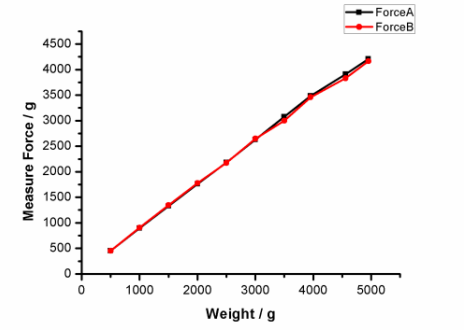


Fig.6 Static force measuring results of area A&B

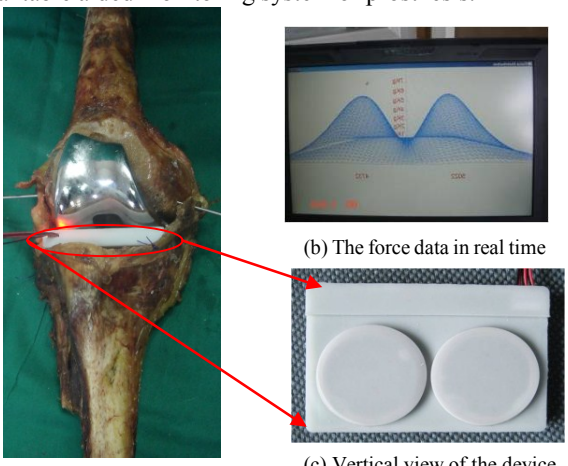
B. In-vivo Experiments

In-vivo experiments were also carried out to find whether the device can meet the requirements which are shown in Fig.7. A real human joint from body is used in the experiment. The test results show that the normal unilateral pressure is between about 3~5kg that is under the device linear measurement range (7.5kg). The proposed system can work properly and display the force data in real time.

V. Future Work And Conclusions

A battery-less implantable aided monitoring system is necessary for checking the situation of the human joint after surgical operation [8]. The SoC design in this work is a good start for the implantable aided monitoring system in the future.

A low-power wireless SoC design for LBMS in TKA is presented in this paper. Several low-power methods were adopted. The results from static test and in-vivo experiments verified the system design. The chip of the signal conditioning circuit test results show that the signal conditioning circuit can operate under the supply from 1.2V to 3.6V and the minimal power consumption is about 139μW@1.2V with a 200KHz clock. The SoC is a good start for future work such as implantable aided monitoring system of prosthesis.



(a) Test with real joint

(b) The force data in real time

(c) Vertical view of the device

Fig. 7 Experimental environment

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