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A Prototype 64-Electrode Stimulator in 65 nm CMOS Process towards a High Density Epi-retinal Prosthesis

N. Tran, E. Skafidas, J. Yang, S. Bai, M. Fu, D. Ng, M. Halpern, and I. Mareels

Abstract—**This paper presents a highly flexible 64-electrode stimulator using 65 nm CMOS process fabricated as a stage towards a 1024-electrode epi-retinal prosthesis, which aims to restore partial vision in patients suffering from eye diseases such as retinitis pigmentosa (RP) and age-related macular degradation (AMD). The stimulator drives 64 electrodes with many flexible features, which are necessary before making a complete 1024-electrode implant chip. Each electrode driver can provide a bi-phasic stimulus current with fully programmable parameters such as amplitude, pulse duration, inter-phase gap, and stimulation rate. The electrode driver operates in an alternately pull-push manner with only one current source working at a time, which helps reduce headroom voltage while controlling charge balance at the active electrode. The stimulator varies both stimulus current amplitude and stimulation rate to represent phosphene brightness. The stimulus current amplitude starts from the tissue depolarization threshold with 64 different levels. The selection of active and return electrodes is arbitrary, any electrodes and any number of them can be selected at any time. The power consumption of the stimulator is 400 µW excluding the stimulus power. Measurement results verify correct operation. The stimulator is easily scaled up to drive 1024 electrodes.**

I. Introduction

Eye diseases such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD) cause vision loss due to the degeneration of photoreceptors. Photoreceptors are the key components in the retina that convert incoming light into neural signals which are then sent to the brain where the scene or image is interpreted. The photoreceptors in a degenerative retina are impaired, which results in no light perception. Bypassing those photoreceptors and electrically stimulating the healthy layers of the retina has been able to restore partial vision in patients [1, 2].

In epi-retinal prosthesis, the ganglion cells are the targeted cells to be stimulated. An epi-retinal prosthesis system includes an external device and an implant device. The external device consists of a camera to capture the scene and a processor to process the captured scene and then send it wirelessly to the implant device. The implant device placed on the retina surface receives the image information from the external device and converts it into corresponding stimulus currents to stimulate the ganglion cells via an array of electrodes. Power for the implant device is transferred from the external device via an inductive link. Fig. 1 shows the architecture of the implant device. The implant device consists of a power recovery circuit with its coil for power reception, a transceiver with its coil and an analog front-end for data communication, a stimulator for processing image data and stimulating the electrode array, diagnostic circuitry for monitoring the implant device's conditions (such as temperature and electrode-tissue contact), and an electrode array for interfacing the stimulator to the targeted tissue cells. The whole implant device except the electrode array and the coils is integrated in one single silicon chip (implant chip).

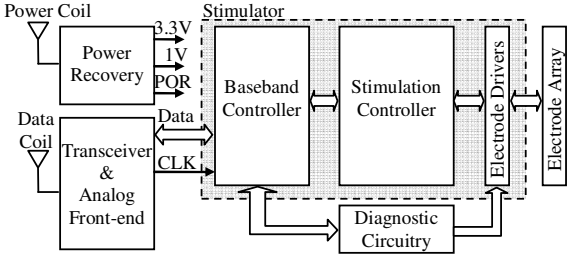

Fig. 1. Architecture of the implant device with the stimulator in this work

An approximation of 600 to 1000 electrodes are suggested to be the number of electrodes required for perceiving basic vision such as reading large-sized text, navigating a room unaided, and recognizing faces [3]. Building an implant chip to drive 1000 electrodes is challenging and requires complicated control circuitry with potentially high power consumption, high data rate for real-time image updating, and compact size for fitting on the limited retina surface. Power consumption challenge is even more critical when the power is transferred wirelessly.

There is a charge threshold from which light perception starts to be achieved. Low threshold is desired as it requires low stimulus current, and hence probably low stimulus voltage. Three-dimensional electrodes ensuring close contact to the ganglion cells have lead to low threshold [2]. This threshold can be made lower if penetrating electrodes are used, as penetrating electrodes ensure much closer contact to the targeted ganglion cells. Therefore, small scale CMOS process is ideal for implementing this implant chip to realize high level of circuit integration as well as low power consumption.

The ultimate goal of the Bionic Vision Australia project is to build a 1024-electrode implant chip using 65 nm CMOS process for low power consumption and high integration. However, building a 1024-electrode implant chip has many

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N. Tran, E. Skafidas, J. Yang, S. Bai, M. Fu, D. Ng, and M. Halpern are with Australia's ICT Research Centre of Excellence (NICTA), Victoria Research Laboratory, Parkville, VIC 3010, Australia. N. Tran, E. Skafidas, J. Yang, S. Bai, M. Fu, and I. Mareels are with the Department of Electrical and Electronic Engineering, The University of Melbourne, Parkville, VIC 3010, Australia.

challenges. To test the feasibility of 65 nm CMOS process retinal stimulator, we developed new stimulation architectures and implemented a 64-electrode stimulator using IBM 65 nm CMOS process.

This paper presents the design of this stimulator. The stimulator consists of three main building blocks: baseband controller, stimulation controller and electrode driver. The following sections present the stimulation strategies, system features, the detailed designs of these building blocks, and some measurement results on the stimulator's functionality and power consumption.

II. Stimulation Strategies and System Features

A. Stimulation Strategies

Fig. 2 shows an illustration of updating and refreshing image frames. The updating rate of video images is about 24 frames per second to provide continuous motion, whereas the refreshing rate is around 60 Hz to achieve flicker-free vision. Therefore, separation of updating and refreshing rate with the help of a data buffer can reduce the required data bandwidth by a half, as compared to the scheme in [4] where updating rate and refreshing rate were the same.

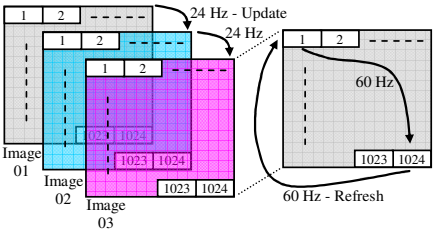


Fig. 2. Image updating and refreshing

Electrical stimulation is to inject a certain amount of charge into targeted tissue cells within certain time duration via electrodes. Fig. 3 a) illustrates an example of electrical stimulation, in which one electrode acts as an active electrode, and the other acts as a return electrode. Different phosphene brightness levels can be achieved by varying the stimulus current amplitude [5] or by varying the rate of stimulation [6]. In Fig. 3 b), the stimulus current amplitude is varied to represent the brightness while other parameters such as current pulse width, inter-phase delay and stimulus rate (refreshing rate) are fixed. In Fig. 3 c), all parameters of the stimulus current are fixed with smaller stimulus pulse duration (240 Hz), and the brightness is given by the number of stimulus pulses (rate of stimulation) in one refreshing period.

In the presented stimulator, each electrode is driven by one driver, which is able to connect the electrode to either a current sink or a current source or power supply or ground. This topology allows each electrode in the array to act as either active or return. An active electrode is first connected to a current sink, and then connected to a current source to generate bi-phasic stimulus current, while its return electrode(s) is (are) connected to power supply, and then ground, respectively. This alternately pull-push manner makes the stimulus current at the active electrode fully controllable and also consumes less headroom voltage, because only one current sink or source is used at a time. In addition, the ability to switch return electrodes between power supply and ground makes it possible to use only a single supply rail, which is preferable in CMOS circuit design. A similar driver has been proposed in [7] where it was followed by a demultiplexer. This design not only consumes more headroom voltage but also reduces the flexibility in choosing active electrodes. Fig. 3 d) describes the electrode driver topology to provide bi-phasic stimulus current.

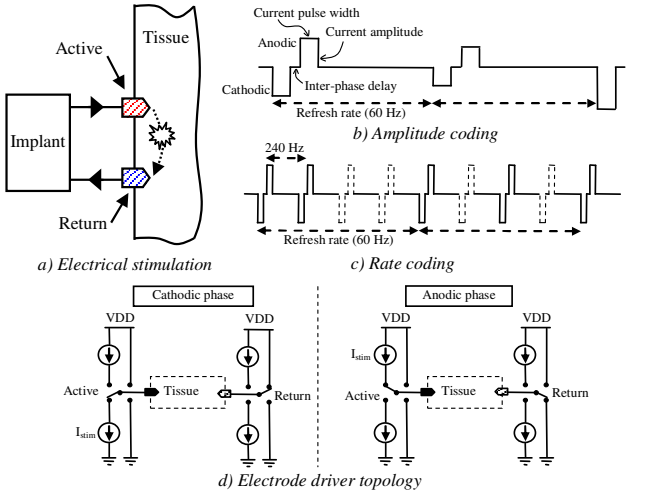


Fig. 3. a) Illustration of electrical stimulation, b) Representing phosphene brightness using current amplitude, c) Representing phosphene brightness using rate of stimulation, d) Electrode driver topology

B. System Features

The stimulator described in this paper was designed to be as flexible as possible. There are many flexible features, among them are: 1) the stimulator provides stimulus currents with wide-range multiple-step amplitude, pulse duration, and frequency; 2) the stimulus current has 64 different levels starting from the depolarization threshold; 3) in the 64-electrode array, any electrode and any number of them can be selected as active or return at any time; 4) the stimulator supports both amplitude and stimulation rate varying to represent phosphene brightness; and 5) the stimulator supports both bi-polar stimulation where return electrodes are from the 64-electrode array and mono-polar stimulation where a remote common electrode acts as return electrode.

III. Stimulator Design

A. Downlink Baseband Controller

The downlink baseband controller receives and processes data from the receiver. Fig. 4 shows the conceptual block diagram of the downlink baseband controller. Each data frame starts with a pre-defined frame synchronization pattern, then main data, and finishes with a corresponding cyclic redundancy check (CRC) code. The data stream first comes to a bit synchronization circuit to align with the clock signal. The aligned data stream is then fed into a frame synchronization circuit. Once the synchronization pattern is detected, the next incoming bits are fed into both the data buffer and the CRC check for CRC calculation. The control logic checks the CRC output after a full data frame has been loaded in, and corresponding signals are generated based on the CRC output and data type. The frame synchronization circuit is disabled after the frame synchronization pattern has been detected, and is kept disabled until the CRC check has

been finished, this ensures no frame detection occurs during the data buffering and CRC checking.

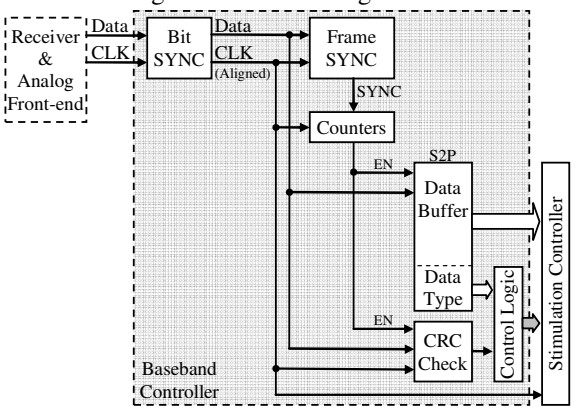


Fig. 4. Conceptual block diagram of the downlink baseband controller

B. Stimulation Controller

The stimulation controller shown in Fig. 5 is the central block in the stimulator and controls the stimulator's operation. There are two operation modes: configuration and stimulation. In the configuration mode, all pre-defined parameters are set such as brightness coding mode (amplitude or rate), leading pulse (cathodic or anodic), pulse duration and inter-phase delay gap, electrode shorting duration, current increment step, threshold current, stimulation mode (bi-polar or mono-polar), sequence of active electrodes, and sequence of return electrodes. To do so, the first data frame goes to the central controller and the pulse generator to define the stimulus pulse profile and set up operation mode. The following data frames in turn go to the active sequencer, the return sequencer (if bi-polar stimulation is chosen), the current bias data registers, and the threshold current data registers. The sequencers allow any electrodes to act as active or return electrodes at any time slices. Once the configuration has been finished, the stimulator switches to the stimulation mode where real-time image data are received and converted into stimulus currents.

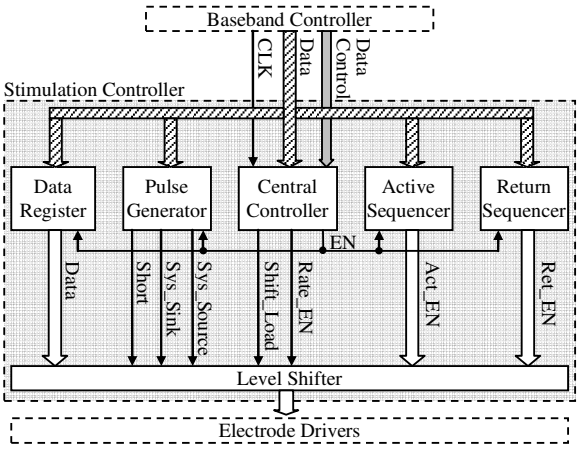
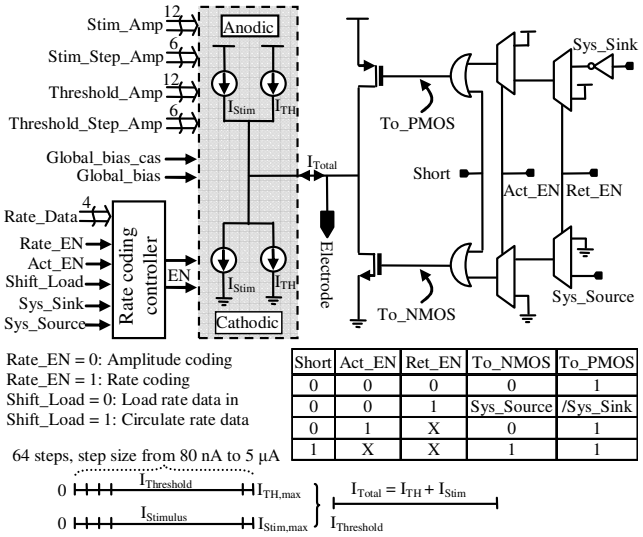


Fig. 5. Conceptual block diagram of stimulation controller

C. Electrode Driver

The electrode driver shown in Fig. 6 can act as an active or return electrode or shorted to ground to discharge all accumulated charge on the electrode it drives. The driver supports both amplitude and rate coding to represent brightness.



Short	Act_EN	Ret_EN	To_NMOS	To_PMOS
0	0	0	0	1
0	0	1	Sys_Source	/Sys_Sink
0	1	X	0	1
1	X	X	1	1

Fig. 6. Conceptual schematic of the electrode driver

The current delivered to the electrode is the sum of the stimulation current and the threshold current. As different regions on retinal surface may require different depolarization thresholds, each electrode driver has the ability of providing its own threshold current, which varies from other drivers. Once the threshold at a specific electrode is known, the stimulus current delivered to that electrode is determined by the stimulation current sink and source with 64 different levels. Therefore, each electrode is independently driven with 64 levels of current starting from the threshold. This combination utilizes all 6-bit data provided to the stimulation current generator. Without the addition of the threshold, some of the 6-bit data representing values less than the threshold are useless and the stimulus current no longer has 64-level resolution.

IV. Results

A. Stimulator Area and Power Consumption

Small size of the implant chip is one of the critical requirements due to the limited area of the retina. A 6x5 mm^2 silicon chip is planed to be used, in which 5x5 mm^2 is allocated to house the 1024 electrode drivers. The other area of 1x5 mm^2 is reserved for other blocks in the implant chip. Flip chip technique is going to be used to connect the outputs of the drivers to the electrode array. The electrode drivers are arranged in an array of 32x32 with pitches of 150 µm between adjacent drivers, resulting in an area of 150x150 μm^2 per each driver. Fig. 7 shows the micrograph of the fabricated prototype chip including the presented 64-driver stimulator. There are two pads at each driver's output, one in the 8x8 array for flip-chip purpose, the other on the chip edge for wire-bonding purpose. The stimulator was fabricated in 65 nm CMOS process with power supply of 1V for low power consumption except the electrode drivers, where thick-oxide transistors are used with 3.3V supply to provide high stimulus current.

Table 1 summarizes some of the stimulator's specifications. The prototype array pitch is 200 µm, but the targeted pitch of 150 µm for the high density stimulator can

easily be achieved with careful layout. The controlling power consumption is 400 µW. The total power consumption of the stimulator is dependent on the stimulation activity. With stimulation time of 1 ms, the refreshing cycle of 16.6 ms (60 Hz) can be divided into 16 time slices in each of which only 4 electrodes need stimulated simultaneously, which reduces significantly the instantaneous power consumption.

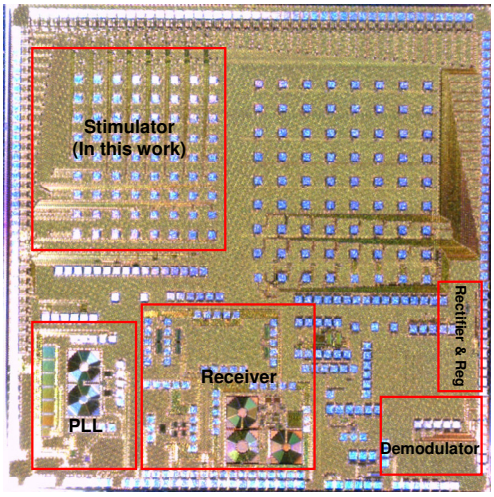


Fig. 7. Micrograph of the chip including the presented stimulator. Chip size is 5x5 mm^2

TABLE I. **STIMULATOR SPECIFICATIONS**

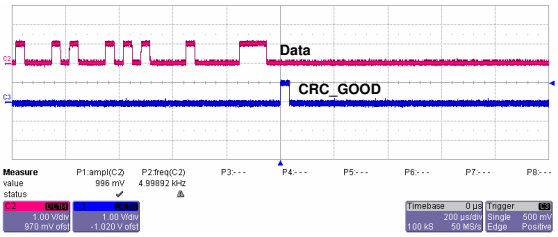
Technology	65 nm CMOS
Stimulator's size	1700 x 1960 µm^2
Single electrode driver's size (with pad)	200 x 200 µm^2
Supply voltage Core controller Output driver	 1 V 3.3 V
Power consumption Central controller Driver array (without stimulation)	 200 µW 200 µW
Current source/sink compliance voltage	3 V
Number of electrode drivers	64

B. Measurement Results

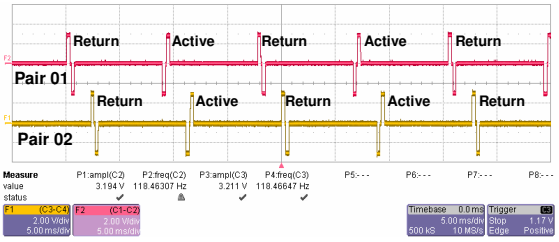
The fabricated stimulator was first tested using a probe station to quickly verify its functionality. Fig. 8 shows the measurement setup, in which digital serial data and clock are transferred to the stimulator from a PC via a data acquisition device (NI-DAQ USB 6363). The data processing and clock generation are implemented using LabVIEW.

Fig. 8. Measurement setup

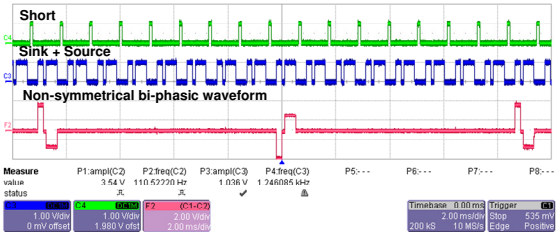
Measurement results in Fig. 9 show that the stimulator operated properly as designed. In Fig. 9 a), good CRC checking was achieved, which means correct data have been received. Fig. 9 b) shows two pairs of electrodes being active and return at different time slices. In each pair, an electrode was active while the other was return and vice versa. Fig. 9 c) shows that non-symmetrical current waveform was able to be generated, which allows more stimulation strategies to be realized.



a) CRC checker output



b) Two pairs of electrodes working at different time slices



c) Generated non-symmetrical waveform

Fig. 9. Some measurement results of the stimulator

V. CONCLUSIONS

A novel and flexible stimulator suitable for a high acuity retinal prosthesis is presented. The stimulator controls an array of 64 electrodes with a lot of flexible features. This stimulator is an essential design stage in building a completely integrated 1024-electrode retinal prosthesis. Measurement results show that the stimulator has flexibility in being able to support various stimulation strategies.

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