33rd Annual International Conference of the IEEE EMBS
Boston, Massachusetts USA, August 30 - September 3, 2011

Towards a Chip Scale Neurostimulator: System Architecture of a Current-Driven 98 Channel Neurostimulator via a Two-Wire Interface

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***Abstract*— With more clinical trials proving viability of visual prosthesis follows the demand for higher resolution devices. As the number of electrodes increases, due to surgical difficulties, it is preferred to keep their length short by placing the implant close to the stimulation site, where there are considerable constraints on device size. On the contrary, the physical volume of the implant generally increases with increasing number of electrodes. Splitting the implant into two modules and placing only the essential circuits near the site of stimulation solves the aforementioned problem. However now the problem is redirected to the robustness and the safety of the interface joining these modules. A novel two-wire interface driving a 98 channel neurostimulator incorporating the split-architecture is presented. The stimulator is provided with both power and data by sending square current waveforms via the two-wire interface. The stimulator itself is fabricated using 0.35 μm HVCMOS technology and occupies 4.9 x 4.9 mm^2 and requires no external decoupling capacitor.**

I. Introduction

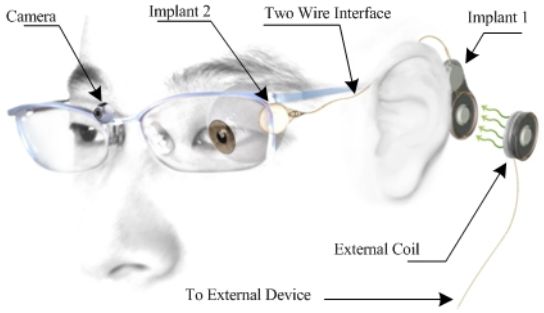

Fig. 1. System overview of the prototype suprachoroidal implant based on the proposed split architecture. Unit 2 is placed near the site of stimulation and Unit 1 as well as the inductive coils are placed behind the ear. A two wire interface joins the two modules.

Recent clinical trial results [1] are reinforcing the credibility of visual prosthesis to provide rudimentary vision to those suffering from retinal neurodegenerative diseases. As more results prove the practicability of such implants, there is an increase in demand for devices with higher number of stimulation channels in an attempt to enhance the functional vision that can be restored by such devices. There are various complications that arise with increasing the number of stimulating channels, one of which is high power dissipation. The maximum number of stimulating channels that can be active at any one time is generally limited by the power, from the inductive link, and the heat dissipation requirements of the stimulator. It is inevitable for future generation devices that the stimulating sources need to be multiplexed between the electrodes possibly with sophisticated encoding schemes [2]. This allows the potential of having high resolution devices with a lesser number of stimulating sources. Even so, every effort should be spent on minimizing the power dissipation of the implant to maximize the number of stimulating electrodes. Another major complication with high resolution devices is that as the number of electrodes increase, it is preferred to place the stimulator as close to the stimulation site. This is mainly due to the surgical difficulties in handling a wide bundle of electrodes that need to be located near the target neural tissue. With increasing number of electrodes this electrode bundle and its interface to a hermetically encapsulated neurostimulator increases in size. Naturally this imposes significant difficulties when implanting such a device in the eye.

In order to resolve both the volume and the power requirement issues, our group is focusing on developing a visual prosthesis based on a split architecture as shown in Fig. 1. The implant itself is split into two modules, one located behind the ear where there is a relatively larger space for a larger device concurrently affording higher heat dissipation capabilities due to increased surface area, with the other placed near the eye with short electrodes designed to sit in the suprachoroidal space. A system architectural overview of a 98-channel neurostimlator designed to be used as an ocular unit in our proposed system and the preliminary measurement results are presented in the following sections.

II. Two-wire interface

An overview of the complete visual prosthesis based on the proposed split architecture is shown in Fig. 2. The system consists of an external unit to acquire images and process them prior to transmitting stimulation data to the implant within the body. The external device is responsible for supplying power and establishing a semi-duplex communications link with the implant. The implant consists

This research was supported by funding from the Australian Research Council as part of its Special Research Initiative in Bionic Vision Technologies.

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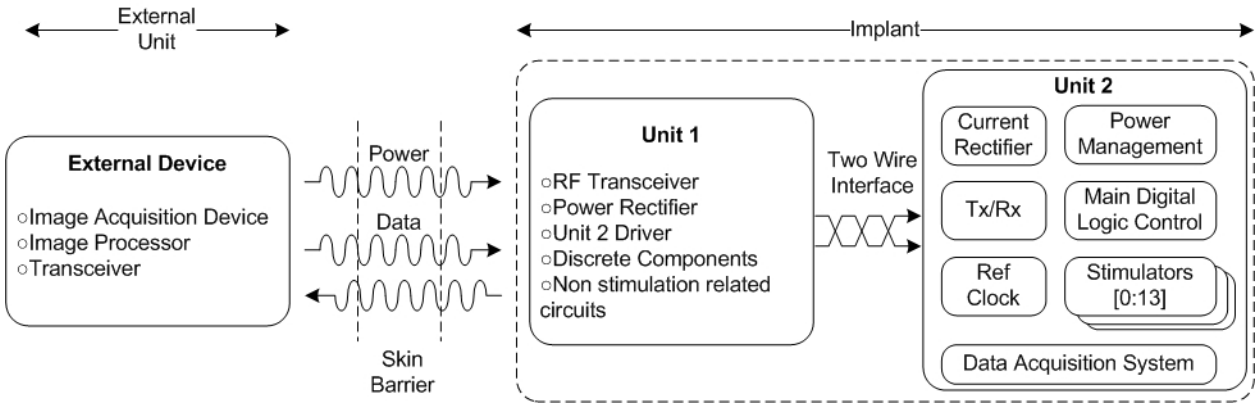

Fig. 2. Block diagram of visual prosthesis based on the proposed split architecture.

of two units. Unit 1, implanted behind the ear, comprises of circuits that are physically large, power hungry and circuits that are not directly involved in stimulation. Such circuits may include RF transceivers and related discrete components, power rectifying diodes, decoupling capacitors and other handshaking and protocol related controls that are essential to successfully communicate to and from the external device. Unit 2 placed in the eye only comprises circuits that are required to carry out the functions of a neurostimulator such as the stimulator, data acquisition modules, local power rectification and a transceiver to communicate to and from Unit 1.

Although such multi-ASIC implants have previously been reported in the literature [3][4], their accompanying multi-wire, DC signal carrying interfaces are more suited for joining modules that are close to each other. For systems shown in Fig. 1 where a lengthy connection is required, the interface should be robust and ideally have a net zero DC value across it to prevent false current paths being formed between the electrodes and the interface itself in the presence of damage to the insulation. The link should also be AC-coupled from Unit 1 to further ensure safety electrically and also to prevent galvanic corrosion of the interface itself.

To meet the specified criteria above a novel two wire interface has been designed and tested. As the name suggests the interface consists of two wires which is the minimum number of wires that can be used to transmit power. AC signals are sent across the interface to achieve a net zero DC across it. Furthermore, square waveforms are sent across the link to minimize the required decoupling capacitance within Unit 2, with a goal to eliminate an external decoupling capacitance and rely completely on an on-chip decoupling capacitor. The link is designed to be driven by current sources and sinks, essentially forming a current-limited voltage source whose current can be monitored to detect abnormalities by Unit 1 during its operation. The communications link from Unit 1 to Unit 2 is achieved by modulating data on to the power signal using a frequency shift keying (FSK) modulation scheme. Data flow in the other direction is achieved by using amplitude shift keying (ASK) modulation of the link itself.

In order to characterize the feasibility of such an interface a 98 channel neurostimlator has been designed. Power saving techniques and thoughtful planning of the system architecture was required to ensure proper operation of an implant incorporating the split architecture. The rest of this paper focuses on the system architecture of Unit 2.

III. System Architecture

This section describes the modules within Unit 2. General functionality and system architecture of each module is briefly described in the following subsections. The focus is not to describe each of the circuits in detail but rather to introduce some of the capabilities of the chip while placing an emphasis on the design techniques employed to realize the proposed architecture.

A. Current Rectifier

The current from the two wire interface is rectified prior to being utilized by the remaining circuits on the chip. The current is rectified by a circuit whose function is similar to that of a full bridge rectifier, however with active switches replacing inefficient on-chip diodes. Sense resistors together with complex switching logic were adopted to accommodate fast transient square current waveforms. Due to the actual circuit operation of this module being outside the scope of this paper, this module is treated as a full-bridge rectifier for the rest of this paper.

A digital signal corresponding to the direction of the incoming current is also generated by this module to be used as data in subsequent modules. The amplitude modulation of the voltage across the two wire interface is achieved by opening and closing of the switches.

B. Power Management Module

The output of the current rectifier is utilized by the power management module to generate 3 power supplies, V_{DDH}, V_{SSH} and V_{DDL}. V_{DDH} is the highest power supply within Unit 2 (8 V to 20 V) which is predominantly set by Unit 1. V_{DDL} (2.6 V) is an internally generated power supply for the

low voltage circuits. V_{SSH} is equal to (V_{DDH} - V_{DDL}) and is used as a floating ground for low voltage (LV) circuits near V_{DDH}. This module is also responsible for generating the virtual ground to which the electrodes can be shorted after stimulation to recover any residual charges that may have accumulated between electrodes. On chip decoupling capacitors were utilized to eliminate the need for an external one. In order to maximize the achievable capacitance, great effort was spent on embedding MOSFET capacitors within the design wherever possible. Also by utilizing capacitive filler cells within the digital logic blocks that have been synthesized, 1 nF high voltage (HV) capacitance was obtainable for the V_{DDH}, 1 nF (LV) for V_{DDL} and 200 pF (LV) for the V_{DDH} - V_{SSH} power supply.

C. Transceiver

The aforementioned digital output of the current rectifier that coincides with the current direction is then processed by the demodulator within the transceiver. A delay element based FSK demodulator [5] with low power consuming delay elements [6] was utilized to decode the incoming data.
As for the reverse telemetry, the binary data generated by the main digital logic block (MDM) is pulse modulated for synchronization reasons and drives the active switches within the current rectifier to induce voltage changes across the two wire interface.

D. Main Digital Logic Block

The MDM consists of five modules namely, a command decoder (CMD), a stimulator module (STM), a data acquisition module (DQM), a status module (STT) and a reverse telemetry module (RVT). Each module comprises a decoder, responsible for local decoding of the incoming data, and a controller, carrying out the function that has been decoded. The serial data output of the transceiver is synchronized within the CMD and is placed on a parallel output bus that is shared with the other modules.
The CMD is responsible for detecting the incoming frame, error detection and redirection of the incoming frame to the target module which is achieved by only enabling the decoder of the module being configured. Once configured the module's controller is set to conduct the programmed task and upon completion the module returns to its idle state. Clock gating is utilized extensively throughout the design to minimize the power consumption of the digital logic blocks within the chip.

E. Stimulator

The chip consists of 14 stimulator blocks. Each stimulator consists of a 7 bit digital to analog converter (DAC) with a current output stage to provide both a current source and a current sink. These are connected to an H-bridge configuration which is then followed by a network of high voltage analog switches controlled by a sophisticated switching logic whose primary task is to control the 7 electrodes in a hexagonal configuration as shown in Fig. 3. The neighboring electrodes surrounding the 7 electrodes

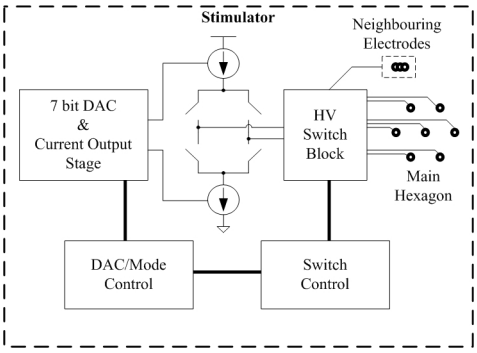

Fig. 3. Block digram representation of the stimulator module.

are also taken into account by the switching logic to allow hexagonal arrangement of electrodes to be formed around each of the electrodes under its control when assigned as a center electrode [7].
Each electrode can also be connected to a bus (SBUS) which can in turn be connected to the virtual ground during shorting periods and to the inputs of the data acquisition system (DAQ).

F. Data Acquisition System

Once a neurostimulator is implanted, it is essential that some analog visibility of critical nodes of the chip is provided to the external device. To meet this criteria, a DAQ consisting of an 8 bit analogue to digital converter (ADC) with a configurable input stage have been designed. The DAQ's input stage consists of 10 low voltage channels and 6 high voltage channels. The low voltage channels are subsequently followed by a low power voltage buffer for sensitive nodes that can be bypassed and a 1 MΩ resistor that can be switched in and out for measuring current. The output of the HV channels are capacitively coupled to the output of the low voltage multiplexer, forming a capacitive divider with the capacitor at the input of the ADC. The DAQ is capable of taking a sample at a time and has access to various critical biasing points within the chip, whether it be a current or a power supply, including SBUS. The DAQ together with MDM can be used to measure a voltage on any electrode reference to the chip ground through repetitive sampling. Each circuit within the DAQ where applicable supports a shutdown mode which is controlled by the STT module within the MDM.

IV. Measurement Results

A prototype chip, shown in Fig. 4, has been designed and fabricated using a 0.35 μm HVCMOS commercial process. The design was conducted using the Cadence design suite.

The test setup used to characterize the performance of the chip is shown in Fig.5. The setup mainly consists of a PXI system (National Instruments, Texas, USA), a custom built two wire interface driver (TWDRV), breakout board with the packaged die and a resistive network of 98 nodes, where each node is joined to all adjacent nodes via individual resistors roughly resembling 98 electrodes in a saline bath.

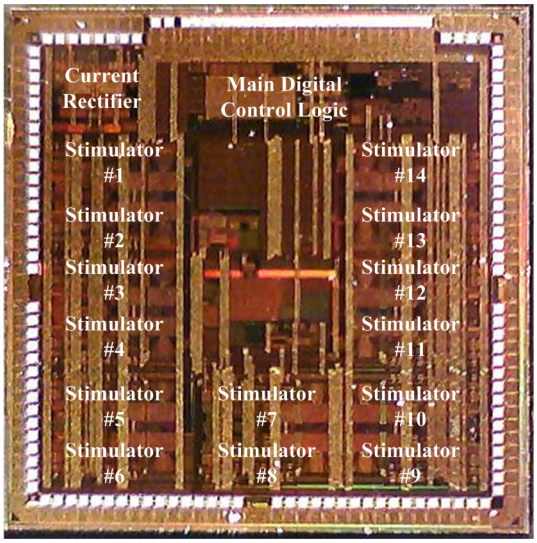

Fig. 4. Die microphotograph of the 98-channel neurostimulator.

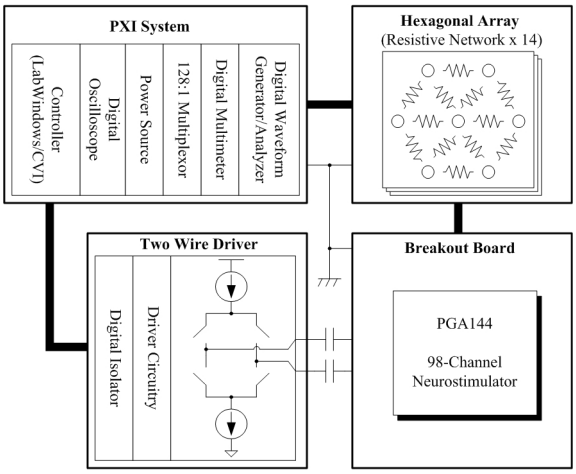

Fig. 5. A simplified block diagram of the test setup used to characterize the 98 channel neurostimulator driven by a two-wire interface.

To allow measurements to be taken by the PXI, Unit 2 and the PXI system were placed on a common ground. Unit 1 was powered by an isolated DC power source in the PXI 4110 DC power supply and driven by the digital vectors generated by the PXI 6541 digital waveform generators isolated by the ADUM440x series digital isolators. The chip was set to be driven by TWDRV both in AC and DC coupled mode. Functional verification of the switching logic was performed using the PXI 2530 with TB 2630 to configure it as a 128:1 multiplexer by calculating the current flowing from individual channels using the voltage measurements across the resistors.

Fig. 6 shows the configuration frame sent across the two wire interface and a bi-phasic waveform generated by the chip across a 1kΩ resistor in response to the incoming stimulation configuration. The stimulator channels were configured to send out a stimulation current of approximately 600 μA. The DC drop across the link throughout the stimulation

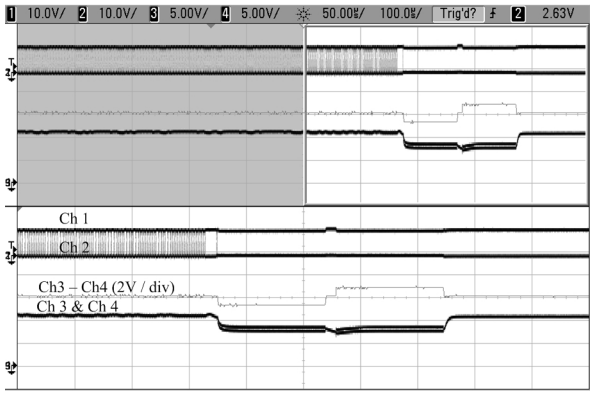

Fig. 6. Measured waveform of a biphasic stimulus across 1 kΩ resistor. Channels 1 and 2 are voltages on the Two-wire interface respect to chip's ground and the channels 3 and 4 are voltages on either side of a 1 kΩ resistor connected to one of the stimulating channel.

is due to the V_{DS} drop across the current source and sink transistors. The system operated without any external decoupling capacitors while not compromising the stimulus current being delivered through any of the 14 concurrent electrodes.

V. Conclusion

This paper provides a system architecture overview of a current driven 98 channel neurostimulator incorporating a split architecture via a two-wire interface. The differentiation of the proposed architecture to those with similar architectures that have been reported in the literature can be made on the interface itself that joins the modules involved. To ensure safety of the interface itself in the presence of an insulation failure, AC square waveforms are sent across the link to achieve a net DC level of zero. In addition to this power is transferred by sending current, essentially realizing a current limited voltage source whose current can be monitored in Unit 1 as another measure of safety and diagnostic mechanism.

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