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Iono-Neuromorphic Implementation of Spike-Timing-Dependent Synaptic Plasticity

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Abstract— **Spike-timing-dependent plasticity (STDP) is the ability of a synapse to increase or decrease its efficacy in response to specific temporal pairing of pre- and post-synaptic activities. It is widely believed that such activity-dependent long-term changes in synaptic connection strength underlie the brain's capacity of learning and memory. However, current phenomenological models of STDP fail to reproduce classical forms of synaptic plasticity that are based on stimulus frequency (BCM rule) instead of timing (STDP rule). In this paper, we implemented a novel biophysical synaptic plasticity model by using analog VLSI (aVLSI) circuits biased in the subthreshold regime. We show that the aVLSI synapse model successfully emulates both the STDP and BCM forms of synaptic plasticity as predicted by the biophysical model.**

I. Introduction

INFORMATION storage in the brain depends upon stimulus-induced synaptic modifications in neuronal networks. This phenomenon is called synaptic plasticity. It is now well-established that synaptic connections could be strengthened or weakened depending on the relative timing between presynaptic and postsynaptic activities [1]. This remarkable phenomenon, generally known as spike-timing-dependent plasticity (STDP), provides strong evidence for Hebbian theory of associate learning and memory.

Synaptic plasticity has been extensively studied under the STDP framework. Several models (e.g., [2][3]) have been proposed aiming at reproducing the experimental data with a mathematical expression to reproduce the STDP characteristic phenomenologically. The limitation of these empirical models is that they do not explain the biomolecular mechanisms underlying STDP at a cellular level.

In contrast, mechanistic models of synaptic plasticity [4]-[6] based on biophysical mechanisms at the molecular level are more informative in interpreting experimental findings. Starting from the calcium control hypothesis [4] which supports the well-known Bienenstock-Cooper-Munro (BCM) rule [7], these mechanistic models suggest that repetitive postsynaptic NMDA receptor activation allowing an influx of calcium ions is the trigger for activity-dependent synaptic plasticity. These receptors also serve as temporal coincidence detectors that relate the temporal pairing of glutamate release from presynaptic terminals and the back-propagation of postsynaptic action potentials up the dendritic tree for STDP induction. However, current mechanistic models of BCM synaptic plasticity cannot explain certain STDP responses, and vice versa.

Recently, a unified model of synaptic plasticity [8] has been proposed that captures the general biophysical processes governing synaptic plasticity. This model considers different types of STDP characteristics reported in the literature and relates them to the BCM rule. It provides a novel modeling approach that overcomes many challenges faced by previous models. Here, we propose a novel iono-neuromorphic (i.e., ion channels-based) analog very-large-scale-integration (aVLSI) circuit that emulates synaptic plasticity based on this unified model.

II. Synaptic System Architecture

The synapse based on the unified STDP model mainly produces two outputs: total calcium level and excitatory post synaptic current (EPSC) representing synaptic weight changes, where EPSC is measured in biological experiment to determine whether STDP occurs in a synapse. However, calcium level is difficult to measure due to limited experiment techniques. Our circuit provides insight about how the calcium level changes in the synapse.

Figure 1 depicts the architecture of the synapse model and its plasticity based on actual biophysical reactions in the synapse. Presynaptic stimuli lead to the release of glutamate neurotransmitter, which is illustrated by the module *Glutamate Receptor*. Postsynaptic activation leads to the propagation of the dendritic action potential in *NMDA channel*. Calcium signaling reaction begins when NMDA receptors promote calcium influx, which is enabled by a glutamate influx and prolonged membrane depolarization due to the back propagating dendritic action potential. This function is described in model *Calcium Integrator*. The final *EPSC Transduction* module constructs the balance between the kinase and the phosphatase, which is determined by the total amount of calcium flowing to the postsynaptic membrane.

Our design chooses current mode circuit based on iono-neuromorphic modeling with ion channel details [9], which is different from silicon neurons in other neuromorphic models with only limited ion channel descriptions. The rest of this section describes the circuit blocks in details.

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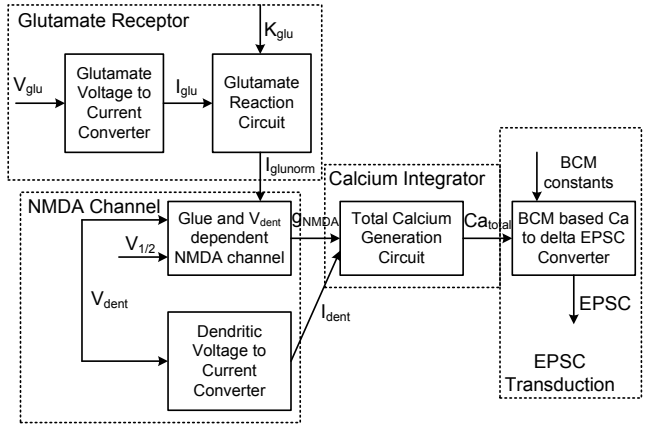

Figure 1: Block diagram for aVLSI synapse

A. Glutamate Receptor

It is shown that NMDA receptor-gated ion channels are the main pathways for calcium flux to the postsynaptic neuron [10][11]. To open the NMDA-receptor channels, it requires both the binding of glutamate and a substantial degree of depolarization. Glutamate binding can be described by the ligand-receptor model, where glutamate ligand concentration combines glutamate receptors in the postsynaptic membrane with an association constant of K_{glu}. Ultimately at equilibrium, the ratio of bound glutamate to the total glutamate concentration is given by

$$\frac{\mathrm{Glu}}{\mathrm{Glu}+K_{glu}} \tag{1}$$

The ratio above is a simple arithmetic representation that involves addition and division. Using aVLSI circuitry, we could implement this with a current adder and a current divider. However, since the presynaptic input V_{glu} is a voltage signal, it has to be first converted to current signal by using a wide linear range transconductance amplifier (TCA). Since I_{glu} is used twice in the equation, it was mirrored twice and a constant current K_{glu} is added to one of the mirrored path. A translinear current divider is used to divide the two mirrored currents to obtain the maximum NMDA receptor conductance. The transfer function can be given by

$$I_{glunorm}=\frac{kI_{NMDAmax}I_{glu}}{I_{glu}+K_{glu}} \tag{2}$$

where k and $I_{NMDAmax}$ are constant gain factors. Figure 2(a) demonstrates the schematic circuit we have developed for the Glutamate receptor. The current sink out of the divider is mirrored to be a current source so that it connects seamlessly with the next current block.

B. NMDA Channel Dynamics

A wide range differential pair can be used to represent the dynamics of NMDA channel, as shown in Figure 2(b). According to [8], the model for NMDA channel dynamics shows some dependences of NMDA channel conductance upon both the dendritic voltage and glutamate concentration,

$$g_{NMDA}\left(V_{dent},\mathrm{Glu}\right)=\frac{g_{NMDAmax}}{1+\exp\left(k_{NMDA}\left(V_{1/2}-V_{dent}\right)\right)}\frac{\mathrm{Glu}}{\mathrm{Glu}+K_{glu}} \tag{3}$$

The second term in Eq. (3) demonstrates the glutamate receptor dependence and has been implemented as $I_{glunorm}$ in Eq. (2). The first term is in complicated sigmoid format and seems challenging for aVLSI implementation. However, by studying the I-V characteristic of the differential pair, it is found that its I-V curve was quite similar to the NMDA channel conductance dynamics,

$$I_{out}=I_{bias}\frac{1}{1+\frac{W_1/L_1}{W_2/L_2}e^{\frac{\kappa(V_+-V_-)}{\varphi_t}}} \tag{4}$$

By comparing Eq. (3) and (4), the NMDA channel conductance parameters can be easily mapped into the aVLSI differential pair. I_{bias} is replaced by $I_{glunorm}$ and V_+, V_- are mapped to $V_{1/2}$, V_{dent}. The two MOSFETs of the differential pair should have exactly the same size.

C. Calcium Integrator

Once we have obtained NMDA channel conductance, we can determine the amount of calcium flowing through our synapse to the postsynaptic neuron. As the NMDA receptors are the major gateway of calcium inflow, calcium concentration is proportional to the integration of current flow through NMDA receptors over the time span of stimuli,

$$Ca\propto\int_{t_{stimuli}}I_{NMDA}dt=\int_{t_{stimuli}}g_{NMDA}V_{dent}dt \tag{5}$$

Here the NMDA current I_{NMDA} is the product of NMDA conductance and dendrite membrane potential.

The multiplication between two signals g_{NMDA} and V_{dent} can be negative because V_{dent} can be a biphasic signal. Therefore, a four quadrant multiplier is designed to implement the multiplication in Eq. (5), as shown in Figure 2(c) and (d). The implementation of integration in circuit is trivial as it could be easily achieved by charging a capacitor with calcium flow.

D. EPSC Transduction

Accumulated calcium in the postsynaptic compartment through the action of NMDA receptors strongly influences the action of synaptic plasticity. Depending upon the total amount of calcium inflow, postsynaptic calcium can either upregulate or downregulate the signal transduction pathways that lead to synaptic plasticity. This influence can be achieved in two steps. The calcium binds with calcium-dependent protein kinase or phosphatase. These enzyme-calcium complexes either insert active AMPA receptors [12] from the membrane under kinase or remove AMPA receptors from the membrane under phosphatases [13]. The remaining active AMPA receptors determine the magnitude of EPSC. The above reaction can be illustrated as

$$\mathrm{AMPAR}_{\mathrm{inactive}}\underset{k_{AMPARb}+\mathrm{Activity}(Ca_4P)}{\overset{k_{AMPARf}+\mathrm{Activity}(Ca_4K)}{\rightleftharpoons}}\mathrm{AMPAR}_{\mathrm{active}}$$

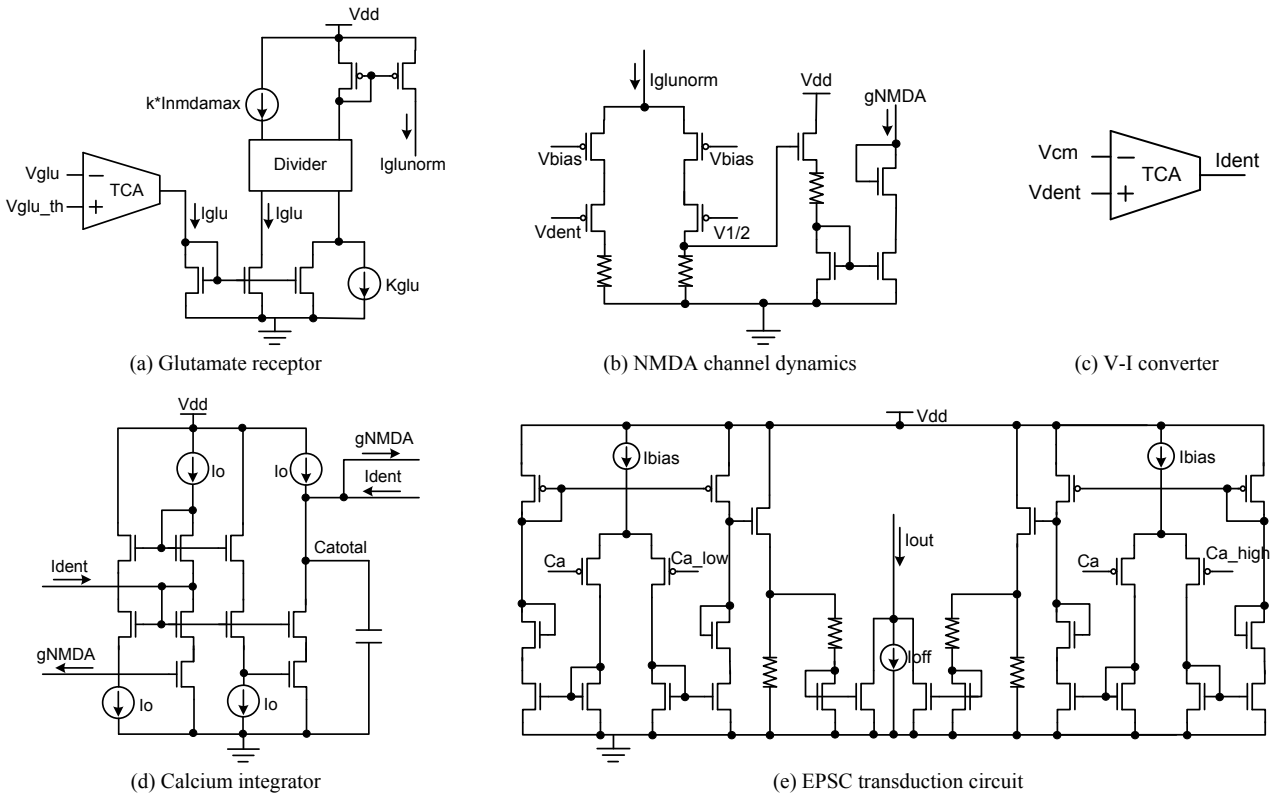

Figure 2: aVLSI building blocks for proposed synapse architecture are illustrated by CMOS circuits.

where k_{AMPAf} and k_{AMAPb} represent the forward and backward reaction rate constants, assuming the total number of AMPA receptors is constant. The change of synaptic strength before and after the application of stimuli can be derived as follows [8]:

$$\Delta W \propto \frac{k_{AMPARf} + Activity(Ca_4K)}{k_{AMPARb} + k_{AMPARf} + Activity(Ca_4K) + Activity(Ca_4P)} - \frac{k_{AMPARf}}{k_{AMPARf} + k_{AMPARb}} \quad (6)$$

The EPSC transduction circuit representing Eq. (6) can be implemented in a mechanistic way, which is one of the most accurate approaches to represent the biophysical processes within the synapse. However, this accuracy compromises the size and complexity of the circuit, which makes the circuit bulky and prone to mismatch problem and is difficult to test. Hence, an alternative and empirical design was adopted as in Figure 2(e), which implements the input-output transfer function implied by Eq. (6).

The circuit implementation utilizes the sigmoidal decomposition, where the transfer function in Eq. (6) is implemented by adding together current outputs of two transconductance amplifiers. The first amplifier (the left half circuit in Figure 2(e)) has a narrow dynamic range and simulates the fast decreasing segment of Eq. (6). The second amplifier (the right half circuit in Figure 2(e)) is designed to have a wide dynamic range and to emulate the slow increasing segment of Eq. (6). The difference in their dynamic ranges can be adjusted by transistor sizing and resistance tuning. The output current I_{out} carries the information of synaptic strength changes ΔW. I_{bias} sets the maxima and minima of synaptic changes and changing I_{off} shifts the synaptic change up or down. The two offset voltages Ca_{low} and Ca_{high} shift the zero-crossing points of synaptic changes to the left or right along the Ca_{total} axis.

III. Results and Analysis

The synapse is designed to verify the proposed unified STDP model [8]. Hence, the natural measurement is to probe the nodes at Ca_{total} and EPSC (I_{out} in Figure 2(e)) to obtain the relationship between synaptic weight and timing difference between pre- and post-synaptic spikes.

Before showing the circuit simulation results, intuitive neurological explanation is shown to explain the simulation results. By investigating Eq. (5), we found that the lag time between the glutamate flux and the arrival of dendritic action potential influences the level of NMDA receptor activation which in turn modulates the amount of calcium influx. Since both transient signals only last for a few mili-seconds, temporal proximity between these two signals is necessary to trigger their interaction.

Figure 3(a) describes the transient profiles of glutamate and dendritic action potential with a lag time of 3ms. Intuitively, if the glutamate overlaps mostly with the positive portion of action potential, the NMDA receptor is activated causing more calcium to flow into postsynaptic neuron. On the other hand, if glutamate influx occurs during the same time of the negative portion of the action potential,

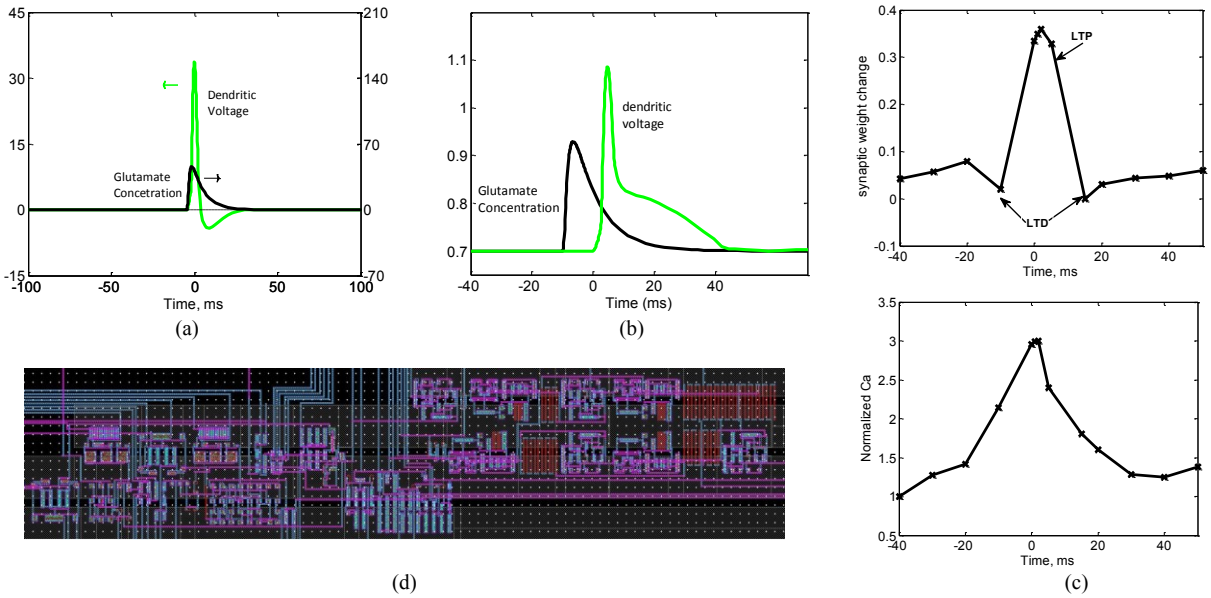

Figure 3: Two different types of glutamate concentration and dendritic voltage in (a) and (b), Ca_{total} and EPSC in (c) and synapse layout in (d).

the NMDA receptor is not fully opened, which results in less calcium inflow. The above analysis leads to the asymmetric STDP response that is often seen in STDP literatures.

The proposed synapse was designed using Cadence and the simulation was performed by Spectre. We tested the synaptic plasticity by measuring the calcium level integrated over the stimulus period and EPSC magnitude representing the change in synaptic efficacy. Synaptic plasticity was induced with varying time offsets, ΔT, between the two inputs V_{glu} and V_{dent}. A positive ΔT implies that a dendritic action potential comes after the glutamate stimulus, while a negative ΔT signifies the opposite timing. Here we used a specific shape for V_{dent} as shown in Figure 3(b) to generate a symmetric type of STDP response with one LTP and two LTD domains as in [4]. Figure 3(c) shows the symmetric STDP response by plotting the Ca_{total} and EPSC (ΔW) for different values of ΔT. Figure 3(d) gives the layout of the aVLSI synapse with the MIT Lincoln Lab ultra-low-power 150nm FDSOI CMOS technology [14]. The die size is 1mm × 4mm and its power consumption is 500nW on a 1.2V power supply.

IV. Conclusion

We have demonstrated the design of an aVLSI synapse with NMDA receptor-dependent synaptic plasticity on the MIT Lincoln Lab ultra-low-power 150nm FDSOI CMOS process. The aVLSI synapse is capable of reproducing all types of symmetric and asymmetric STDP responses. (Here due to limited space, only the symmetric STDP curve is shown.) The designed synapse is in theory able to emulate both time- and rate-based plasticity, as predicted by the unified model. Our next step is to test this hypothesis using rate-modulated presynaptic stimuli both in simulation and in hardware on-chip measurements.

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