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Development of Cost-effective Biocompatible Packaging for Microelectronic Devices

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***Abstract* - A cost-effective, miniaturized and biocompatible packaging method for medical devices is proposed, resulting in a small, soft and comfortable implantable package.**

Towards this end, the barrier materials and fabrication process for the individual die encapsulation are largely explored. We demonstrate that various common clean room materials are good candidates for preventing metal leaching into body. In accelerated tests at higher temperature, several conductive barrier materials are damaged by the test bio-fluid, suggesting insufficient resistance to body fluids in long term. Covering electrodes by noble metals will solve this problem.

For metallization, noble metals as Pt are best candidates. CoO calculations showed that selective plating of Pt is more cost-effective than sputtering. To reduce the cost of a sputter process, Pt recycling is very important.

I Introduction

Traditionally implantable electronic devices are packaged in rigid Titanium boxes to ensure hermetic packaging of the microelectronic parts. Such a large Ti box causes a larger insertion wound and a more pronounced Foreign Body Reaction (FBR), and a higher risk on adverse effects such as infection and irritation during device use.

The miniaturization technologies in packaging of microelectronics can be extended towards packaging of implanted medical devices. By selecting proper materials, the final package can be made soft and biomimetic, resulting in a small and comfortable implantable device, causing limited FBR and adverse effects.

II Packaging Concept

The concept of this implantable package is illustrated in Fig. 1. Three main phases are distinguished. First, individual dies (or subdevices) are encapsulated by one or more capping layers which should provide a hermetical enclosure for each die (Fig 1a). The encapsulation consists preferably of more than one layer, to avoid any influence of possible pinholes, and hence ensuring hermeticity. The capping layers should be biocompatible and fulfill the task of bi-directional diffusion barrier: no body fluids should leach into the device, and no diffusion of harmful materials such as Copper (Cu) should diffuse into the body tissue.

In phase 2, the various chips of one device are assembled in an interposer-like package (Fig. 1b). Finally, in phase 3, the assembly of the final device is performed (Fig 1c).

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In phase 2 and 3, the sub-devices should be embedded in a biocompatible material which provides sufficient mechanical support for the subcomponents. The final embedding is preferably done using a soft, flexible material such as PDMS, to limit the FBR upon implantation. For the metallization in step 2 and 3, a biocompatible metal is used, with strong corrosion resistance even when exposed to body fluids. Gold are Platinum are very interesting candidates.

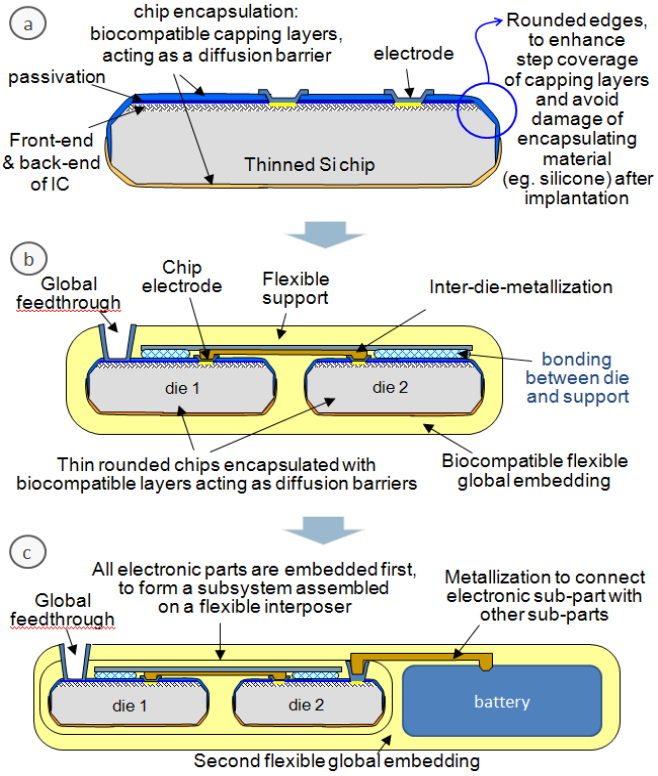

Fig. 1. *Imec's proposal for compact implantable packaging (a) all chips are individually encapsulated; (b) metallization and embedding of multiple chips; (c) final system assembly including metallization and final embedding.*

III Fabrication of Die Encapsulation

For the first phase of this packaging concept, a dedicated process is developed for the chip encapsulation (Fig 2). To obtain a cost effective process, phase 1 is carried out as wafer-based post-processing in the clean room (CR), hence many chips are processed simultaneously.

The individual chips are partially diced using an adjusted process to realize a slope at the top of the groove. Next, the top and sidewalls of the chip are covered with a stack of

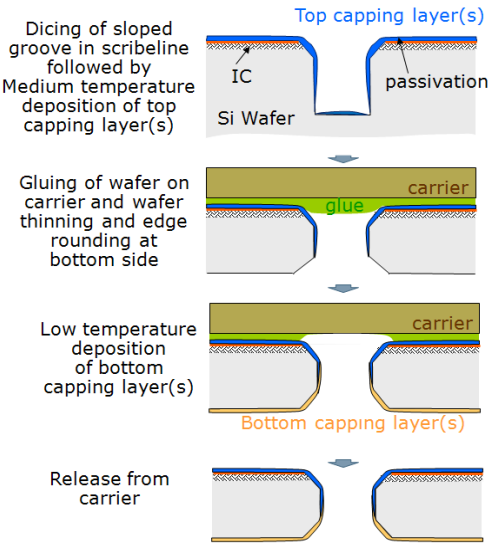

Fig. 2. *Process scheme of a hermetic wafer level chip encapsulation technique using only two deposition steps in order to cover all sides of the dies.*

barrier layers to form a bi-directional diffusion barrier. The deposition should be done at temperatures below 400℃, to maintain chip functionality. At such temperature, step coverage of deposited layers is often problematic, hence a dedicated process needs to be developed, since poor step coverage will result in poor barrier properties. For the backside processing, the wafer is glued upside down on a carrier wafer and the wafer is thinned down to ~50µm. The backside chip corners are rounded and all chips are covered with the backside barrier layers. An early stage demonstrator of the chip top rounding and encapsulation is shown in Fig.3. Excellent step coverage has been obtained with a dedicated oxide deposition process carried out below 400℃. Also the vertical sides of the chips are nicely covered with this oxide capping.

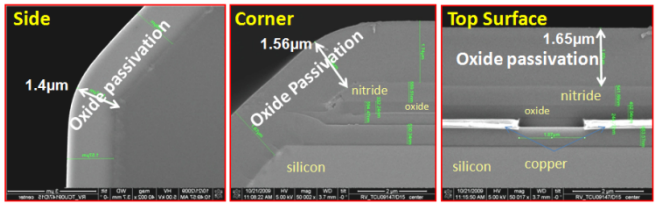

Fig. 3. *SEM picture of a encapsulated die with excellent step coverage of the edges by silicon oxide. A dedicated medium temperture process is developed for the oxide deposition.*

III DIFFUSION BARRIER MATERIALS

The capping materials used for die encapsulation should be biocompatible and should serve as suitable bi-directional diffusion barrier. With respect to electrical properties, two types of materials needs to be identified: insulating barriers and barriers which are conductive to fabricate the electrical contacts, as shown in Fig 4.

A. Selection of barrier layers

The insulating capping layers can be composed of Silicon oxide (Ox) and nitride (N), two well-known materials in a standard CMOS CR. Since the backside process flow uses a

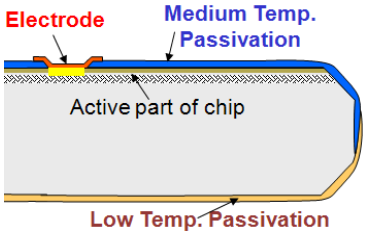

Fig. 4. *Cross-section of an encapsulated chip. The passivation layers form an insulating barrier, the interconnection electrode needs a conductive barrier. The total barrier consists typically of various layers.*

glue not stable above 200℃, the bottom capping layer should be deposited at a lower temperature. Therefore we investigated silicon oxide and nitride deposited at a medium temperature of ~400℃(OxM and NM) and at a low temperature of ~200℃ (OxL and NL).

For the conductive barrier, again well-known CR materials are good candidates: titanium (Ti), Ti-nitride (TiN), tantalum (Ta) and Ta-nitride (TaN). Depending on the deposition process these materials can be biocompatible and can have interesting barrier properties [1-3].

B. tests for cytotoxicity and Copper diffusion through barrier layers

To investigate the biocompatibility of the material, cytotoxicity tests are performed based on ISO10993. A thin layer (~100nm) of the barrier material is deposited on a blanket silicon wafer and diced into small pieces for testing. After cleaning, a glass ring is glued on the surface with biocompatible PDMS to define the cell culture area.

To test diffusion properties, two types of tests are needed: evaluation of Cu diffusion through the barrier layer by Cu sensitive cell cultures, and evaluation of fluid leaching through the barrier layer by Cu corrosion tests. For the first test, cell cultures are carried out on ~100nm thick barrier layers deposited on blanket Cu wafers. For this test, Cu is chosen since it is commonly present in chips and since it is known to be toxic for most cells [4]. Cu corrosion tests are currently ongoing hence they are not discussed in this text.

Mice primary cardiomyocytes are used, standard cell culture dish (C-) and pure Cu are selected as negative and positive control. After 5 days co-culture, cell viabilities are determined by fluorescence staining and cell counting. Following the USP standard, up to 20% decrease from the negative control is still considered as non-cytotoxic, although we consider a viability decrease >10% as unacceptable, since we aim for long term implantation. In the following graphs, the areas of ±10% viability deviation from the control are marked by a green background.

For all tests, all cells died on pure Cu after one day incubation, and the copper surfaces corroded significantly.

For the insulating barriers, the test results are shown in Fig. 5. None of the materials is cytotoxic for these cardiac cells. The diffusion barrier tests (Fig. 5, right) revealed that ~100nm OxL is not performing well as barrier, also NL is performing marginally. The layers deposited at higher temperatures are typically from better quality, also the diffusion tests show clearly this trend, ~100nm OxM and NM are good diffusion barriers for the top layer. For safety,

always a stack of OxM and NM will be used in the final devices. For the bottom layer, covering only silicon, NL in combination with ie. Parylene might be sufficient as a first protection barrier. Before moving to Phase 2, also the top of the dies might be further protected by Parylene.

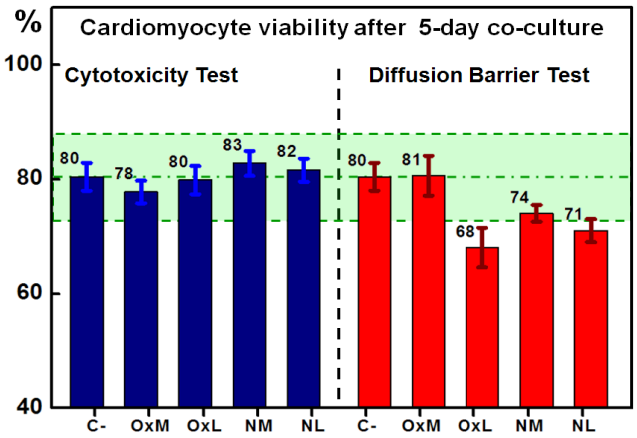

Fig 5. *Cadiomyocytes viability after co-culture tests on insulating barrier materials. C- stands for negative control, i.e. standard cell culture dish.*

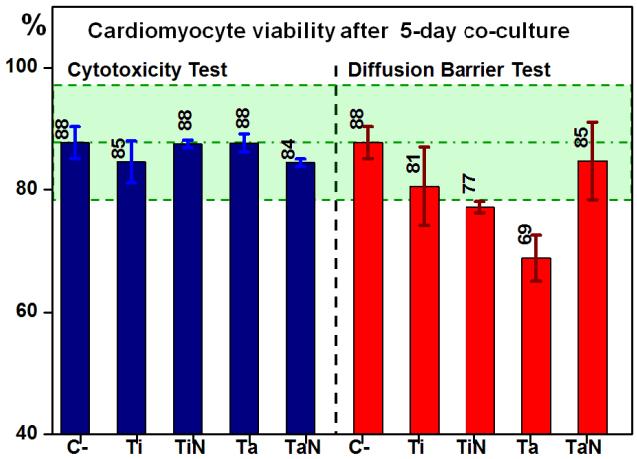

Fig. 6. *Cardiomyocyte viability after co-culture tests on conductive barrier materials.*

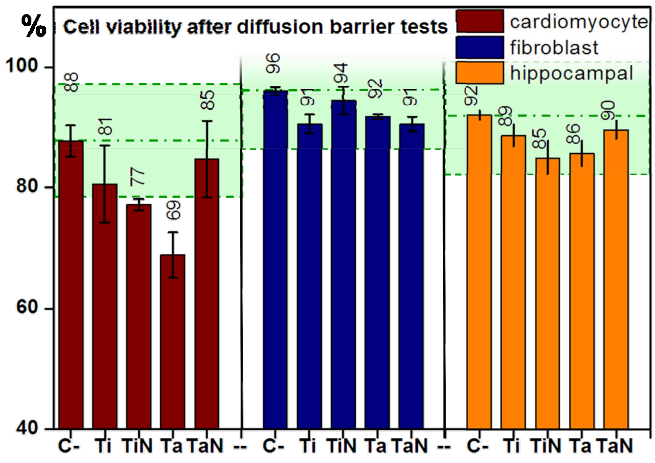

Fig. 7. *Cell viabilities determined using various types of cell after co-culture on conductive barriers. Cardiomyocytes seem most sensitive to Cu.*

Also for the conductive barriers, the cytotoxicity tests results are very good, as shown in Fig. 6 (left). With respect to diffusion properties, we can conclude that ~100nm Ta is not performing well, and 100nm TiN has only marginal barrier properties, but might be fine if thicker layers are used. Ti and TaN are performing very well.

Various cell types have a different sensitivity for the presence of Cu. We have seen that cardiomyocytes were repeatedly showing a higher sensitivity to Cu than primary fibroblasts or hippocampal cells. One test result of the many comparisons we did is shown in Fig. 7. Diffusion barrier tests are shown, using cardiomyocytes, fibroblasts and hippocampal cells. Although the diffusion of Cu is the same, only the cardiomyocytes show clearly that Ta and TiN do not perform well. Because of this, we prefer to test barrier properties by Cu diffusion tests using cardiomyocytes.

C. Accelerated diffusion tests

Long term implants might stay 50 years or even longer in the body, hence accelerated testing with respect to bi-directional barrier properties is essential. Diffusion and Mean Time To Failure (MTTF) are related to time and temperature, as expressed in the Arrhenius equation [5]:

$$MTTF = A\exp(-\frac{Ea}{kT})$$

A is the pre-exponential constant,
Ea is the activation energy
T is the temperature in Kelvin,
k is the Boltzmann's Constant.

High temperature accelerated tests were performed for conductive barrier materials. The barrier-on-Cu samples were incubated at 70℃ (according to USP standard) with Dulbecco's Modified Eagle Medium (DMEM) on the top surface for 4 days. To compensate for evaporation, some DMEM was added daily. Then, the sample surfaces were inspected under microscope after cleaning with DI water. For all four barrier metals, the surfaces suffered from some erosion caused by the DMEM solution. The TiN surface is damaged most severely (Fig 8). The orange-colored haze is a remnant of DMEM and can be wiped away easily, but the dark spots on the surface seem to be etched copper.

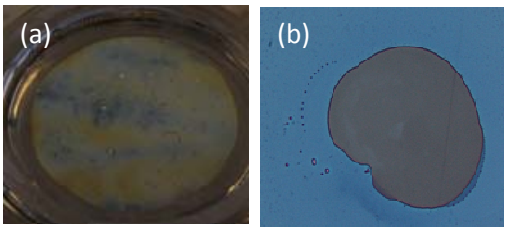

Fig. 8. (a) damaged TiN surface after an accelerated test with DMEM, (b) microscopic view of a dark spot.

Since the conductive barrier materials under test are not resistant to culture medium at high temperature, it is reasonable to predict that those materials are not stable in body fluids in the long term, although more tests will be performed to understand the surface damage better. For the final barrier stack, we propose to use a much more stable metal as top layer, such as Platinum.

IV Cost calculation of Platinum metallization

For metallization of a long term implant, low electrical resistivity combined with extreme corrosion resistance is needed, hence noble metals such as gold or platinum (Pt) are very good candidates. Pt is preferred due to its superior corrosion resistance, but has an important disadvantage: its cost. Since in each packaging phase Pt metallization will be used, the cost of it will be important. To understand this cost better, Cost of Ownership (CoO) calculations are performed.

For calculating the CoO for phase 1 of our packaging concept, we suppose an annual production of 100.000 wafers of 200mm diameter in a standard CR. Standard CR tools are assumed, with corresponding maintenance costs, CR floor space cost, process labor cost, etc. Using die encapsulation processes as described above, the cost of phase 1 is in the order of 25US$ per wafer, excluding the Pt metallization cost. The cost of phase 2 excluding Pt metallization can only be estimated since the process is not fixed yet, we calculated a cost between 40 and 80 US$ per wafer.

For the Pt metallization, two deposition processes are commonly used: sputtering combined with lift-off, and selective electroplating combined with seed layer deposition and later removal. For both processes, a CoO calculation is performed for 200mm wafers which need Pt metallization supposing the need of 30% wafer coverage by this metal.

For Pt plating, 80% bath depletion and 75% plating efficiency is assumed. The cost of a commercial available plating solution is used, and standard CR tools are assumed. Based on these assumptions, one Pt metallization step cost ~30US$ per wafer, from which 17US$ is raw material cost.

For Pt sputtering, recycling of material is a key factor to reduce the cost. Pt targets have to be replaced before they are fully consumed, but target recycling is common and can be done with 95% cost efficiency. Sputtering efficiency is the relative amount of Pt deposited on the substrate, compared to the total Pt deposition, hence including Pt deposition on chamber walls, the shutter and the wafer holder. Sputtering efficiency depends on the tool configuration; we assumed an efficiency of 70%. Recycling of Pt scraping from walls etc. is possible but not straightforward, hence a cost efficiency of ~80% is realistic. Recycling of Pt from the lift-off fluid is far from standard but might be possible. We supposed this recycling step can be done with 50% cost efficiency. The Pt sputter process with target recycling is further called 'S1', with additional scraping recycling is called 'S2', and with target, scraping and fluid recycling is called 'S3'.

Fig. 9 shows the CoO calculations resulting in the Pt material cost and the total cost (tool, labor, material,..) for one Pt metallization step on a 200mm wafer. Selective plating is obviously much more cost effective than sputtering, even when maximum Pt recycling is performed. For a Pt coverage of 30%, plating costs 30US$ a wafer, sputtering from 45 to 60US$, depending on Pt recycling options. For all cases, the cost of Pt metallization will form a considerable part of the total implantable package cost.

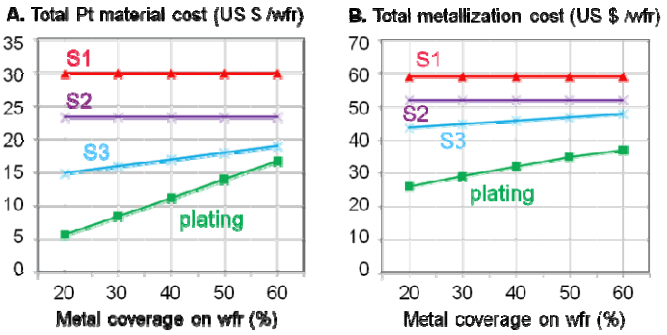

Fig. 9. *Cost of Pt material (A) and of the total Pt metallization step (B) for one 200mm wafer, using Pt plating and sputter processes. Sputtering is always more expensive, even when maximum Pt recycling (S3) is applied.*

V Conclusions

A cost-effective, miniaturized and biocompatible packaging method for medical devices is proposed, resulting in a small, soft and comfortable implantable package.

Phase 1 of this packaging concept is largely explored; various common clean room materials are tested with respect to their suitability as biocompatible barrier layer. Cytotoxicity tests and Cu diffusion tests showed that several materials –both insulating and conductive materials- are excellent candidates as barrier layer, but corrosion tests still need to be performed. Various standard processing steps are adjusted towards this specific encapsulation goal, in order to meet the various requirements. Accelerated tests at higher temperature revealed that various conductive barrier materials are damaged by the test bio-fluid, suggesting insufficient resistance to body fluids in long term. Covering electrodes by noble metals as Pt will solve this problem.

CoO calculations showed that selective plating of Pt has higher cost-effectiveness than sputtering. To reduce the cost of a sputter process, Pt recycling is very important.

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