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A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-driven Microfluidic Devices

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Abstract— **Recent research has demonstrated the use of microfluidic devices and electro-kinetics in areas such as medicine, genetics, embryology, epidemiology and pollution analysis, where manipulation of particles suspended in liquid media is required. Micro-fabrication technology has made it possible to increase system complexity and functionality by allowing integration of different processing and analysis stages in a single chip. However, fully integrated and autonomous microfluidic systems supporting ad-hoc stimulation have yet to be developed. This paper presents a flexible, configurable and programmable stimulator for electro-kinetically driven microfluidic devices. The stimulator is a dedicated System-on-Chip (SoC) architecture that generates sine, triangle, and saw-tooth signals within a frequency range of 1Hz to 20 MHz, capable of delivering single, dual, and superimposed waveforms, in a user defined test sequence for a selected time period. The system is designed to be integrated into complete, autonomous Lab-on-Chip, portable or implantable devices. As such, it is expected to help significantly advance current and future research on particle manipulation.**

I. Introduction

Research on fluidic transport at micrometer scale has received considerable attention in areas such as medicine, genetics, embryology, and epidemiology, where isolation of specific particles is a main step in experimental procedures. Microfluidic devices contain channels where suspended particles in a buffer may be trapped and separated. Electric stimulators generate electric fields through channels manipulating particles with electrokinetic forces, being the preferred particle manipulation technique as it is flexible and compatible with miniaturization.

The precise effect of a particular waveform, amplitude or frequency over a specific type of particle is an active area of research. Current manipulation experiments use standard equipment like signal generators in predominantly manual procedures; this implies tedious, slow, inefficient, and inaccurate set-ups, leading to slow progress in the related research. Recent proposals on fluid sample stimulation suggest that more complex stimulation using highly controlled experiments could improve results and lead to new lab procedures and tests.

In this paper, we present the first design of an autonomous, configurable, integrated stimulation System-on-Chip (SoC) for microfluidic devices. This stimulation system represents a flexible solution for a variety of setups and applications: it has configuration options to define specific complex and automated test procedures beyond the limitations of current stimulation systems. Furthermore, its integrated open nature enables miniaturization for application in a wide range of areas, e.g. as a key component of implantable, portable, Lab-on-Chip or Point-of-Care.

The rest of the paper is organized as follows: after a discussion of related work in Section II, Sections III and IV present the system design and physical realization. Finally, Section V concludes with a summary and outlook.

II. Related work

Particle manipulation experiments, which use electric stimulation, have been performed since the early 70's using signal generators and frequency synthesizers for this purpose. Current research suggests that configurable systems would provide a more controlled experimental environment [1] allow researchers to explore new areas [2]. Though there are proposals for configurable stimulation systems, they tackle the integration problem partially by focusing on specific waveforms or frequencies [3], or by presenting fewer configurable options [4]. Some proposals are too specific to be considered in other settings [5][6] and other present a partial integration of elements [7][8] or they focus on particular experiments only [3]. Some CMOS based designs [3][9] use dedicated systems that can not be re-configured. In contrast to standard signal generators, our system allows for automated delivery of complete sequences of superimposed signals. To the best of our knowledge, there is currently no integrated solution for a stimulation system that can be used on a variety of particle manipulation environments and allows for full integration with the next generation of devices.

A flexible design like the one presented here targets a wide range of experiments and applications where microfluidic devices are used. It can run as a stand-alone module, be integrated as a block into Lab-on-Chip designs or be the base design to develop customizable systems, allowing for integration with such recent proposals and designs as presented in [9][10].

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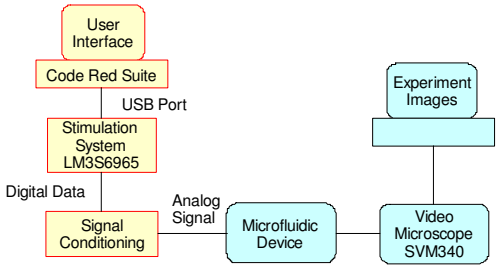

Figure 1. System setup.

III. SYSTEM DESIGN

The system presented here is a configurable, programmable System-on-Chip (SoC) design that can deliver multi-waveform dual-frequency signals. Figure 1 shows the elements in a particle manipulation setting: user and configuration interface on a PC, stimulation SoC, signal conditioning circuit, fluidic device, video-microscope, and a PC for analysis and storage of the experiment images.

Instead of a board-level implementation we propose a specialized and customized design that targets portable or implantable devices where area and power are important parameters. This SoC design also finds application in existing Lab-on-Chip developments, in which it can be externally added as the stimulation module or be integrated at the chip level using the external data and instruction bus interfaces included in the design.

Careful design considerations and trade-offs were made in order to achieve a low power, small area, and high performance design. In relation to storage requirements, instruction memory space was reduced by sharing functions between operation modes. Memory space for data samples and processed data was minimized by reducing base waveform data samples and by re-using data structures for pre-processed and output across operation modes.

To achieve a high performance and a maximal output to clock frequency ratio, we minimized the number of load-store transactions performed during data pre-processing and signal generation. Furthermore, all data samples for signal superimposition are processed before signal generation begins. As such, no computation instructions are executed during frequency synthesis and only a minimum number of clock cycles is needed for writing out the final data samples.

The application program itself was designed to be as modular as possible for maximal function code re-usability. The same set of routines and program flow is used regardless of the signals, patterns or sequences to be delivered: 1) store the base data samples for selected waveforms, 2) get configuration and operation parameters 3) pre-process data samples to get desired frequencies and operation modes, 4) generate a single data table for signal generation, and 5) execute a cycle of frequency synthesis.

A. *Hardware Description.*

The application specific hardware architecture designed for this modular bus-based system consists of a processor, a memory system, peripherals, and on-chip and communication buses. Figure 2 shows the block diagram of the stimulation SoC. It was designed using freely available synthesizable components models from OpenCores.org. A central OR1200 processor runs the application software. Application code and boot loaders are stored in the ROM array. A RAM array holds waveform samples and temporary data generated during execution. Memory arrays were built using Artisan Memory Generators. Parallel and serial ports are provided via four 8-bit GPIO and standard UART peripheral from OpenCores.org. The parallel port is used to deliver data samples for frequency synthesis. The serial port is used to communicate with external PC that runs the user interface, controlling overall system operation. All peripherals, memories and cores are connected via an internal Wishbone bus. Corresponding bus wrappers were added to peripheral cores and memories. Bus bridges (BIUs) allow for interfacing the SoC with external components.

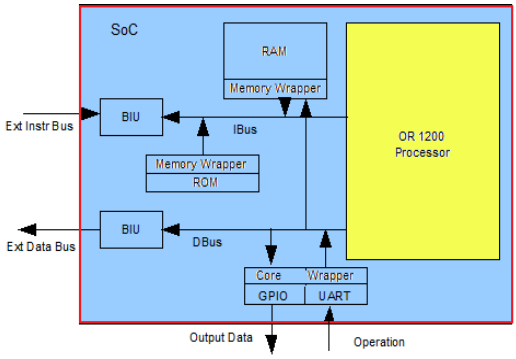

Figure 2. Hardware architecture and in-chip blocks.

B. *Software Description.*

The main functionality of the application-specific program is to deliver signals with single or dual frequency for any superimposed mix of 3 basic waveforms (sine, triangle, and sawtooth). Execution and operation modes are based on user selected parameters such as frequencies, waveforms, superposition, waveform mix, exposure times, etc. which define specific stimulations for particular experiments.

A novel frequency synthesis methodology is employed to process data from base waveform samples. It first creates temporary data tables for frequencies f_1 and f_2, and then creates a single output table containing single, separated or superimposed frequencies to be sent to output ports. Data pre-processing executes all the needed computation before signal generation begins, so no computation occurs during signal generation cycle. In all operation modes a simple final address-load-store cycle takes a minimum time between port updates to achieve maximum output frequencies. Modular code allows to add or remove functions for a specific application, to integrate additional waveforms, and to extend the number and size of data samples. A single table creation routine and a single data memory space are used for all operation modes. Base data tables, temporary tables and output data tables are stored in up to 8K-byte data memory.

TABLE I
ROUTINE LIST AND DESCRIPTION

Element	Description
Get operation parameters	Get operation mode, waveform, samples per cycle, output frequencies, and time of exposure.
Set output signal pattern	Set from: single sine, triangle, or sawtooth, 2 superimposed sinusoids, a superposition of sine over sine, triangle over sawtooth, triangle, etc.
Calculate time and space separation	A memory space separation is calculated as the time separation between data samples for resulting signal patterns.
Do time match Modes 2 & 3	Generate one single table containing both sets of data samples matching in time.
Create Temp Tables	Extract data from original data table to construct data table for 1 signal output or for 2 superimposed or separated frequencies.
Output Signal Generation	Load from data table and store to parallel port loop. No computation instructions executed.

The application software requires less than 3Kbyte of instruction memory. Table I summarizes the software routines and program flow.

C. Configurable features.

The system supports configurable features and programmable parameters either defined during the design stages or set on operation to achieve a flexible implementation:

Pre-loaded application. The application program is stored in on-chip ROM as a generic application to cover a variety of standard stimulation procedures and experiments. A modified boot loader can read a specific application from external memory on startup, e.g. when frequent modifications to the software are expected.

Waveforms. Available waveforms are sine, triangle and sawtooth with 256 8-bit data samples each. 8 bit data samples support output signals with 256 voltage steps from –V (00x0) to +V (FFx0). The data width can be extended to 16 or 32 bits by grouping GPIO ports.

Operation modes. The system provides 4 output channels via 8-bit parallel ports each supporting single or superimposed frequencies.

Output frequencies. The maximum output frequency is $f_{max} = (f_{clk})/(n*N)$, where $\boldsymbol{f_{clk}}$ is the system clock frequency, **n** is the number of samples in the signal cycle, and **N** is the number of clock cycles between samples.

Output sequences: The same or an unlimited sequence of different signal patterns can be sequentially and repeatedly delivered for user selected time periods.

IV. SYSTEM REALIZATION

The SoC architecture was synthesized with Synopsys Design Compiler using TSMC Physical Libraries for cost-effective 180µm technology. RAM and ROM arrays were built with Artisan Memory Generators. Place and route, clock tree synthesis and IO ring design were realized with Synopsys IC Compiler. Power analysis and grid design were performed using Prime Time-Px. Processor, peripherals and on-chip communication buses were synthesized using Verilog source code from OpenCores.org.

TABLE II
SYSTEM OPERATING FREQUENCIES

Concept	Operating frequency
System Clock	190 MHz
Wishbone bus clock	47.5 MHz
GPIO, 8 bit data Load and Store	5.94 MHz

TABLE III
AREA AND POWER BY BLOCK GROUP

Block	Area, mm^2	Power, Watts
Processor	1.4866	0.17696 W
Memories	1.9772	0.14540 W
Peripherals	0.0522	0.00638 W
Bus and interconnect	1.4694	0.00962 W

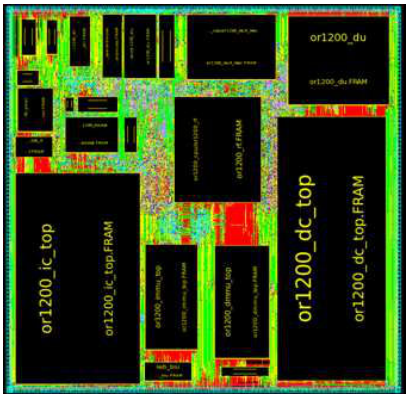

Figure 3. System-on-Chip layout.

Timing analysis was performed during the synthesis process to determine implementation-dependents system clock, bus clock, and port clock frequencies. Final post-synthesis timing parameters are shown in Table II. With the processor running at 190 MHz, the execution time of the parameter set up function in the application software is 168ns to get the operation parameters from the user and generate the related data. Data processing requires 3368ns to create temporary and output tables for 2 frequencies with 32 samples each. Finally, the time between samples during signal generation is 21ns.

Power and area numbers after synthesis are shown in Table III. Block power considers full throttle operation. Minimum area was achieved by varying the aspect ratio of mayor blocks. Table IV summarizes the final parameters for the synthesized design, in TSMC 180µm technology. Figure 3 shows the final SoC layout.

The application software and system design was tested and prototyped on an ARM-based development board using a setup as shown in Figure 4. Figure 5 shows samples of signal patterns delivered by the application for single and superimposed frequencies of a varying mix of waveforms.

To demonstrate functionality and applicability of this system, we applied our prototype to stimulation of a microfluidic CarbonDEP device with saccharomyces cerevisiae ATCC 24858 cells in DI water. Manipulation was observed in a SVM340 video-microscope. Live and dead

TABLE IV
SOC MAIN PARAMETERS

Concept	Value
Area	2.44 x 2.44 mm^2
Power	0.523 Watts
Operating frequency	190 MHz
IO pins	189 pins
Instruction/Data Memory	8 KB/ 8 KB

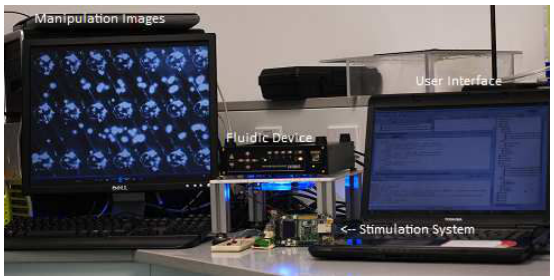

Figure 4. Experimental environment: user interface, processor based stimulation system, and images from video-microscope.

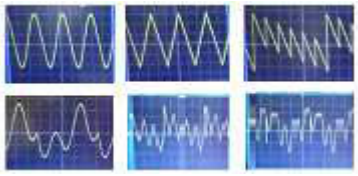

Figure 5. Sample delivered signals.

yeast cells were successfully separated by applying a 4 V_{pp}, 100 Hz sinusoidal signal. Another experiment used a mixture of viable yeast cells and 10.14 µm carboxylated polystyrene particles: when a 5 V_{pp}, 28 kHz signal is applied, latex particles and cells are displaced.

V. SUMMARY, CONCLUSIONS AND FUTURE WORK

In this paper, we present a stimulation System-on-Chip for electro-kinetically driven microfluidic devices. This stimulation system finds application in research areas where experimentation requires particle manipulation within fluid samples: separating specific cells in body fluids, identifying pathological cells in human organs, detecting contaminants in food or water, isolating environmental pollutant agents, or manipulations at the DNA, embryo or single cell level.

The flexibility of operation allows users from different application areas to define a specific stimulation pattern by selecting signal parameters such as frequency, waveform, type, superposition, samples per cycle, time of exposure, and sequence. Table V illustrates applications where this system can be used as a stand-alone stimulation module or integrated as a core into such currently proposed devices.

To our knowledge, this is the first flexible stimulation system that delivers a variety of signal waveforms within a wide frequency range and superimposes equal or different waveforms in one signal, while allowing users to select operation parameters such as signal type, output frequencies, number of samples per cycle, and time of exposure. Our design can be used as a stand-alone stimulation module or it can be integrated into complete Lab-on-Chip systems via external bus interfaces. The 189-pin IC runs on a 190MHz clock, consuming 0.523 W during operation, small enough to be considered for portable or implantable devices.

TABLE V
PARTICLE MANIPULATION EXPERIMENTS

Ref	Stimulation	Purpose
[3]	2 sine, v1=-v2. 9.9V, ~KHz	Detect Eukaryotic cells
[4]	Sine, 8Vpp, 1MHz, V_1=-V_2	Trap-Sort DNA and proteins
[5]	100Vpp Sine, up to 200Hz. Vary phase, freq. amplitude.	Use multiple droplets and set a particle route for each particle
[6]	Stimulation within a limited frequency range	Real-time biological cell multi bio-analysis.
[7]	Up to 180Vpp, 5-500KHz, varying voltage and freq.	Manipulates contaminants, chemicals, virus, and cells.
[9]	4 Sine, sweep 1KHz-5MHz	Manipulate poly-styrene beads
[11]	+-6V, 200KHz , 2 superimposed frequencies	Separate red blood cells from lymphocytes T.
[12]	10- 20 V_{pp}, 2 superimposed frequencies: 10Kz+500 Hz,.	Separate T-cell/red blood cells
[13]	7Vrms, 30-50 KHz	Separate MD23 cancer cells
[14]	Sine, 10V, 1 MHz AC/DC.	Manipulation of pathogens
[15]	Sine, 4Vrms, 50KHz	T cells in blood, HIV diagnose

The application software is currently being tested in particle manipulation experiments on a development board, so new functionality requirements can be easily added and prototyped. In the future, we plan to tape out a chip of the proposed SoC design, which will allow us to validate final performance and achievable output frequencies.

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