A 65nm CMOS Low-Power MedRadio-band Integer-N Cascaded Phase-Locked Loop for Implantable Medical Systems

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***Abstract*—This paper presents a low-power MedRadio-band integer-N phase-locked Loop (PLL) system which is composed of two charge-pump PLLs cascade connected. The PLL provides the operation clock and local carrier signals for an implantable medical electronic system. In addition, to avoid the off-chip crystal oscillator, the 13.56 MHz Industrial, Scientific and Medical (ISM) band signal from the wireless power transmission system is adopted as the input reference signal for the PLL. Ring-based voltage controlled oscillators (VCOs) with current control units are adopted to reduce chip area and power dissipation. The proposed cascaded PLL system is designed and implemented in TSMC 65-nm CMOS technology. The measured jitter for 216.96 MHz signal is 12.23 ps and the phase noise is -65.9 dBc/Hz at 100 kHz frequency offset under 402.926 MHz carrier frequency. The measured power dissipations are 66 μW in the first PLL and 195 μW in the whole system under 1-V supply voltage. The chip area is 0.1088 mm^2 and no off-chip component is required which is suitable for the integration of the implantable medical electronic system.**

Keywords—phase-locked loop; implantable; low power; MedRadio band

I. INTRODUCTION

Recently, the research of implantable medical electronic systems has been grown rapidly to provide feasible solutions in health monitoring or disorders/diseases treatment. To improve the flexibility and stability of the implantable systems, the wireless transmission system provides an efficient way to modulate the implanted system. In 2009, the Federal Communications Commission (FCC) announced the broadened MedRadio band (401M-406 MHz) for implantable diagnostic and therapeutic purposes [1], and since then relevant work of MedRadio-band PLLs have been proposed numerous. For most implantable systems, the wireless data transceiver with PLL or frequency synthesizer is the most power consuming subsystem. Thus, reducing the PLL power is of vital importance in reducing the total required power which can results the prolonging of the battery life and reducing the risk which accompanied with the frequently surgical procedures for battery replacement. Moreover, the required operation clocks for the accurate operation are crucial for the subsystem in the implantable system such as the processor and analog-to-digital converter (ADC). Thus, fully-integrated PLLs with low power consumption and compact chip area are required.

Many low-power MedRadio-band synthesizers or PLLs have been proposed [3]-[5]. To supply a stable operation frequency, a LC VCO is utilized in [4]. Off-chip components are used in [4], [5]. These all lead to a large chip area and decrease the feasibility for the system integration. To eliminate the frequency drifting from process variation, external tuning mechanism is required to keep the frequency of the output clock signal located at the desired band which makes it disadvantageous for the integration of the implantable medical system [5], [6].

The proposed PLL is composed of two low-power integer-N PLL which are cascaded connected [7] to provide two major clocking signals. The output signal of the first PLL is used as the primary clock signal which sent to the processor to generate the required clocks for each functional block such as the ADC. The second PLL provides the MedRadio-band carrier signal for wireless signal transmission which adopts on-off-keying (OOK) modulation with sleep mode control for power management. Ring-based VCO is designed with current control unit to provide stable oscillation signal. Moreover, the reference signal of the system is provided by the power receiving coil of the power transmission system [8] to eliminate the use of the external crystal oscillator for enhancing the capability for implantable medical system integration.

The proposed PLL is designed and implemented with TSMC 65-nm CMOS technology. The PLL occupies 0.1088 mm^2 chip area without any off-chip component. The measured jitter for 216.96 MHz signal is 12.23 ps. The measured power dissipations are 66 μW in the first PLL and 195 μW in the whole system under 1-V supply voltage.

II. ARCHITECTURE AND CIRCUIT DESIGN

A. System Architecture

The system architecture of the proposed cascaded PLL is shown as Fig. 1, both PLL is implemented with charge-pump PLL which composed of a phase frequency detector (PFD), a (or two) charge pump (CP), a low-pass filter (LPF), a VCO and digital dividers. Since the proposed PLL is designed for implantable medical system, the input reference signal is designed with 13.56 MHz sinusoidal signal in the ISM band from the power receiving coil which is used for wireless

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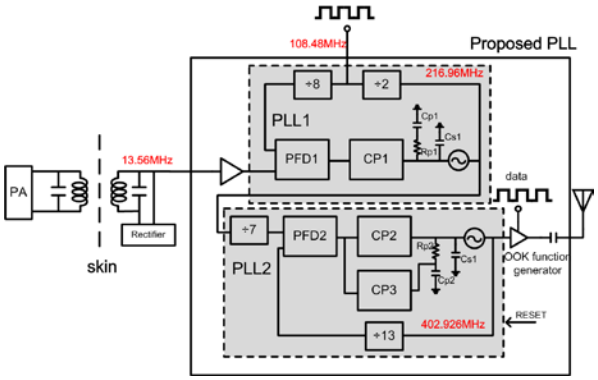

Fig. 1. The block diagram of the proposed cascaded PLL system.

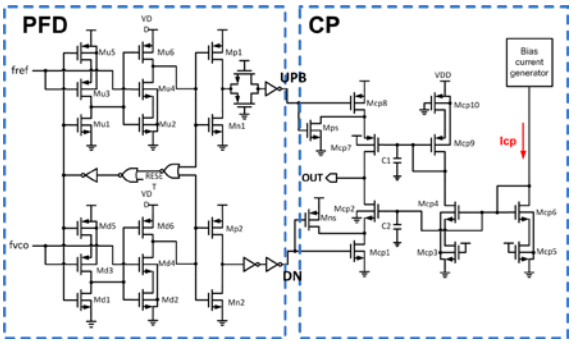

Fig. 2 . The schematic of PFD and CP.

power transmission. The first PLL (PLL1) generates a 216.96 MHz signal with the divide-by-16 unit and 13.56 MHz signal as the reference signal. With a divide-by-2 unit, a 50% duty cycle 108.48 MHz signal is generated and fed to the processor and ADC for system operation. Meanwhile, the 216.96 MHz signal is also used as the input reference signal of the second PLL (PLL2), and the PLL2 produces a 402.926 MHz MedRadio-band carrier signal for wireless data transmission.

Since the reference signal of PLL2 comes from the output of PLL1, the noise from the input is the dominate noise source. To minimize the output phase noise, the bandwidth of the PLL2 is set at low frequency to improve the input noise suppression. However, small bandwidth leads to a large capacitor in the LPF which is disadvantageous for the integration of medical device. Thus, a second charge pump (CP3) with output current designed proportional to that of CP2 is adopted in PLL2 [9]. The equivalent bandwidth, zero and the capacitor used in LPF can be lowered and the required current in the charge pump can also be reduced. To eliminate the process-variation induced affect, a current control unit is designed to obtain a stable VCO gain (K_{vco}) which can eliminate the tuning loading capacitor and hence reduce the required current in the VCO. To further minimize the power consumption of the entire system, a RESET signal is designed for power gating to turn off PLL2 when data transmission is not needed.

For noise consideration, since the output of the PLL1 will be the clock of processor and ADC in the implantable medical system, period time variation influences the accuracy of the system greatly. For an 8-channel ADC with 500k sampling rate and 11-bit resolution, the required root mean square (RMS) jitter for the 216.96 MHz signal is 29 ps. For PLL2, the phase noise requirement for communication system is

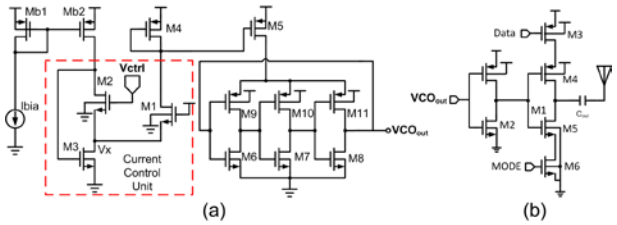

Fig. 3. The schematic of the voltage controlled oscillator.

TABLE I COMPONENT VALUES OF PLL'S LPF

PLL1		PLL2	
R_1	87.3kΩ	R_2	34.033kΩ
C_{p1}	9.12pF	C_{p2}	4.67pF
C_{s1}	0.38pF	C_{s2}	3.11pF

important. In the proposed OOK communication system, the required phase noise at 100 kHz offset from the carrier signal of frequency at 402.926 MHz is about -64.8 dBc/Hz [3].

B. PFD , Charge Pump, and Low-Pass Filter

The PFD detects the phase difference between reference signal and feedback signal and provides response at the output as shown in Fig. 2. The PFD consists of two true single-phase-clock (TSPC) D flip-flops [2] to detect the rising edges of the input signals and contains a feedback path with a delay time to provide a reset signal when both flip-flops are triggered. The outputs of the D flip-flops act as the control signals UPB and DN for the CP. The propagation delays between the two output paths of D flip-flops to CP are compensated by inserting a transmission gate. The source-switching topology is adopted to eliminate the leakage current by Mns and Mps which can avoid the charge sharing effect between the parasitic capacitors and the LPF by bypassing the charges at the drains of Mcp1 and Mcp8 respectively [3].

The charge pump reflects the UP and DN to charge or discharge the LPF. The charging (or discharging) time is decided by the phase error between the input reference signal and the output feedback signal. A second CP (CP3) is adopted in PLL2 to reduce the effective loop bandwidth of PLL2. The output current is -0.9 times of CP2. This will reduce the zero, bandwidth of PLL2 and the C_{p2} in LPF [9]. A second order LPF is used as the loop filter in the proposed PLL system. The parameters of the LPF set the loop bandwidth and hence determine the performance of the system such as the noise and the stability. The parameters of each LPF are shown in Table I.

C. VCO and OOK Function Generator

Fig. 3(a) shows the schematic of 3-stage ring-based oscillator which is used in both PLL. M6-M11 are utilized as the inverter chain for oscillating. To eliminate the process-variation induced frequency drifting, a current control unit composed of M1-M3 is designed to convert the input control voltage to the current which the oscillator's output frequency is directly proportional to. When control voltage (V_{ctrl}) is fed from loop filter, Vx in Fig 3 can be shown as (1) :

$$V_x = V_{ctrl} - V_{th} - \sqrt{\frac{2I_{bia}}{\beta_{M2}}} \qquad (1)$$

where I_{bia} is the constant bias current of the VCO $\beta = \mu C_{ox} W/L$, μ, C_{ox}, W, L, and V_{th} are the mobility, gate

capacitance density, width, length and threshold voltage of the MOS device, respectively. Since the bias current is a constant value, the Vx changes with V_{ctrl}. Thus, the current feeding to the inverter chain can be expressed as (2):

$$I = \frac{1}{2}\beta_{M1}(V_{dd} - V_{ctrl} + \sqrt{\frac{2I_{bia}}{\beta_{M2}}})^2 \quad (2)$$

It can been seen from (2) that the current is not sensitive to V_{th} which can reduces the variation of the required V_{ctrl} and hence avoids the mismatch current produced by M_{cp2} and M_{cp7} in CP that caused by short-channel effect.

The tranconductance (GM) and K_{vco} of the VCO can be expressed as:

$$Gm = \frac{d_I}{d_{vctrl}} = \beta_{M1}(V_{dd} - V_{ctrl} + \sqrt{\frac{2I_{bia}}{\beta_{M2}}}) \quad (3)$$

$$K_{vco} = \frac{d_{FREQ}}{d_{vctrl}} = \frac{Gm}{NC_{par}V_{sw}} \quad (4)$$

where the N is stage number of the inverter chain, C_{par} is the parasitic capacitance of the inverter chain and the V_{sw} is the signal swing of VCO's output. It can be seen from (3) and (4), the GM and K_{vco} will not be affected by the variation of V_{th}, hence fix the loop bandwidth and remain the noise performance satisfy the designed condition.

Fig. 3(b) shows the schematic of the OOK function generator that composed of an output buffer and modulated by the transmission data. The mode control signal (MODE) is designed to turn off the OOK function generator when data transmission is off.

D. Digital Frequency Divider

4 divide-by-2 frequency dividers are connected in series to implement the function of divide-by-16 in PLL1. The first three frequency divider adopts the TSPC topology D flip-flops. Without static currents and less number of transistors, the power dissipation can be reduced. The last divide-by-2 frequency divider is designed with static CMOS D flip-flops for reducing leakage power. For PLL2, the digital counters based on resettable D-flip-flops are served as 7-times and 13-times frequency divider.

III. EXPERIMENTAL RESULTS

The proposed PLL system chip is fabricated by using 65-nm 1P6M CMOS technology which occupied 0.1088 mm^2 chip area and the chip photomicrograph is shown in Fig. 4. With the signal coming from the signal generator adopted as the reference signal, a 50% duty cycle 108.48 MHz signal can be generated by PLL1 and its RMS jitter is 17.29 ps which can be transferred to 12.23 ps RMS jitter for the 216.96 MHz signal as shown in Fig.5. Fig. 6 shows the output spectrum of the PLL2. The peak power of the TX output is around -25.145dBm at 403 MHz which is smaller than the MedRadio Band requirement of -16 dBm. Fig. 7 shows the measured phase noise of the PLL2 output. At 100-kHz frequency offsets, the phase noise is -65.9 dBc/Hz. The experimental result above can prove that both PLL can work very well to

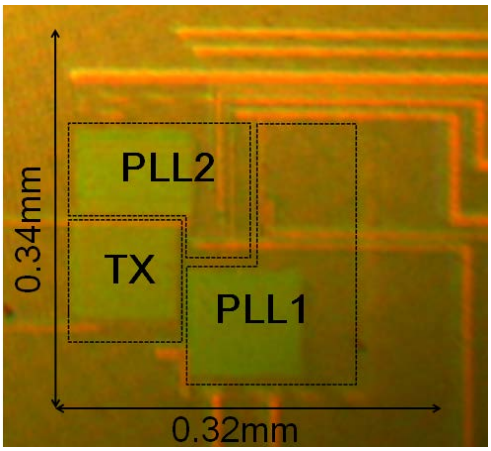

Fig.4. Chip photomicrograph of the proposed PLL.

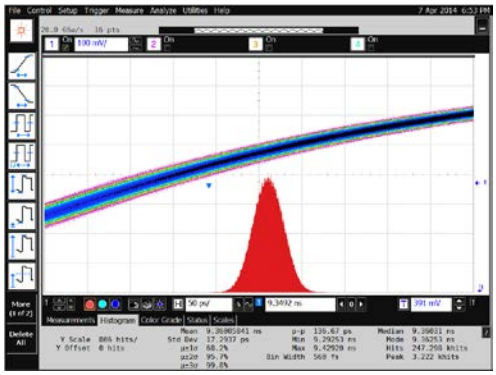
Fig. 5. Jitter measurement of PLL1 with clock generator input.

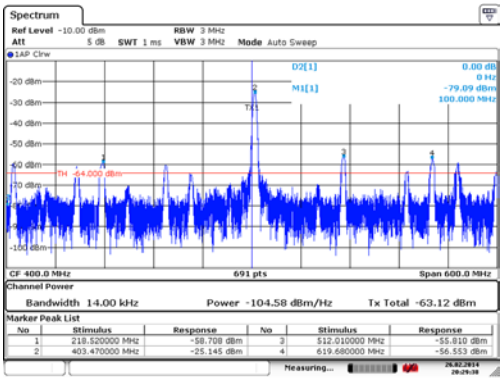

Fig. 6. Measured output spectrum of the PLL2.

provide the correct frequency signal and satisfy the system requirement. When the input reference signal of the proposed PLL system is coming from the power transmission coil, as shown in Fig. 8, the measured RMS jitter of 108.48 MHz signal is 42.30 ps, which means the equivalent RMS jitter of 216.96 MHz signal is 29.91 ps as shown in Fig.9. When all the blocks of two PLL are turned on, the power consumption is 195 μW (excluding the OOK function generator). If the PLL2 is turned off by the power gating reset signal, the system's power consumption is reduced to 66 μW.

Table II summarizes the performance of the proposed PLL and the comparison with state-of-the-art reported PLLs. As may be seen from Table II, the proposed cascaded PLL consumes lower power dissipation with smaller chip area without crystal oscillator and external components.

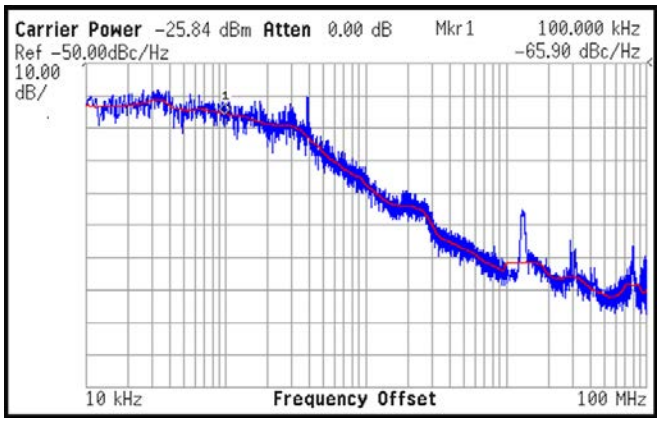

Fig. 7. Measured phase noise of the output of PLL2.

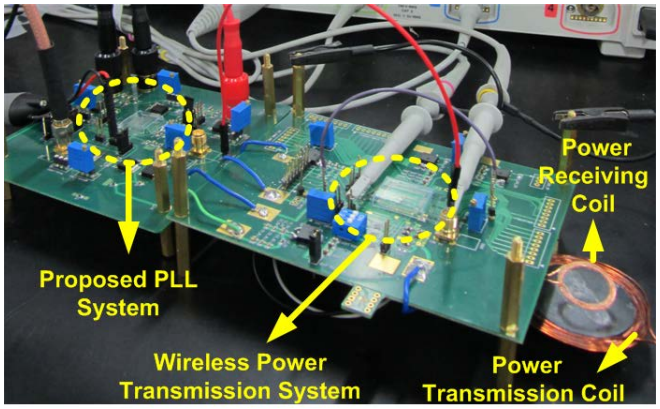

Fig. 8. The experimental setup with the input reference signal coming from the coils.(Shielding is removed to reveal the coils.)

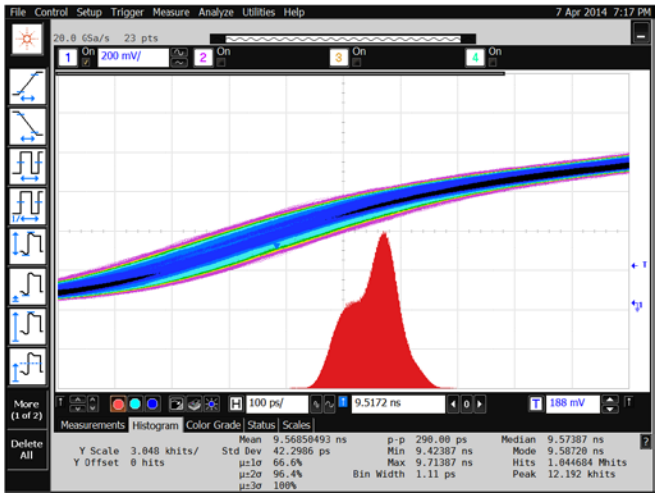

Fig.9. Jitter measurement of PLL1 with coil input

IV. CONCLUSION

A low-power MedRadio-band integer-N cascaded PLL system for the implantable medical electronic system has been designed, fabricated, and measured in 65-nm CMOS technology. In the proposed PLL, the cascaded structure is adopted with the ring-oscillator VCO utilizing current control unit to enhance the stability of the oscillating frequency without crystal oscillator and external RC components. The experimental results show that the proposed PLL system can work well and generate required clock and carrier signal without any off-chip component that satisfied the required specification for system operation and provide a promising solution for the integration of a medical electronic system.

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TABLE II PERFORMANCE SUMMARY AND COMPARISON WITH THE REPORTED PLLS

Parameters	This work	2013 BioCAS [3]	2012 TBCAS [4]	2012 JSSC [5]	2010 RFIC [6]
Type	Clock Generator	Clock Generator	Frequency Synthesizer	Frequency Synthesizer	Frequency Synthesizer
Operating Frequency	402.926MHz	402.92 MHz	400.8-405 MHz	400-433MHz	400-410MHz
Technology	65nm	0.18um	65nm	130nm	0.18um
Reference frequency	13.56MHz	13.56MHz	300kHz	1.8432MHz	10MHz
Supply	1V	1.8V	1V	0.5V	1.8V
Current	66μA (PLL1) 195μA (System)	256μA	430μA	880μA	700μA
Spur level	-30dBc	-32dBc	-45dBc	-38.3dBc	-55dBc
Phase noise	-65.9dBc/Hz @100kHz ; -65.1dBc/Hz @100kHz*	-79dBc/Hz @100kHz	-102.1dBc/Hz @200kHz	-91.5dBc/Hz @1MHz	-83.6dBc/Hz @300kHz
VCO type	RING	RING	LC	RING	RING
Area (excluding PAD)	0.1088 mm^2	0.192 mm^2	0.54 mm^2	0.072 mm^2	0.14 mm^2
Input reference	Coil	Coil	MEMS	Crystal	Crystal
Off chip component	NO	NO	NO	YES	NO

* Reference signal from coil.

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