CMOS-Based High-Speed Nanopore Recording: Signals and Systems

Sebastian Magierowski, Syed Zahidul Islam, Yiyun Huang, and Ebrahim Ghafar-Zadeh

***Abstract*— This paper considers the potential of CMOS-based nanopore measurement systems for high-speed molecular recording and DNA sequencing in particular. As such it approximates the signal fidelity limitations of a CMOS-based nanopore readout channel and discusses the means by which throughput could be increased through the use of a parallel CMOS readout system.**

I. INTRODUCTION

A convergence between CMOS microelectronic and nanopore technologies has been underway for the last few years. It has led to a miniaturization of the nanopore apparatus that brings benefits beyond the obvious footprint reduction. Concrete accomplishments include the demonstration of improved sensitivity [1] and functionality [2] through the use of CMOS amplifiers. Others have built nanopores directly in CMOS substrates [3] with the hope of leveraging such benefits even more profoundly, mainly to increase the sensitivity and the processing speed of these sensors. The latter point not only refers to the rate achievable per sensor, but the throughput advantage that can be attained if the integration advantages of CMOS technology can be adequately exploited.

In this paper (§ II) we employ simple nanopore signal models and note reported device and circuit performance levels to approximate the rate at which CMOS-based nanopore DNA sequencing systems with varying degrees of fidelity (i.e. ability to resolve alternate molecular events) can operate. We then (§ III) explore parallel nanopore-CMOS systems options to boost measurement throughput and conclude with a proposal for a CMOS-based nanopore readout array.

II. NANOPORE SIGNALS

In this section we consider the general qualities of nanopore induced signals and the degree to which they can be adequately processed by the front-end electronics that forward them for digital capture. This analysis leads to an approximation of the rates that a single nanopore-CMOS channel employed for DNA sequencing can be reasonably expected to achieve.

A. Signal Speeds

A nanopore system's front-end CMOS is tasked with amplifying ionic currents in the pico/nanoampere range that roughly assume the characteristics of a multilevel random telegrapher signal (RTS). Excluding DC, the double-sided power spectral density of such a signal is expressed as

$$S_s(f) = \frac{I_{avg}^2 v_t}{(2\pi f)^2 + (2v_t)^2}, \quad f \neq 0 \tag{1}$$

where v_t denotes the average translocation velocity of molecular entities through the nanopore and I_{avg} denotes the average current deviation from the DC baseline, I_{dc}, flowing through the pore. From the integral of this expression over f the measurement bandwidth necessary to capture sufficient signal energies can be derived.

In the context of DNA sequencing, the translocation velocity refers to the rate at which nucleotides (nt) pass through the nanopore and hence the rate at which they induce measured signal variations. Viewed more generally, the translocation velocity can be imagined as a record of structural and positional variations ("events") experienced by a monomer as it progresses through the nanopore. The dynamics of these processes may advance at rates several times higher than the average movement of the nucleotide itself. Still, from the hardware perspective, the perturbations invoked by these dynamics can ultimately be abstracted to some ionic current level and temporal duration, the identification of which is left to the measurement system's downstream digital analysis tools. For simplicity we will denote v_t in terms of nt/ms units.

B. Signal Fidelity Requirements

Even though a measurement system may have the necessary bandwidth to process the signal without attenuation it invariably corrupts it with noise. This, in turn, compromises its ability to associate current pulses with the correct translocation event. Corruption is to be expected in any practical measurement system, but what is an acceptable level? Commercial DNA sequencing methods can be of some guidance here with error rates ranging from roughly 5×10^{-4} (Life Tech. SOLiD) to 10^{-1} (PacBio RS) [4].

The probability of incorrectly deciphering the current value in a multi-level signal such as measured by a nanopore can be approximated with [5]

$$P_e \approx 2Q(\sqrt{SNR}) \tag{2}$$

where SNR refers to the ratio of signal energy to noise energy over some observation period. A plot of this relation is shown in Fig. 1. From this relation it can be seen that in order to achieve performance levels on par with contemporary sequencing technologies the pore's SNR should be between 4 and 11 dB.

The authors are with the Department of Electrical Engineering and Computer Science, Lassonde School of Engineering, York University, 4700 Keele St, Toronto, Canada magiero@cse.yorku.ca

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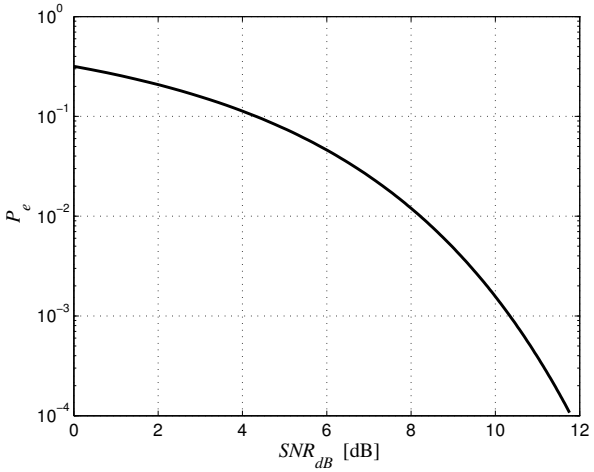

Fig. 1. Error-rate as a function of measurement SNR.

Generally speaking the SNR of a measurement system can be expressed as the ratio of the energy difference between signals to be distinguished and the noise energy present over the course of a measurement. A simplistic and straightforward detection metric determines the measured signal level by integrating over a characteristic period. Since the signal is constant over such time while the noise is random a boost between signal and noise can be expected.

For nanopore events this integration time can be some fraction of inverse event velocity, kv_t^{-1} where $0 < k \leq 1$. Assuming a minimum difference of i_δ between the ion currents generated by different events we obtain

$$\sqrt{SNR} = \frac{i_\delta}{2i_{n,rms}}\sqrt{\frac{kB_m}{v_t}} \tag{3}$$

where B_m is the measurement bandwidth needed for a given v_t. The noise current present in the system is represented by $i_{n,rms}$, its root mean square value over the measurement bandwidth. We now turn to considerations of this noise term.

C. System Noise

With an SNR goal identified above we can consider the system noise characteristics that are required for a nanopore measurement apparatus working over a variety of v_t. In general this apparatus conforms to a standard approach that involves amplifying the signal over a number of stages until it is ready for digitization. As with all signal-processing chains the first amplifier stage is of significant influence because in a soundly designed system it has the largest impact on overall noise behaviour.

In nanopore systems the preamplifier typically takes on a transimpedance form with the intention of converting the small input current signal into the voltage domain. A large number of potential noise contributors have been identified within this signal chain by researchers [6], [7], [8]. These include the commonly encountered thermal, shot, and flicker mechanisms along with the potential for dielectric loss contributions and, most importantly for systems aspiring to high-speed operation, the attenuating affect of the capacitance present at the preamplifier's input.

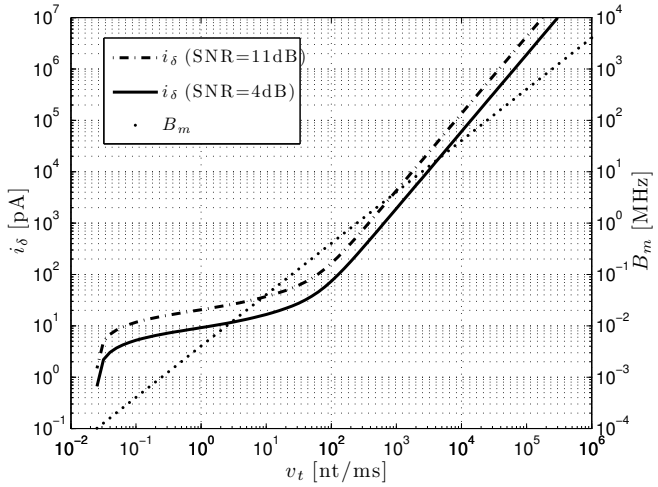

Fig. 2. The requisite measured event level spacing, i_δ, to achieve between 10% (4-dB SNR) to 0.05% (11-dB SNR) detection error.

A simplified expression for the input-referred current noise spectral density of a nanopore measurement system is

$$\overline{i_n^2} = \overline{i_f^2} + \overline{i_s^2} + \overline{i_a^2} \tag{4}$$

where $\overline{i_f^2}$ refers to the flicker noise contributions from the sensor, $\overline{i_s^2}$ refers to the shot noise contribution from a continuous-time offset cancelling mechanism [9] and $\overline{i_a^2}$ refers to the capacitance enhanced noise mentioned above. Expressions for these components take on the form: $\overline{i_f^2} = AI_{dc}^2/f$, $\overline{i_s^2} = 2qI_{dc}$, and, $\overline{i_a^2} = \overline{e_a^2}C_T^2(2\pi f)^2$.

How large a signal current do we need to maintain SNR's of 4–11 dB at different frequencies? Fig. 2. Combines the noise expressions above with (3) to plot i_δ as a function of the translocation velocity, v_t. This curve is derived assuming a normalized Hooge's parameter of $A = 3 \times 10^{-7}$, a quiescent current of $I_{dc} = 5$ nA (not uncommon in solid-state nanopore [10]), a preamplifier input referred noise voltage of $\overline{e_a^2} = 5.5$ nV/$\sqrt{\text{Hz}}$ and a net input capacitance of $C_T = 7.4$ pF (as reported in [1]).

For example, given current technology, our approximations suggest that measurements requiring event speeds of 100 nt/ms and employing a simple detection scheme need $B_m \approx 400$-kHz and a $i_\delta \approx 75$-pA current level split between events to achieve an SNR of 4-dB. An 11-dB SNR requires 165-pA separations.

To put this example in perspective, studies of biological nanopores have shown a current separation on the order of $0.03I_{dc}$ with a range of $0.2I_{dc}$ between minimum and maximum where I_{dc} is the open pore dc current [11]. With biological nanopores conducting I_{dc} 100 pA the ability to discern different sequences requires the resolution of signals roughly 5 pA apart if uniformly spaced levels unique to a single nucleotide can be excited.

More realistically, in the near-term read levels will likely depend on 3 to 4-long nucleotide sequences. This will require the reader to discern 64 to 256 levels and hence a signal resolution of < 0.3-pA. Such a system would be able to

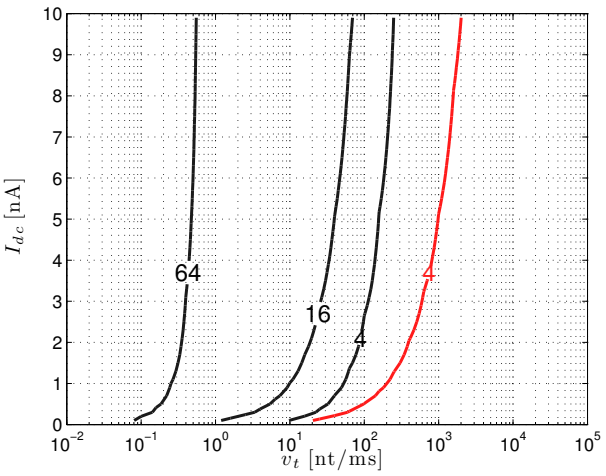

Fig. 3. Contour plot of $0.1I_{dc}/i_\delta$ needed to achieve 4-dB SNR. The black curves assume the noise settings noted above, while the red curve ignores the effect of capacitance-induced noise.

support event speeds (events now being the result of several nucleotides) of roughly 0.25 nt/ms with a measurement bandwidth of 1-kHz.

Solid-state nanopores offer the ability to operate at higher bias levels than their biological counterparts as well as possessing higher conductance levels. This promises deeper current-level excursions in response to individual translocation events, although recent reports describe a range of about $0.1I_{dc}$ between minimum and maximum [10].

The contour plots in Fig. 3 indicate the fraction of a $0.1I_{dc}$ level span required by i_δ to achieve a 4-dB SNR as a function of v_t and I_{dc}. The black lines correspond to results obtained for the noise and amplifier values noted earlier. They indicate that in order to resolve 4 levels within a range of $0.1I_{dc}$ (i.e. $0.1I_{dc}/i_\delta = 4$) at 4-dB SNR a maximum rate of less than 300 nt/ms can be supported. Obviously the maximum achievable rate is diminished as the number of individual events we seek increases. Specifically, our translocation rate drops to 0.5 nt/ms, a measurement bandwidth of 2-kHz, for $0.1I_{dc}/i_\delta = 64$.

Finding a means to eliminate the high frequency noise contribution can help propel operation to even higher velocities. The red contour in Fig. 3 tracks $0.1I_{dc}/i_\delta = 4$ under the idealistic condition where this noise source has been completely eliminated. Although this has the potential to reach translocation seeds up to 2000 nt/ms its advantage is largely lost (not shown in Fig. 3) for 16 and 64 level signalling.

Thus, under the assumptions marshalled in this paper, noise, predominantly the shot noise, has accumulated sufficiently at the lower frequencies to prevent substantial improvement in nanopore resolution even as the signal levels, i_δ, expand with increased quiescent current, I_{dc}. In short, where capacitance-based noise prevents our ability to discern coarse levels at high event rates, the shot noise interferes with our ability to distinguish large numbers of levels at lower event rates.

III. PARALLEL SYSTEMS

A. Performance Targets

A means of system speed-up complementary to increased bandwidth is naturally one that employs multiple sensors operating in parallel. This is a role that CMOS is certainly quite suited to. It has already been leveraged for DNA base calling in the form of a charge detector, the "ion chip", used as part of a sequencing-by-synthesis procedure [12]. Recent ion chip reports describe its realization in a 110-nm CMOS technology with a sensing-channel density of roughly 1.5-μm^{-2} [13] and a total of 660 million sensors on a die roughly 25 mm on a side. This technology exhibits a speed of roughly 3×10^{-7} nt/ms per sensor [12] assuming a ten-fold coverage and a 2-hour processing time. With 660M sensors operating in parallel this results in an equivalent event throughput of about 200-nt/ms. Of course this result does not account for sample preparation time as well as the ensuing bioinformatics effort.

To achieve a similar result a nanopore based system intended to discern 64-different patterns, but limited to the noise characteristics outlined above (contour-value 64 in Fig. 3) would require 360 parallel readout circuits. If 16 patterns were discerned only 3 units would be needed.

B. Multichannel CMOS Architectures

A fully parallel nanopore chip is certainly within the realm of possibility. Assuming a 750 μm pitch, a dimension already shown sufficient for a nanopore electrode and pre-amplification circuitry in a 130-nm CMOS technology [1], 360 channels could be realized on a die spanning about 14 mm per side. Of course the need to connect 360 pinouts to an ensuing chip presents a formidable challenge, especially in a low-noise scenario and as event speeds increase.

It is likely that as the system scales a means of serializing signals onto a lower number of lines will be needed. This is most convenient once the data has been digitized. Of course in the extreme case this requires each channel to employ not only pre-amplification, but filtering and data converter circuitry as well. Although this is certainly within the capacity of today's CMOS technology, managing the heat induced by the added circuitry operating in parallel may present another complication for biological recordings.

In anticipation of the issues just noted, it is tempting to consider a readout arrangement similar to that employed in the ion chip architecture [14], whereby on-chip *trans* electrodes, each isolated in an individual SU-8 chamber, are organized in a row/column array. Each electrode in the array could then be polled in some fashion through the activation of switches between itself and following signal processing blocks. The switches themselves would be under the control of row and column decoders.

Unlike the ISFET sensors employed by the ion chip, a nanopore recorder processes signals about 5 orders of magnitude weaker with time signatures about 5 orders of magnitude smaller. Hence, an arrayed system with component access mediated by transmission-gate switching is

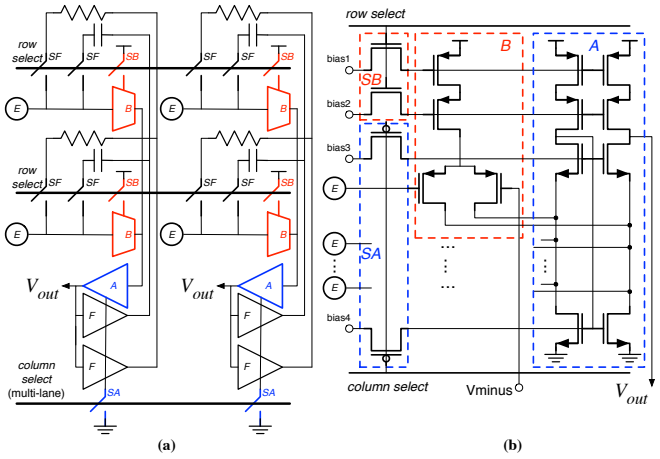

Fig. 4. (a) An active parallel nanopore readout system with buffer (B), amplifier (A), and feedback amplifiers (F) and (b) a CMOS schematic representation of a parallel nanopore readout system: a folded cascode amplifier partitioned into column/row segments.

unlikely to provide satisfactory performance levels at large scales. For example a 130-nm NMOS switch can achieve a per unit width $R_{on} \approx 650\ \Omega \cdot \mu$m (including parasitic source/drain resistance loss) and an $R_{off} \approx 1\ \text{G}\Omega \cdot \mu$m at $V_{ds} = 500$ mV assuming a 100-mV/V drain-induced-barrier-lowering (DIBL) parameter. With solid-state nanopore resistances varying between roughly 100 MΩ and 350 MΩ during operation the NMOS switch would pass its intended signal sufficiently, but in the OFF state would have trouble effectively blocking disturbances from neighbouring nanopores.

A compromise arrangement is presented in Fig. 4(a). Instead of directly interfacing transistor switches to electrodes (E) this complex multiplexes over buffer circuits (B) that form the first stage of an op-amp completed by A. As shown in Fig. 4(a) the switches (SA, SB, SF) only engage with the signal processing components and thus are prevented from appearing in series with the signal path. In particular, SB, are used to activate the buffers using a *row select* signal while, SA, are activated by a *column select* signal to turn on any one buffer's ensuing amplification complement, A. The column output voltage signal, V_{out}, can then be digitized and forwarded to an appropriate detection element. AC feedback via an integrating capacitance as well as DC corrective feedback via a (active) resistance is facilitated by more amplifiers, F. These connections can be facilitated by yet another bank of switch components SF.

A simplified CMOS circuit level arrangement of the architecture illustrated in Fig. 4(a) is shown in Fig. 4(b). Due to space limitations only one instance of B and A are shown and the feedback components are not detailed. Together, B and A constitute a folded-cascode amplifier. The *row select* signal manages the activation of B's (and partly A's) bias circuitry via SB which pass the potentials "bias1" and "bias2". The *column select* completes the amplifier activation via SA which pass potentials "bias3" and "bias4" to A. The low-impedance nature of the link between A and B helps mitigate the growing output capacitance as the number of rows (and hence the number of Bs) increases.

IV. SUMMARY

CMOS-based nanopore signal and system characteristics were subject to an approximate analysis in this paper. A firmer footing between nanopore measurement bandwidth requirements and translocation velocity was proposed based on an RTS model. By invoking a measurement error model referenced to contemporary DNA sequencing technology it was noted that an SNR goal of 4 to 11-dB would serve as a competitive target. This result was used to derive the required ionic current levels which were used to approximate the maximum speed of nanopore systems. A system capable of discerning 64 levels was approximated to be limited to a speed of 0.5 nt/ms given current sensor and CMOS electronic performance levels.

A parallel readout system was then discussed as a complementary means of boosting nanopore measurement throughput. The number of channels needed to match emerging DNA sequencing technology was approximated followed by a proposal for an arrayed nanopore system with distributed amplification.

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