Real-Time Processing of Fast-Scan Cyclic Voltammetry (FSCV) Data Using a Field-Programmable Gate Array (FPGA)

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***Abstract*—This paper reports the hardware implementation of a digital signal processing (DSP) unit for real-time processing of data obtained by fast-scan cyclic voltammetry (FSCV) at a carbon-fiber microelectrode (CFM), an electrochemical transduction technique for high-resolution monitoring of brain neurochemistry. Implemented on a field-programmable gate array (FPGA), the DSP unit comprises a decimation filter and an embedded processor to process the oversampled FSCV data and obtain in real time a temporal profile of concentration variation along with a chemical signature to identify the target neurotransmitter. Interfaced with an integrated, FSCV-sensing front-end, the DSP unit can successfully process FSCV data obtained by bolus injection of dopamine in a flow cell as well as electrically evoked, transient dopamine release in the dorsal striatum of an anesthetized rat.**

I. Introduction

Fast-scan cyclic voltammetry (FSCV) at a carbon-fiber microelectrode (CFM) is recognized as the preferred choice for real-time monitoring of endogenous neurotransmitters in behaving animals due to its exquisite temporal, spatial and chemical resolution [1]. Indeed, this measurement modality provided the first monitoring of any neurotransmitter with subsecond temporal resolution at a brain-implanted, micron-sized probe in an awake, freely behaving animal [2]. Great strides have also been made in developing CMOS integrated circuits (ICs) that monitor neurochemistry [3], [4], and one recent example has even extended the sensing-only functionality to the realm of high-fidelity, dynamic control of neurochemistry [5], paving the way for developing new neuromodulation devices that can impose therapeutic neurochemical profiles or maintain optimal neurochemical levels in disease states via real-time feedback control.

Basic processing of FSCV data to obtain a temporal profile of concentration variation and a chemical signature to identify the target analyte has traditionally been performed offline on a home-base computer post-data acquisition. To usher in the next-generation, closed-loop devices that feature combined sensing, computation and control functions for long-term, autonomous operation, FSCV data processing needs to be performed in real time (i.e., as the recording is taking place) to alleviate a need for the home-base computer.

In this paper, we propose a digital signal processing (DSP) unit for real-time processing of FSCV-based dopamine data. Our test analyte, dopamine, underlies cognition and motivation, and is intimately involved in the neuropathologies of Parkinson's disease and drug abuse [6]. The DSP unit is realized in hardware using a field-programmable gate array (FPGA) and interfaced with an integrated, FSCV-sensing front-end that has previously been developed [5]. The functionality of the DSP unit is successfully evaluated via *in vitro* (i.e., flow injection analysis, FIA) and *in vivo* biological experiments with anesthetized rats, paving the way for ultimately implementing it on a custom IC.

The paper is organized as follows. Section II describes the fundamentals of dopamine sensing with FSCV at a CFM. Section III presents the DSP unit architecture and its FPGA realization. Section IV presents our measured results, and Section V draws some conclusions from this work.

II. Fundamentals of FSCV-Based Dopamine Sensing

FSCV at a CFM for dopamine sensing is shown in Fig. 1. Typically, the CFM potential is linearly swept every 100ms by a triangle wave between a resting potential of -400mV and a peak voltage of 1.3V at a rate of 400V/s, resulting in scan duration of 8.5ms. During the positive sweep, dopamine is oxidized (by losing two electrons) to dopamine-ortho-quinone, which is reduced back to dopamine (by gaining two electrons) during the negative sweep. The current resulting from this electrochemical reaction includes both background and faradaic components. Panel A shows a current recording obtained in an *in vitro* experiment with a CFM positioned in the inlet of a flow cell reservoir. The solid black line depicts the background current obtained in one triangular FSCV scan prior to any bolus injection of dopamine into the flow cell. The dashed red line shows the measured total current (i.e., background + faradaic currents) obtained in another FSCV scan after a 5-second bolus injection of dopamine.

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Since the background current is typically stable over a short period of time, it can be subtracted from the total current to reveal the faradaic current, which is the one proportional to dopamine concentration, as depicted in Panel B. The faradaic current when plotted against the CFM potential creates the background-subtracted cyclic voltammogram, which is used as a chemical signature to identify the analyte as shown by Panel C where the oxidation and reduction peaks at +0.57V and -0.2V, respectively, indicate dopamine. Dynamic information, indicative of the temporal pattern of concentration changes, is obtained by plotting peak dopamine current measured at dopamine oxidation potential in each voltammogram *vs.* time for multiple successive FSCV scans. This is shown in Panel D where each data point (indicated by a dot) represents the peak dopamine current from one voltammogram every 100ms (a total of 200 voltammograms in 20 seconds with FSCV at 10Hz).

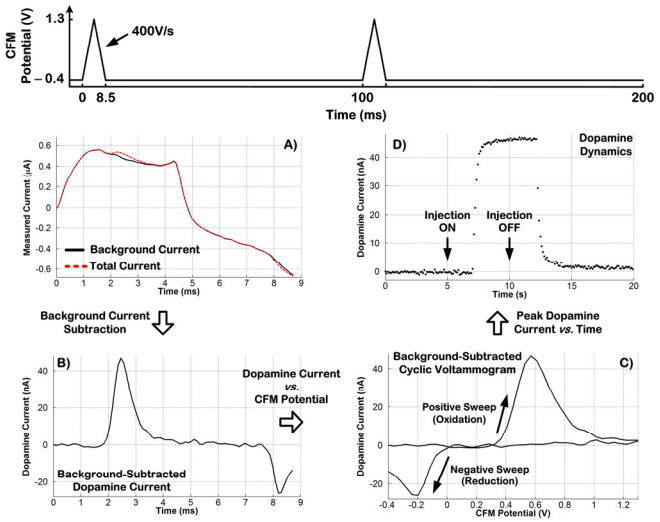

Fig. 1. Fundamentals of fast-scan cyclic voltammetry (FSCV) at a carbon-fiber microelectrode (CFM) for dopamine sensing.

III. FPGA Implementation of FSCV Data Processing

Fig. 2 depicts the architecture and timing operation of the system developed for real-time processing of FSCV data, comprising an integrated, sensing front-end interfaced with a CFM working electrode (WE) and a DSP unit implemented on an FPGA, which is the focus of this paper. The FSCV-sensing front-end integrates a waveform generator and a 3rd-order, continuous-time, ΔΣ modulator (ΔΣM) with an oversampling ratio (OSR) of 64 clocked at 625kHz with single-bit quantization [5]. Due to the use of oversampling in the ΔΣM, the DSP unit incorporates a decimation filter to remove the out-of-band noise and convert the low-resolution (1b), oversampled, digital data at the output of the FSCV-sensing front-end to high-resolution (14b), decimated data.

The decimation filter is followed by an FSCV processor for real-time processing of the sensed current to compute the averaged background current (*Avg Bckgnd*), background-subtracted, faradaic current (*Bckgnd Sub*) and peak oxidation current (*Peak Ox*) in each FSCV scan. These data along with the decimated ones are serially sent out using the onboard data framing and serializer block. The DSP unit also incorporates an internal memory to upload decimation filter coefficients and FSCV processor parameters via the programming interface prior to the actual experiment.

The timing operation of the system is controlled by the timing control (*TC*) signal generated by the FSCV waveform generator of the sensing front-end. Specifically, when the *TC* signal goes high, the ΔΣM is activated, the FSCV waveform is applied to the CFM WE after a delay of 2.3ms and FSCV sensing is subsequently performed for 8.5ms. The DSP unit is also concurrently enabled for real-time FSCV processing. The peak dopamine oxidation current (*Peak Ox*) is computed by the time the *TC* signal goes low and remains valid until the next FSCV cycle. The design of the decimation filter and FSCV processor as the main building blocks of the DSP unit is described in more detail below.

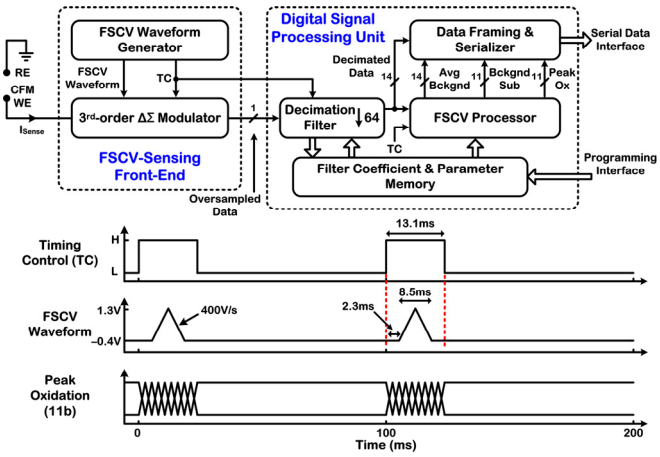

Fig. 2. Architecture and timing operation of the proposed DSP unit for real-time processing of the FSCV data.

A. Decimation Filter

Fig. 3 depicts the schematic block diagram of the decimation filter of the DSP unit realized using three lowpass filter stages. A cascaded integrator-comb (CIC) filter is used for the first stage to decimate the ΔΣM output by a factor of 16 (i.e., to 4× the Nyquist rate) requiring no multiplication. For a 3rd-order ΔΣM, a 4th-order CIC filter is needed to adequately attenuate the noise that would otherwise alias into the desired signal band [7]. The CIC filter is implemented with two's complement, wrap-around arithmetic and with 17b word-length for internal registers to minimize the effects of overflow in the integrator stages [8].

Following the CIC filter, a cascade of half-band (HB) and finite impulse response (FIR) filter stages is used to down-sample the data further by a factor of 4 to a decimated rate of ~9.77kHz. An HB filter is a subset of the FIR filter family, in which all odd coefficients are equal to zero except for the center one, resulting in fewer taps, less hardware resources and hence low power consumption. An 18th-order, HB-FIR filter is used to adequately suppress noise aliasing

into the desired signal band. Finally, a 50th-order, FIR filter is used as the third stage, targeting a transition band centered at ~3kHz for the decimation filter to limit the bandwidth and further reduce noise. Each of the two FIR filters uses only one multiplier for efficient use of the available hardware. To increase the arithmetic precision in the two FIR filters, the word-length of the internal nodes is increased to 20b. The filter coefficients are quantized with 18b and stored in the internal memory of the DSP unit, and a finite-state machine is used to update the memory address of the coefficients required for each multiplication. Since the front-end ΔΣM features a dynamic range of 80.8dB in an input current range of ±1.2μA (i.e., ~13b-resolution) [5], the output word-length is converted to 14b, with an extra bit for sign information. Table I tabulates the overall decimation filter specifications.

B. FSCV Processor

Fig. 4 shows the schematic block diagram and operation timing of the FSCV processor in the DSP unit, incorporating functional blocks for background current averaging, background current subtraction and moving average, as well as peak oxidation current detection. The *TC* signal is high for 13.1ms [5], during which 127 samples of decimated data are generated at the rate of 9.77kHz. The first 31 samples in each FSCV scan are discarded due to the decimation filter delay (~2ms) and the 2.3-ms delay from the rising edge of the *TC* signal to the start of FSCV waveform (see Fig. 2).

The background current-averaging block calculates and stores a stable, averaged background current (*Avg Bckgnd*) for the purpose of subsequent subtraction. Upon receiving a *Reset* signal, *Avg Stat* goes low and, depending on the user-set *Avg Mode1* parameter (2b), background currents of 4, 8 or 16 consecutive FSCV scans are added and stored in an internal memory of 96 × 18b. Next, *Avg Stat* goes high in the subsequent FSCV cycle, and the averaged background current associated with each timestamp, $AB_{1\sim96}$, is generated by dividing the memory content for that timestamp by 4, 8 or 16. *Avg Stat* remains high and the memory content does not change until the next *Reset* signal arrives, indicating that the user wants to update the averaged background current.

When *Avg Stat* goes high, the background current subtraction/moving average block is also activated. Upon receiving the decimated data $D_{32\sim127}$, the averaged background current associated with the corresponding timestamp, $AB_{1\sim96}$, is subtracted from it, and the resulting background-subtracted, faradaic current, *Bckgnd Sub*, is converted to 11b data. Next, depending on the user-set *Avg Mode2* parameter (2b), the background-subtracted current of each timestamp, $BS_{1\sim96}$, of the present FSCV scan is averaged with those of the 0, 1, or 3 previous FSCV scans to smooth the response. Three internal memories of 96 × 11b are used to store up to 3 previous background-subtracted, faradaic current data for the moving average function.

Sub Stat goes high at the start of FSCV cycle when *Bckgnd Sub* becomes ready and remains high until the next *Reset* signal from the user. With *Sub Stat* high, the peak oxidation current detection block is enabled to find *Peak Ox*

Fig. 3. Schematic block diagram of the decimation filter in the DSP unit.

TABLE I
DECIMATION FILTER SPECIFICATIONS

Decimation Factor	64×
Input Sampling Rate	625kHz
Output Sampling Rate	9.77kHz
3-dB Bandwidth	2.7kHz
Passband Ripple	< 0.006dB
Stopband	3.8kHz
Stopband Attenuation	> 78dB
Resolution	14b

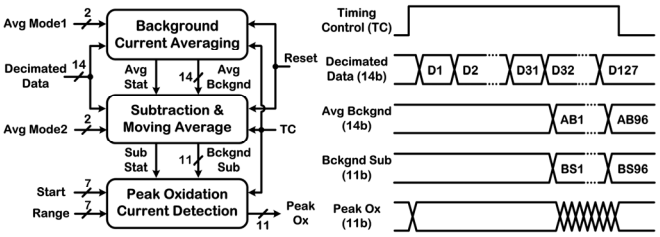

Fig. 4. Schematic block diagram and operation timing of the FSCV processor in the DSP unit.

among $BS_{1\sim96}$ in each FSCV scan. The start and range of *Bckgnd Sub* timestamps to find *Peak Ox* is defined by user-set *Start* and *Range* parameters (7b). The peak dopamine oxidation current is then computed by the time the *TC* signal goes low and remains valid until the next FSCV cycle.

IV. MEASUREMENT RESULTS

The DSP unit as depicted in Fig. 2 was synthesized and mapped to the Cyclone II FPGA, EP2C35F672C6, using Altera's Quartus II design software. The FPGA device was interfaced with the previously developed FSCV-sensing front-end [5] for FIA and biological experiments. In all subsequent tests, the FPGA device was programmed to obtain *Avg Bckgnd* from 16 consecutive FSCV scans and *Bckgnd Sub* from a moving average with that of the three previous FSCV scans. All FSCV data depicted in Figs. 5-7 were processed in real time using the FPGA device.

The FSCV-sensing front-end was interfaced with a CFM WE positioned in the inlet of a flow cell reservoir for *in vitro* experiments via FIA. All measurements were collected in buffer containing 150mM NaCl and 15mM TRIS (pH = 7.4). Dopamine concentrations of 0nM (i.e., buffer-only), 125nM, 250nM, 500nM, 750nM and 1μM were applied as a 5-second bolus injection to the flowing stream via a loop injector driven by a pneumatic actuator. The Ag/AgCl reference electrode (RE) was placed at the bottom of the buffer-filled reservoir. Fig. 5 shows the dynamic plot (i.e., *Peak Ox vs.* time) with a dopamine concentration of 750nM injected into the flow cell. The rise and fall time instances correspond to when dopamine injection in the flow cell was turned ON and OFF, respectively. The time offset is due to an inherent lag in the flow cell before electrolyte reaches the electrode. Fig. 6 depicts the measured calibration curve (i.e., *Peak Ox vs.* concentration), where data are the mean

± standard error of the mean (SEM) for three repetitions at each dopamine concentration. The red dashed line is the best-fit line determined by linear regression, and *r* is the correlation coefficient. A highly linear response was achieved, exhibiting a measured sensitivity of ~47.9nA/µM.

Biological experiments were also performed using urethane-anesthetized, adult, male Sprague-Dawley rats in accordance with guidelines approved by the Institutional Animal Care and Use Committee at Illinois State University. A twisted, bipolar, stimulating electrode (SE) was implanted in the medial forebrain bundle (MFB) and a CFM WE in the dorsal striatum, a rich, dopamine-innervated region of the forebrain implicated in the control of movement. Biphasic current pulses (±300µA, 60Hz, 4ms pulsewidth) were applied for 2s (i.e., a total of 120 pulses) to the dopamine axons traversing the MFB in order to evoke dopamine release in the dorsal striatum. The CFM, whose position was optimized in the dorsal striatum to sense the electrically evoked dopamine release, was externally interfaced with the integrated, FSCV-sensing front-end. FSCV measurements were conducted at a sweep rate of 400V/s and scan frequency of 10Hz. Fig. 7 depicts the transient dopamine release measured in the rat dorsal striatum following electrical stimulation of its MFB for 2s as indicated by the black bar below the trace. The corresponding background-subtracted cyclic voltammogram for chemical identification is also shown in the INSET. The dynamics of the evoked dopamine recording processed in real time with the FPGA device is in excellent agreement with that obtained offline using a home-base computer [4].

V. Conclusion

This paper reported on a DSP unit and its hardware implementation for real-time processing of FSCV data using an FPGA. In conjunction with an integrated, FSCV-sensing front-end, the functionality of the DSP unit was successfully evaluated via *in vitro* FIA and *in vivo* biological experiments. This work paves the way to ultimately co-integrate the neurochemical sensing and processing units together on an IC, enabling long-term experiments with awake, behaving subjects.

References

[1] D. L. Robinson, et al., "Monitoring rapid chemical communication in the brain," *Chem. Rev.*, vol. 108, pp. 2554-2584, 2008.

[2] P. E. Phillips, et al., "Subsecond dopamine release promotes cocaine seeking," *Nature*, vol. 422, pp. 614-618, 2003.

[3] M. Roham, et al., "A wireless IC for time-share chemical and electrical neural recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3645-3658, December 2009.

[4] M. Roham, et al., "A wireless IC for wide-range neurochemical monitoring using amperometry and fast-scan cyclic voltammetry," *IEEE Trans. Biomed. Circuits and Systems*, vol. 2, no. 1, pp. 3-9, March 2008.

[5] B. Bozorgzadeh, et al., "A neurochemical pattern generator SoC with switched-electrode management for single-chip electrical stimulation and 9.3µW, 78pA$_{rms}$, 400V/s FSCV sensing," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 881-895, April 2014.

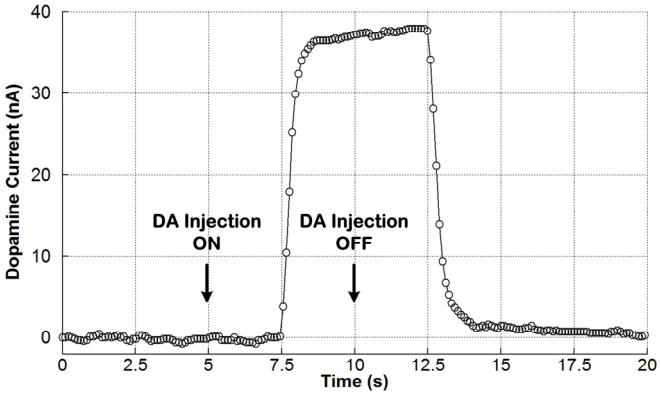

Fig. 5. Background-subtracted, peak oxidation current of 750–nM-dopamine after 20 seconds of 400-V/s, 10-Hz FSCV measured by FIA.

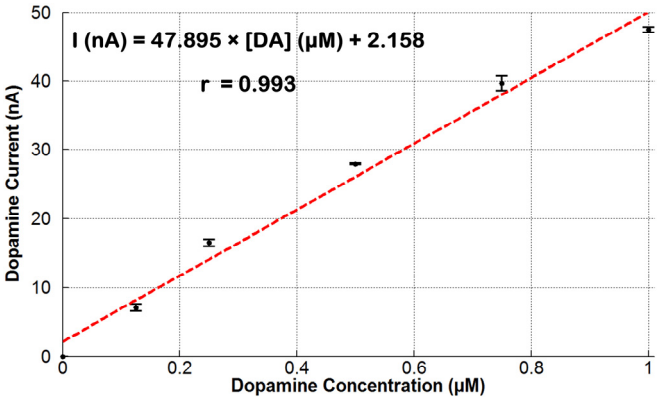

Fig. 6. Calibration curve (background-subtracted, peak oxidation current of dopamine *vs.* concentration) measured by FIA, exhibiting a sensitivity of ~47.9nA/µM. The red dashed line is the best-fit line determined by linear regression, and *r* is the correlation coefficient.

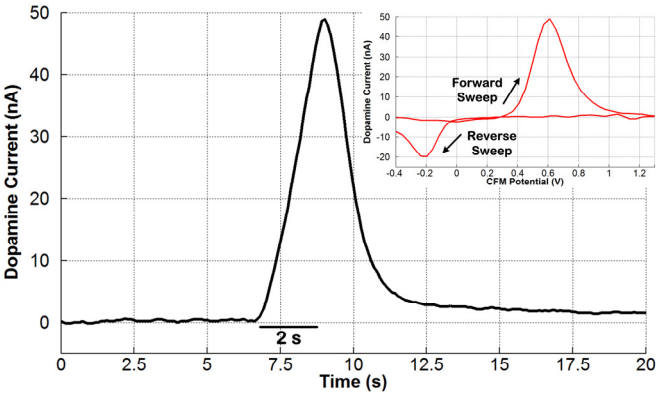

Fig. 7. Transient dopamine release measured in the rat dorsal striatum after 2s of electrical stimulation at 60Hz was applied to the rat MFB, indicated by the black bar below the trace. The corresponding background-subtracted voltammogram for chemical identification is also shown in the INSET.

[6] S. D. Iversen and L. L. Iversen, "Dopamine: 50 years in perspective," *Trends Neurosci.*, vol. 30, no. 5, pp. 188-193, 2007.

[7] J. C. Candy, "Decimation for sigma-delta modulation," *IEEE Trans. Communications*, vol. COM-34, no. 1, pp. 72-76, January 1986.

[8] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoustics, Speech, Signal Processing*, vol. ASSP-29, no. 2, pp. 155-162, April 1981.