High Throughput Single-Ion-Channel Array Microsystem with CMOS Instrumentation

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***Abstract*—Ion channels play critical roles in transporting chemical species into and out of cells. Ion channels are also targets for drug discovery and new receptor-based analytical technologies. To better understand ion channel structure and function, a high throughput membrane protein characterization microsystem is being developed. This microsystem integrates a 1024-element array of planar bilayer lipid membrane (pBLM) chambers with microfluidics and embedded CMOS electrochemical instrumentation circuits. This paper introduces the CMOS instrumentation circuits that support readout of 1024 pBLM elements in parallel and provide current pixel amplifiers within each cell for local amplification of the weak ion channel response currents.**

I. Introduction

Information about membrane protein functionality, their interactions with lipids and other proteins, and their dynamics and structure, is essential for an improved understanding of biological membranes and cell function in general. The implications of ion channels in a variety of diseases, including diabetes, epilepsy, hypertension, cancer and even chronic pain, have signaled them as pivotal drug targets. Approximately 15% of the world's 100 top-selling drugs are targeted at ion channels [1]. Ion channels have received widespread recognition for their application in biosensors, drug discovery, and protein/ligand screening.

Single-molecule techniques have been developed for the study of individual ion channels. Single molecule detection techniques enable an opportunity to record the behavior of an individual ion channel in real time. Two single-molecule techniques, patch clamp and pore-based membranes, have been used for single ion channel detection (SICD). Patch clamp is a laboratory method for studying the behavior of biomembranes *in situ.* The major drawback of patch clamp is the lack of control over the protein and lipid composition of the membrane patch. Pore-based membrane techniques overcome this drawback by incorporating purified channel protein into a bilayer lipid membrane (BLM) with a controlled lipid environment. BLMs have a simple structure with predictable, well-defined electrical properties. Artificial BLMs suspended across a pore, with control of the environment on either side of the pore, are often referred to as planar BLMs (pBLM).

Unfortunately, the existing pore-suspended pBLM methodologies require tens of hours to characterize a single membrane protein target, even at a minimal level of detail. Attempting to characterize membrane protein function in more detail, with regards to membrane lipid composition, solute composition (pH, ions, etc.), and the presence of ligands, then becomes an almost intractable task. To overcome these challenges, an automated microsystem structure with ~1000 pBLMs has been designed to enable truly groundbreaking capabilities for high throughput studies that permit rapid characterization of multiple membrane proteins simultaneously. The parallel-automatic solution control is achieved by a microfluidic array, which enables pBLMs to have a controlled lipid environment and rapid pBLMs screening. CMOS instrumentation has been used for single molecule recording [2-5]. However, no prior circuits capable of simultaneous measurement of ~1000 biomembrane elements, maintaining a single-molecule signal level (~pA), and maintaining high bandwidth to capture ion channel opening/closing events (~10 μs to 1 ms) have been reported. To address these challenges, the design of CMOS instrumentation circuits capable of rapid measurement, single-ion-channel resolution, and high density array implementation have been developed, and their characterization by simulation are reported in this paper. To readout the response of ~1000 pBLMs, the circuits utilize a time division multiplexing technique that reduces area and power consumption. Moreover, local pixel amplifiers are introduced to amplify the ~pA response current prior to further signal processing.

II. High Throughput Single-Ion-Channel Array Microsystem

A. Pore-based pBLM and Electrochemical Methods

PBLM with pore supported technique is widely used in functional studies for single ion channels because the pore structure supports ions passing through the ion channel. The general structure of a pore-based pBLM is presented in Fig.1. Two sides of the BLM are isolated in fluid chambers, which are filled with electrolyte solution. One protein is inserted in the pBLM and ions go through the ion channel under a given potential. The ion channel opening/closing events are recorded by the constant potential amperometry (CPA) technique that measures the response current pulse between electrode A and B at a DC potential. CPA is also used to evaluate the pBLM formation quality by measuring the pBLM impedance. Additionally, the electrical properties of a pBLM can be characterized using the electrochemical impedance spectroscopy (EIS) technique, which enables extraction of pBLM equivalent circuit model parameters.

B. Microfluidic

Recently, a pBLM positioned vertically within a microfluidic channel was introduced [6, 7]. The approach

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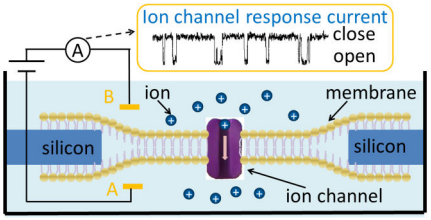


Fig. 1. General structure of a pore-based pBLM cell with a single ion channel protein. The opening/closing events of the ion channel can be detected by monitoring response currents between electrodes A and B.

forgoes the need of an aperture-containing substrate and permits an array of pBLMs to be self-assembled within microchambers shaped into the sidewall of a microfluidic channel. When a buffer and organic lipid solution are sequentially flowed through the channel, a pBLM is constructed at the mouth of each microchamber. The structure of the pBLM microchamber is shown in Fig. 2(a). With one electrode in each pBLM microchamber and one electrode is in the main channel, this structure enables many electrochemical measurements to be made in parallel. This structure is also suitable for high density array formation, as illustrated in Fig. 2(b-c). Microfluidic techniques facilitate rapid and cost-effective fabrication of BLM microarrays, whose properties vary combinatorial across the array. The capability of rapidly altering the solute environment around the pBLM by virtue of microfluidics provides be a major technical advance.

C. *High Throughput Microsystem*

Multiple microfluidic channels provide the capability of automatic, rapid, and high throughput pBLM formation. One challenge for a high throughput SICD microsystem is the wiring bottleneck inherent in connecting hundreds of individually measurable microchambers to instrumentation electronics. To overcome this challenge and enable high throughput membrane protein characterization, the pBLM microchamber arrays can be embedded with a CMOS electrochemical instrumentation chip. When the microfluidics are combined with CMOS instrumentation for electrical recording, the integrated system can achieve rapid and parallel-screening membrane proteins under multiple environmental conditions.

The SICD array microsystem being developed utilizes a carrier substrate to expand the surface area beyond the instrumentation chip, allowing room for multiple fluidic inlets/outlets while also connecting circuits I/O pads to external electrical contacts. The high density electrode array is fabricated on the surface of the instrumentation chip and directly connected to circuits for electrochemical readout. When connected to a computer-controlled data acquisition system, the user would have full control of the pumps and valves managing microfluidic operation as well as display and storage of characterization data. The SICD microsystem is illustrated in Fig. 2(c). For a typical 5 × 5mm^2 instrumentation chip, eight independent fluidic channels fit well within the area based on our experiences. When a buffer and organic lipid solution are sequentially flowed through the

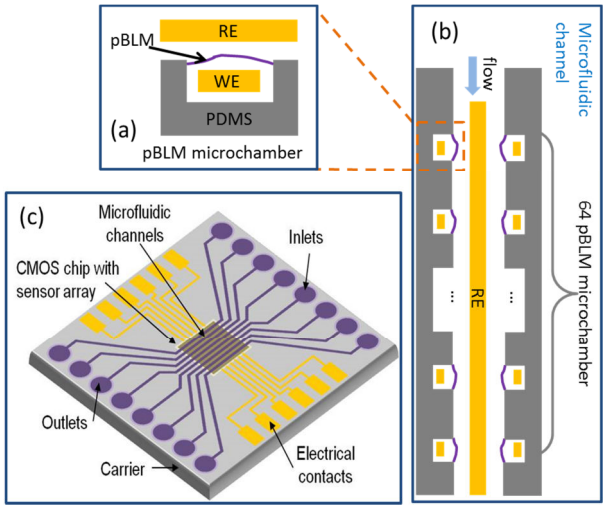


Fig. 2. (a) The structure of one pBLM microchamber with working electrode (WE) and reference electrode (RE). (b) One microfluidic channel with shared RE. (c) Concept view of the high throughput array microsystem for single ion channel detection.

microfluidic channel, a pBLM can be constructed at the mouth of each microchamber. The width of the pBLM microchamber is 50µm and the center-center pitch of the microchambers is 80µm. 64 pBLM microchambers could be in each microfluidic channel for a 5 × 5mm^2 chip, making the total number of the pBLM microchambers equal to 1024. This microsystem has been designed to enabled, for the first time, simultaneous characterization of single-molecule events within multiple biomembranes.

III. CMOS Instrumentation

A. *Multi-mode Instrumentation Circuits*

Microfluidic-driven pBLM formation and protein characterization are complicated processes. The CMOS instrumentation circuits are designed to support multiple modes based on the needs of different assays.

Mode 1: pBLM formation quality test by CPA technique.
Mode 2: pBLM classification by EIS technique.
Mode 3: simultaneous single ion channel event detection by CPA technique.

The pBLM quality can be evaluated by the membrane impedance because a poor quality pBLM has a large leakage current (as noise) that considerably reduces the membrane impedance. In *mode 1*, the circuit will determine if/when a high quality membrane is formed by comparing the pBLM impedance with a programmable threshold value selected from 100MΩ and 1GΩ. Generally, the impedance of a good quality pBLM should be above 1GΩ, and when the pBLM impedance is less than 100MΩ it is assumed to be poor. Any poor pBLMs will be skipped over during subsequent modes.

Mode 2 provides pBLM classification via EIS characterization. Different classes of pBLM have unique phase/amplitude spectrum characteristics, providing a second layer of information to describe the protein's environment beyond the impedance information provided in *mode 1*.

Mode 3 is the most challenging because it requires recording single channel opening/closing events with MHz

speed and sub-pA resolution. The instrumentation electronics have to guarantee *mode 3* performances, which require ultra-low noise and high speed readout circuits.

B. CMOS Instrumentation Architecture

To address the requirements and realize high throughput chip-scale biosensor arrays with simultaneous characterization of multiple bio-interfaces, a single protein electrochemical characterization (SPEC) chip was designed. For a 1024-element BLM array with simultaneous characterization, a straightforward approach is to have 1024 CPA/EIS readout blocks. However, the power consumption for 1024 readout blocks would be extreme (up to hundreds of watts), which would generate local hotspots that would degrade pBLM interface.

Because of the delicate nature of pBLM formation, this initial step of array formation can be expected to have a low yield, around 30% based on empirical evidence. Our experience also suggests the good quality pBLMs will occur roughly equally in three distinct structural classes. Furthermore, we estimate that the likelihood of populating an individual pBLM with a single membrane protein to be about 20% after experimental optimization. In other words, we expect a very low yield of single-protein, single-pBLM-class interfaces, demanding a high density array. However, this low yield provides an opportunity for several pBLM interfaces to share one CPA/EIS readout circuit. Based on these estimates, we expect 1-3 good quality, single-class, single-protein interfaces within each microfluidic channel. Thus, the instrumentation array has been designed with four CPA/EIS readout circuits per channel. This should ensure capture of single ion channel events, simultaneously across most functional interfaces, while also achieving hardware efficiency; a total of 32 CPA/EIS readout circuits occupies only 3.1% of area required for an instrumentation chip with 1024 CPA/EIS circuits and enables implementation within a 5x5mm^2 chip.

Tens of CPA/EIS current readout circuits working simultaneously introduce a noise immunity challenge. The high throughput array also has a large parasitic capacitance that distorts the electrochemical current signals. To solve these problems, an in-pixel electrochemical current amplifier for each pBLM element was chosen in the SPEC chip. This pixel amplifier significantly increases immunity to signal interference, solves the signal distortion caused by the array parasitic capacitance, and loosens the resolution requirement of the CPA/EIS readout circuit.

The architecture of the designed SPEC chip is shown in Fig. 3. There are eight independent potentiostats that set the independent bias potential for each microfluidic channel during CPA and EIS measurement. Digital memory is used to buffer the results between the CPA/EIS readout and uploading to an external host system through a serial peripheral interface communication bus. A digital control block manages the operation mode. Potentiostat and CPA/EIS readout circuit specifications for each mode are listed in Table I.

IV. CMOS Implementation and Results

A. Pixel Amplifier Design

Noise and speed are the two key considerations in the pixel amplifier design because the input signal of the amplifier is a high speed (down to 10µs pulse width) and weak (~pA) current pulse. A resistive feedback amplifier is simple to implement, but it suffers from the noise generated by the feedback resistor. A capacitor feedback amplifier is not suitable for measuring high speed low-level signals because the feedback capacitor limits amplifier speed. A current conveyor was selected as the amplifier in our design because it is good at high speed and for weak current amplification.

A cascade current mirror structure was utilized in the pixel amplifier to reduce crosstalk noise generated by the high speed switch coupling. The schematic of the pixel amplifier is shown in Fig. 4(a). Transistor M1 is a current sink controlled by 'Bias' thatensures amplification of the bi-direction ion-channel current. 'Sel' is the pixel selection signal. A large, pF-level, column parastic capacitor (Cp) is associated with each pixel amplifier output in the high throughput array, and the total gain of the amplifier was set as 25 to ensure capability to drive the Cp load. To eliminate the delay caused by transistor parasitic capacitances, the minimal gate length (L=0.6µm) was selected for all transistors. The layout size of the pixel amplifier is 27µm × 80µm, as shown in Fig. 4(b), which is small enough to ensure that each pBLM microchamber has its own pixel amplifier.

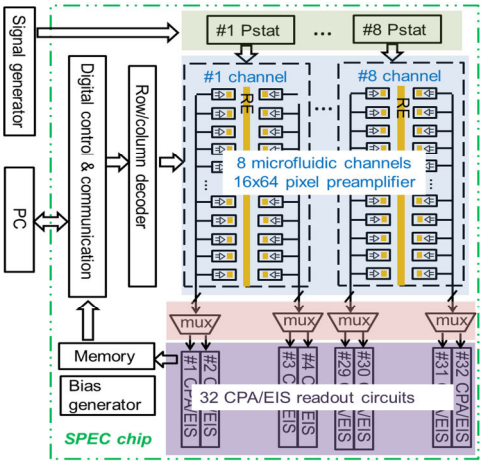


Fig. 3. Architecture of the single protein electrochemical characterization (SPEC) high density array chip.

TABLE I. THE PERFORMANCE REQUIREMENTS FOR POTENTIOSTAT AND READOUT CIRCUITS FOR EACH MODE.

	potentiostat	CPA/EIS readout circuit
mode 1 (CPA)	(1)frequency: DC (2)voltage range: ±250mV (3) step resolution: 10mV	(1)current readout mode: DC (2)current range: pA to mA (3)bandwidth: 10kHz
mode 2 (EIS)	(1)frequency range: 100mHz-1kHz (2)AC amplitude: 10mV (3)DC bias range: ±250mV	(1)current readout mode: AC (2)current range: pA to mA (3)phase range: -180° - 180° (4)bandwidth: 100kHz
mode 3 (CPA)	(1)frequency: DC (2)voltage range: ±250mV (3)step resolution: 10mV	(1)current readout mode: DC (2)current range: pA to 200pA (3)resolution: 300fA (4)bandwidth: 10MHz

B. CPA/EIS Blocks

The CPA/EIS electrochemical readout with digital output was adapted from our prior work [8]. The only limitation of this circuit is that its response could be slower than the fastest ion channel events, down to 10s of microseconds [3]. This limitation can be addressed by migrating the existing circuits to an advanced CMOS process to reduce the parasitic resistance and capacitance.

C. Simulation Condition and Results

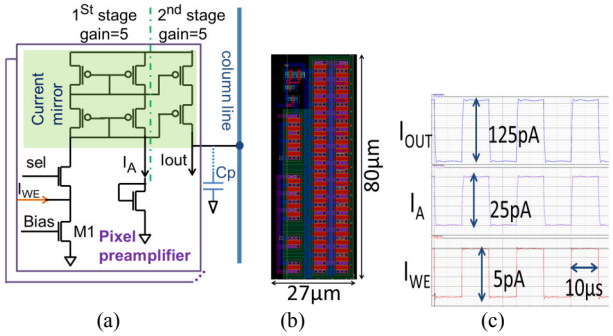
The pixel amplifier was designed at AMI 0.5µm CMOS technology and simulated in Cadence Spectre. The simulation parameters are listed in Table II. Cp = 1.5 pF was added at the load of the pixel amplifier in the simulation. To verify the function of the pixel amplifier, a 5pA, 10µs width current pulse was connected to the input of the pixel amplifier to mimic the fastest single ion channel opening/closing current. The simulation results of the pixel amplifier first and second stage output are presented in Fig. 4(c). These results show that the pixel amplifier can amplify a high speed current at a single molecule level (~pA).

To calculate the speed limitation of the pixel amplifier, a series of various width pulse current inputs were simulated. The simulation results are shown in Fig. 5. The pulse waveform distortion caused by the parasitic capacitance can be defined by the pulse width distortion percentage (PWDP), as shown in the right corner of Fig. 5. The PWDP for a 10µs pulse width current (the fastest ion channel speed) is only 1.04%. Thus, the pixel amplifier is fast enough to track the high speed opening/closing events.

In order to evaluate the pixel amplifier operation in a larger scale biosensor array, dependence of PWDP on array capacitance was simulated. Fig. 6 shows the simulated PWDP of I_{OUT} under various array capacitor values for a 10µs pulse input I_{WE}. The PWDP is only 2% even for a large Cp = 15pF.

D. Area Estimation and Power Consumption

Based on our previous experience with potentiostat, row/column decoder, bias, memory, digital control, and communication circuits, the total estimated area of the full SPEC instrumentation circuit defined by Fig. 3 is 5.36mm^2, which is well within the 5 × 5mm^2 chip size goal.



(a) (b) (c)

Fig. 4. (a) Schematic of two stage current conveyor pixel amplifier with column lineparastic capacitor. (b) Layout of the pixel amplifier. (c). Simulation results of the first stage output (I_A) and second stage output (I_{OUT}) with a 5pA, 10µs pulse current input (I_{WE}) that mimics a single ion channel opening/closing current.

TABLE II. SIMULATION PARAMETERS FOR PIXEL AMPLIFIER.

Process	2-Poly 3-Metal, 0.5µm
VDD	5 V
Temperature	25°C
Bias voltage (Bias)	0.9V
Column line parasitic capacitor (Cp)	1.5pF

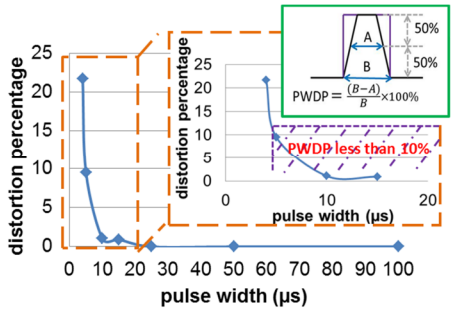


Fig. 5. Pixel amplifier simulation results of the distortion percentage (DP) with various input current (I_{WE}) pulse widths. Pulse width distortion percentage (PWDP) is defined in the top right corner.

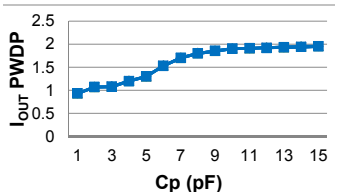


Fig. 6. Simulated I_{OUT} pulse width distortion percentage (PWDP) as a function of the column line parastic capacitance (Cp).

To manage power consumption, the pixel amplifiers and readout block were realized with the minimal power needed to achieve performance goals. Various power distribution schemes could be implemented to regulate surface heating. The power consumption of one pixel amplifier and one CPA/EIS is 15.5µW and the 5.4mW, respectively. The estimated total power consumption of the SPEC instrumentation chip is only around 200mW.

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