

Low complexity Underdetermined Blind Source Separation System Architecture for Emerging Remote Healthcare Applications

Suresh Mopuri, P Sreenivasa Reddy, Karthik Ch, Siva Prasad A, Amit Acharyya, Siva Ramakrishna V

Abstract—In this paper, we have proposed a low complexity architecture for the Under-determined Blind Source Separation (UBSS) algorithm targeting remote healthcare applications. UBSS algorithm, departing from the typical BSS conventional number of the sources and sensors present, which is of tremendous interest in the field of Biomedical signal processing especially for remote health care applications. Since such applications are constrained by the on-chip area and power consumption limitation due to the battery backup, a low complexity architecture needs to be formulated. In this paper, firstly we have introduced UBSS architecture, followed by the identification of the most computationally intensive module N-point Discrete Hilbert Transform (DHT) and finally proposed a low complexity DHT architecture design to make the entire UBSS architecture suitable for such resource constrained applications. The proposed DHT architecture implementation and experimental comparison results show that the proposed design saves 50.28%, 48.40% and 46.27% on-chip area and 53.25%, 48.01% and 45.95% power consumption when compared to the state of the art method for $N=32$, 64 and 128 respectively. Furthermore the proposed DHT architecture works for $N=2m$ point, but the state of art architecture works for $N=4m$ point, where m is an integer.

I. INTRODUCTION

Cardiovascular diseases (CVD) are the prime contributor to the high amount of mortality rate causing more than 30% global deaths in the world [1]. With the advent of mobile and communication technologies, advancement in the VLSI industries leading to the emerging field of Cyber physical systems and Internet of things are gradually making the remote personalized CVD monitoring systems a reality. In such remote health monitoring scenario the underlying principle is to capture the vital signs from the body, processing it on-chip and transmit it when necessary [2]. However, the vital signs are mixed with noise and other physiological artifacts, which therefore need computationally intensive signal processing to retrieve the physiological information back from the composite. Aforementioned problem resembles to the typical Blind Source Separation (BSS) where signals are separated without knowing how signals are mixed at the sensors. However, a well defined BSS system requires as many number of sensors as the sources there by increasing the number of on body sensors of the human subjects if the information is to be separated amidst the mixture of many signals [3-4]. These pose an engineering challenge to obtain

the information using less number of sensors than the sources present. This falls under the category of Underdetermined Blind Source Separation (UBSS) [5], which involves computationally intensive signal processing modules including Discrete Hilbert Transform (DHT) making it unsuitable for such remote health care applications where on-chip area and power consumptions are limited because they need continuous monitoring using battery backup. These aforementioned real problems and the corresponding engineering challenge motivate us to explore the UBSS system architecture in this paper by considering algorithm architecture holistic view and propose a low complexity UBSS system architecture. To the best of our knowledge this is the first attempt to take UBSS algorithm to the architecture level for its on-chip implementation especially but not limited in the context of the remote CVD monitoring problem.

UBSS system is based on the time-frequency (TF) domain approach [5], where DHT is a computationally intensive module as mentioned above. Our intention in this paper firstly is to propose UBSS architecture followed by low complexity architecture for the DHT module, which leads to low complexity design of UBSS system targeting for remote health care systems. The existing literature on the implementations of DHT can be broadly classified into transform domain and time domain implementations. Fast Fourier Transform (FFT) architecture [6] requires complex additions and multiplications. This was simplified using an architecture based on Fast Hartley transform [7] involving real additions and multiplications, that is computationally less complex compared to the FFT based architecture [6]. Apart from these, various approaches were present for the implementation of DHT such as Winograd Fourier Transform Algorithm, prime factor algorithm and Discrete Cosine Transform based approach [8-10]. Architectures in the time domain, on other hand, includes filtering approach [11] and systolic array approach [12]. In filtering approach the infinite duration of Hilbert transform was truncated to a finite duration and was implemented as a FIR filter causing significant loss accuracy [11]. In the fixed point systolic array based implementation [12] a parallel pipelined architecture was implemented with the help of precomputed coefficients but reconfigurability could not be achieved. Recently Reconfigurable architecture was implemented based on systolic arrays [13], which is limited for $4m$ -point, its computationally intensive nature does not allow its usage in the implementation of remote health care devices.

Motivated by the aforementioned facts, in this paper we present an architecture for UBSS system. Subsequently we

S.M, P.S.R, K.Ch, S.P.A, A.A, S.R.V are with department of Electrical Engineering, Indian Institute of Technology, Hyderabad, India-50205, e-mails: {ee13p0004, ee12p1007, ee13m1011, ee13m1010, amit.acharyya, svanjari}@iith.ac.in .This work is partly supported by the DEITY, India under the "IOT for Smarter Healthcare" under Grant No: 13(7)/2012-CCBT, Dated 25th Feb, 2013.

designed the architecture for DHT, which is low complexity and reconfigurable for 2m-point, where m is an integer . The paper is organized as follows. Section II describes in detail about the proposed UBSS architecture and proposes low complexity, reconfigurable DHT architecture followed by the experimental results and comparison in Section III and Section IV concludes the discussion.

II. PROPOSED ARCHITECTURE FOR UBSS SYSTEM

A. Prerequisites

The instantaneous linear mixing model of UBSS can be written as

$$x(t) = As(t) \quad (1)$$

where $s(t) = [s_1(t), s_2(t), \dots, s_N(t)]^T$ is source vector, $x(t) = [x_1(t), x_2(t), \dots, x_M(t)]^T$ is mixing vector, $A = [a_1, a_2, \dots, a_N]$ is real valued $M \times N$ mixing matrix, a_i steering vector and $M < N$ (M = Number of sensors and N = number of sources). The architecture has been developed for UBSS system based on time frequency approach in [5]. In this algorithm, the sources are extracted from mixtures by using STFDs (Spatial Time Frequency Distribution) and $N \leq 2M - 1$.

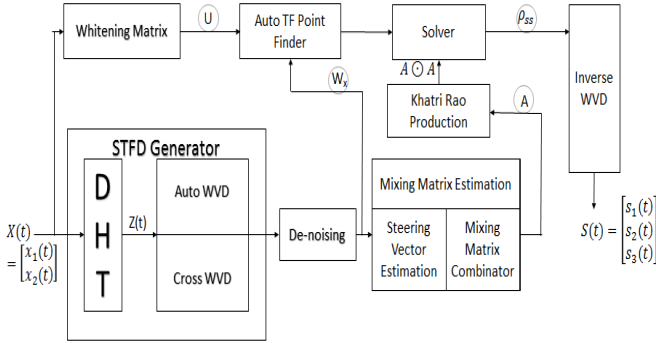


Fig. 1. Proposed Architecture for UBSS system

B. Overview of the Proposed Architecture

In real time signal processing, negative frequencies do not exist. Thus the application of Discrete Hilbert Transform (DHT) can eliminates negative frequencies. The signal which does not have negative frequencies, is called Analytical signal defined [14] as

$$z(t) = x(t) + jH\{x(t)\} \quad (2)$$

where $H\{\cdot\}$ represents DHT. The auto WVD (Wigner ville Distribution) of any square integral signal $z(t)$ is defined as

$$\rho_{zz}(t, f) = \int_{-\infty}^{\infty} z^*(t - \frac{\tau}{2})z(t + \frac{\tau}{2})e^{-j2\pi f\tau} d\tau \quad (3)$$

WVD is energy distribution in time-frequency (TF) domain. Similarly cross WVD is defined as

$$\rho_{zz}(t, f) = \int_{-\infty}^{\infty} z_1^*(t - \frac{\tau}{2})z_2(t + \frac{\tau}{2})e^{-j2\pi f\tau} d\tau \quad (4)$$

If substitute (1) in (3) and (4)

$$W_x(t, f) = AW_s(t, f)A^T \quad (5)$$

The STFD matrix (see Fig 1) for $x(t)$ is defined as

$$W_x(t, f) = \begin{bmatrix} \rho_{x_1x_1}(t, f) & \rho_{x_1x_2}(t, f) & \dots & \rho_{x_1x_M}(t, f) \\ \rho_{x_2x_1}(t, f) & \rho_{x_2x_2}(t, f) & \dots & \rho_{x_2x_M}(t, f) \\ \vdots & \ddots & \ddots & \vdots \\ \rho_{x_Mx_1}(t, f) & \rho_{x_Mx_2}(t, f) & \dots & \rho_{x_Mx_M}(t, f) \end{bmatrix} \quad (6)$$

The diagonal elements of (6) are auto WVD terms and others are cross WVD terms. Preprocessing is required to de-noise the STFDs because of inherent property of WVD. The de-noise procedure (see Fig1) is defined as

$$\frac{\|W_x(t_m, f_n)\|}{\max_f \|W_x(t_m, f_n)\|} \geq \epsilon_1 \quad (7)$$

where ϵ_1 is a threshold close to 0. If satisfies (7) keep (t_m, f_n) .

Mixing Matrix Estimation (see Fig 1): The mixing matrix is estimated by using traditional method single source domain (SSD) assumption and considering negative values of WVD. SSD means only one source is active. Under SSD, (5) can be written as

$$W_x(t, f) = a_i a_i^T \rho_{s_i s_i} \quad (8)$$

where $W_x(t, f)$ is a rank-1 matrix. The TF point satisfies the following criteria, which is under assumption of SSD.

$$\frac{\|W_x(t, f) - \operatorname{argmax}(|\lambda|)vv^T\|}{\|W_x(t, f)\|} \leq \epsilon_2 \quad (9)$$

Here, ϵ_2 is a real positive threshold close to 0 and set to be in [0.001, 0.1], λ Eigen value of $W_x(t, f)$ and v is unit normal vector which is linearly proportional to steering vector a_i . After that K-means clustering technique has been applied to combine the steering vectors, combined matrix is the mixing matrix A.

Separation of sources: In the separation of sources, first extract all the auto TF (see Fig 1) points by using the following criteria

$$\frac{\operatorname{trace}(UW_x(t, f)U^T)}{\|UW_x(t, f)U^T\|} \geq \epsilon_3 \quad (10)$$

Here U is the whitening matrix (see Fig 1) which is the inverse square root of the covariance matrix of the mixtures $x(t)$. ϵ_3 is a threshold close to 1. After that, the auto WVD of sources have been extracted using Khatri-Rao product (see Fig 1). The extraction of auto WVD of sources is defined as

$$\xi = (A \odot A)^{-1}W_x(t, f) \quad (11)$$

where $A \odot A$ is khatri-Rao product, $\xi = [\rho_{s_1s_1}, \rho_{s_2s_2}, \dots, \rho_{s_Ns_N}]^T$ is the auto WVD of sources. After that, take the inverse WVD (see Fig 1) to extract the sources. From (2), DHT (see Fig 1) is the most important module in the real time UBSS system. But DHT is computationally intensive nature, so here we proposing an architecture which is low complexity and reconfigurable for any N-point.

C. Proposed Low complexity DHT Architecture

The impulse response of DHT is defined as

$$h(n) = \begin{cases} \frac{2\sin^2(\frac{\pi n}{2})}{\pi n} & n \neq 0 \\ 0 & n = 0 \end{cases} \quad (12)$$

The Hilbert transform of a signal is computed as

$$y(n) = x(n) * h(n) \quad (13)$$

To calculate DHT, the generalized formula is obtained by substitution of (12) in (13) for $N = 2m$ -point.

$$y(n) = \frac{2}{N} \sum_{m=0}^{\lfloor \frac{N}{4} \rfloor - 1} [x(a) - x(b)] \cot\left(\frac{\pi}{N}(2m+1)\right) \quad (14)$$

$$y(n) = \sum_{m=0}^{\lfloor \frac{N}{4} \rfloor - 1} k_m [x(a) - x(b)] \quad (15)$$

where $0 \leq n \leq N-1$ and $k_m = \frac{2}{N} \cot\left(\frac{\pi}{N}(2m+1)\right)$

$$a = \text{mod}(n + N - 2m - 1, N) \quad (16)$$

$$b = \text{mod}(n + 2m + 1, N) \quad (17)$$

Where $\text{mod}(t, N)$ indicates that, if $t < 0$ then $t = t + N$ and if $t \geq N$ then $t = t - N$. From (15), we observed a similarity in computation, and it is treated as core element (CE), is defined as follows, can be used for computation of DHT recursively.

$$c = k(x(a) - x(b)) + c \quad (18)$$

Where a, b are memory indices of input memory (X memory).

The architecture has been implemented for $2m$ -point reconfigurable DHT, where m is an integer, based on (15), (16), (17) and (18). Here coefficients are precomputed and stored in the K memory. Having stored all these coefficients in memory, the computational complexity gets reduced significantly, as shown in the next section. X and Y memories are input and output memories respectively. The architecture as shown in Fig 2. The Controller (designed based on (16) and (17)) controls the CE, memories based on N signal. The reconfiguration can be extended to any M -point by increasing memory sizes and storing the precomputed coefficients. This will bring the *reconfigurability* in the design without any change in the basic architecture. The EOC (End of Computation) has been generated after completion of computation. From (16), (17) and (18) can conclude that the controller is implemented with help of adders, shifters and two counters leads to *low complexity* design. It has external write and read signals to write the samples to the input memory and to read the computed samples from output memory.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The purpose of this section is to show experimental results such as Power and Area for the DHT architecture. The architecture is coded in VHDL for 16 bit word length, synthesized with help of Cadence Encounter (R) RTL compiler at UMC 90-nm technology @ VDD=1V and clock frequency is @ 1MHZ and power consumption is computed using Synopsis Prime Time. The power consumption and Area have been

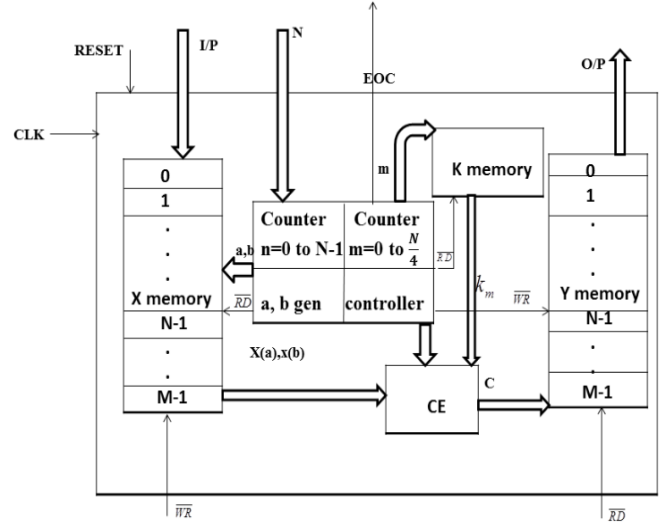


Fig. 2. Architecture for DHT

compared with state of the art method [13] as shown in Fig 3. It can be observed from Fig 3(b) $N=22$ that the state of the art method [13] is not applicable because it is reconfigurable design for $4m$ -point but not for $2m$ -point. Similarly in Fig 3(c) for $N=62$ and Fig 3(d) for $N=78, N=98$ the state of the art method [13] can not be used. It can also be noted from Fig 3(a-d) that the proposed architecture saves 50.28%, 48.40% and 46.27% on-chip Area and 53.25%, 48.01% and 45.95% Power consumption when compared with the state of the art method [13] for $N=32, 64$ and 128 respectively. The architecture's output is compared with original algorithm's (MATLAB) output in Fig 4(a-c) for different input ECG data like ECG suffering with Bundle branch block, Myocardial infraction and Healthy person ECG respectively took from PTB database [15] and Fig 5(a-d) for different input EEG data like Healthy EEG and Unhealthy EEG took from University of Klinik for Epileptologie database [16]. From Fig 4 and 5, it can be observed that the original algorithm's output and proposed architecture's output match favorably with maximum absolute error less than 1.39%.

IV. CONCLUSIONS

Here a low complexity architecture of the Under-determined Blind Source Separation (UBSS) algorithm is proposed based on TF domain approach [5]. Since the DHT is the computationally intensive module in the UBSS, a low complexity and reconfigurable N -point DHT architecture design is proposed where N is multiple of 2, which makes the entire UBSS suitable for the resource constrained applications like remote healthcare applications. Our proposed DHT architecture saves 50.28%, 48.40% and 46.27% on-chip area and 53.25%, 48.01% and 45.95% power consumption when compared to the state of the art method [13] for $N=32, 64$ and 128 respectively.

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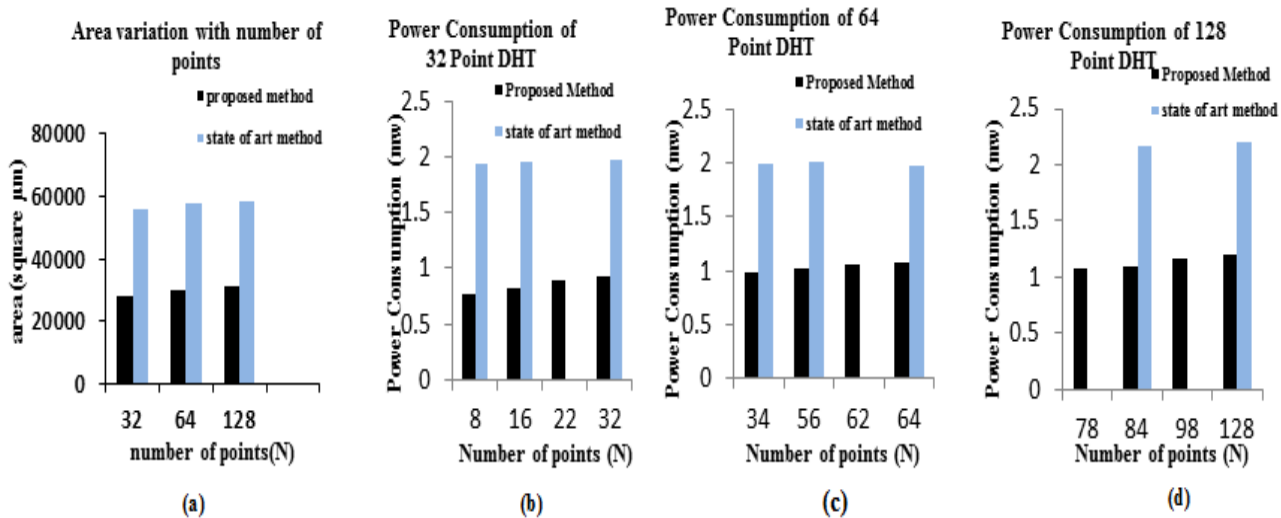


Fig. 3. Comparison of (a) Post synthesis area for different points, Power consumption for different point reconfigurable designs (b) 32, (c) 64, (d) 128

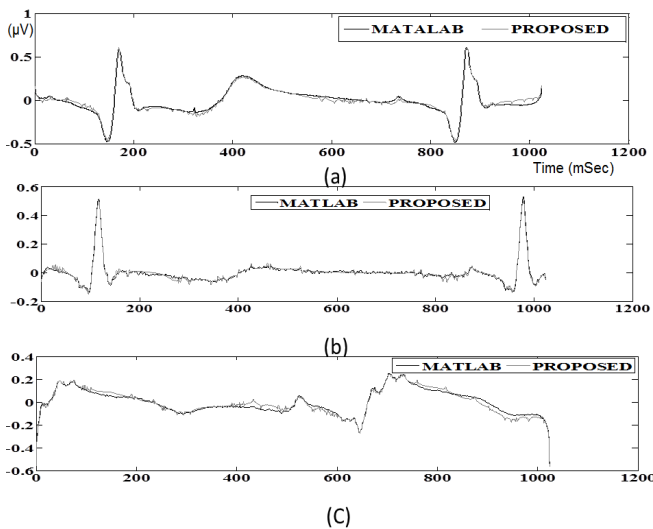


Fig. 4. Comparison of Proposed architecture's output with MATLAB's output (a) Bundle branch block ECG, (b) Myocardial infarction ECG, (c) Healthy person ECG

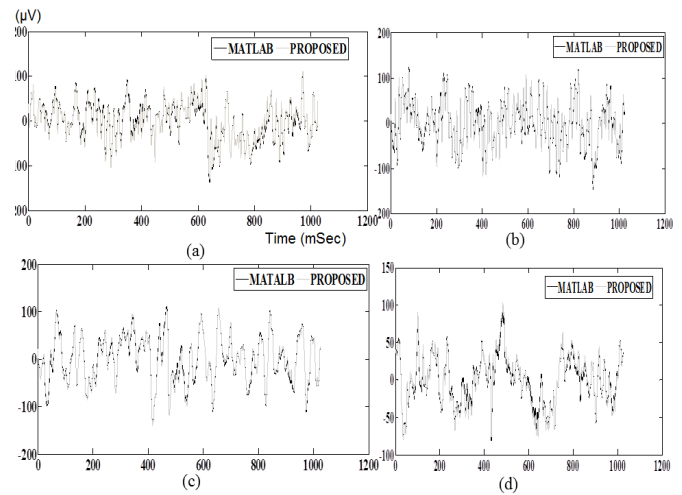


Fig. 5. Comparison of Proposed architecture's output with MATLAB's output (a), (b) Healthy person EEG, (c), (d) Unhealthy person EEG

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