Multichannel Wireless ECoG Array ASIC Devices

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***Abstract*— Surgical resection of epileptogenic foci is often a beneficial treatment for patients suffering debilitating seizures arising from intractable epilepsy [1], [2], [3]. Electrodes placed subdurally on the surface of the brain in the form of an ECoG array is one of the multiple methods for localizing epileptogenic zones for the purpose of defining the region for surgical resection. Currently, transcutaneous wires from ECoG grids limit the duration of time that implanted grids can be used for diagnosis. A wireless ECoG recording and stimulation system may be a solution to extend the diagnostic period. To avoid the transcutaneous connections, a 64-channel wireless silicon recording/stimulating ASIC was developed as the electronic component of a wireless ECoG array that uses SIROF electrodes on a polyimide substrate[4]. Here we describe two new ASIC devices that have been developed and tested as part of the on-going wireless ECoG system design.**

I. Introduction

In order to localize epileptogenic foci prior to brain resection surgery, an ECoG electrode array is placed on the brain surface to monitor the spatial distribution of neural activity under the array. This array may also be used to stimulate areas of the brain to assess the degree to which eloquent cortex would be at risk during a surgical resection. Transcutaneous connections to the array increase the risk of infection, thus limiting the duration of current ECoG-based diagnoses; a wireless ECoG array system is therefore desirable.

The wireless ECoG array under development is shown in Figure 1. A component of this system is a silicon ASIC (Applications Specific Integrated Circuit) which amplifies neural signals from, and provides stimulation pulses to, the electrodes. It also provides wireless bidirectional data connectivity.

An initial prototype array used an ASIC capable of controlling 64 electrodes. This 64 channel silicon ASIC is shown as item D in Figure 1. This ASIC was designed to provide 64 channels of simultaneous wireless recording to monitor brain activity, and also includes a single stimulator and switching network. The stimulator with the switching network can selectively stimulate one or more of the 64 electrodes in two groups. The prototype silicon 64-channel ASIC was successfully used to evaluate the *in-vitro* reliability of the ECoG assembly. This chip also included some experimental approaches which were helpful in the development and improvement of the two new devices described below.

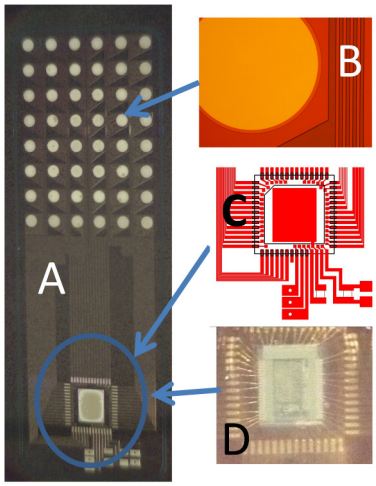

Figure 1. 64-electrode polyimide array used for electrochemical characterization and stability tests. The first-spin 64 channel chip is shown at item D.

For initial *in-vivo* experiments, it was decided that a smaller array would be easier to implant in the dog animal model. A smaller die size would also mean a smaller rigid object pressing against brain tissue. Two new devices were designed, an 8 channel device and a 16 channel device. Figure 2 shows their comparative sizes, as fabricated in the XFab CX08 BiCMOS process.

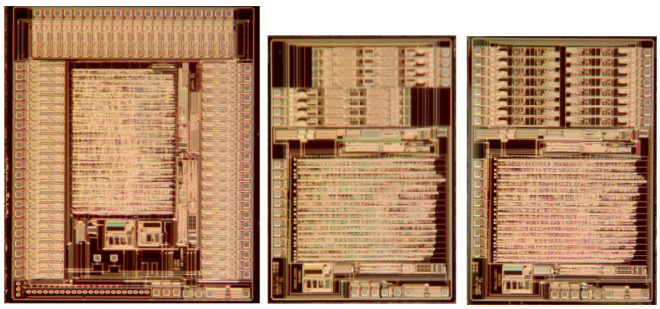

Figure 2. From left to right: First-spin 64 channel ASIC (4.3mm x 5.3mm), 8 channel and 16 channel ASICs (both 3.2mm x 4.7mm).

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Figure 3 below shows a functional block diagram of all three ASICs.

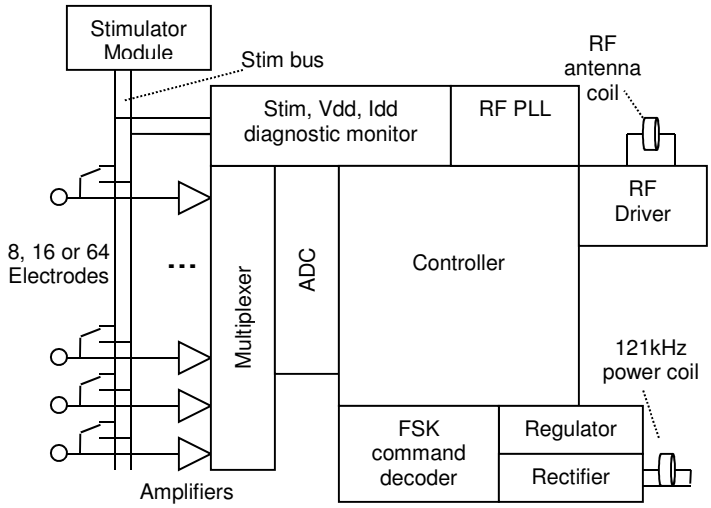

Figure 3. Functional block diagram of all three epilepsy ASICs.

II. Description of Operation

All three ASICs share the same command set, and can be used with identical external hardware and software. The 8 channel and 16 channel ASICs are identical except for the number and types of amplifiers used to amplify the EEG signals.

The ASIC is powered by a 121kHz magnetic field. This field is FSK modulated to provide an inward telemetry path for sending commands to the ASIC. The commands are protected by CRC error detection. The ASIC has two mutually exclusive modes, "record" and "stimulate".

In record mode, the stimulator is turned off. EEG signals are amplified, and a multiplexer TDM interleaves them and they are serially converted by the ADC into a data stream. A PLL uses the 121kHz powering field as a reference and generates a phase-coherent RF carrier, selectable to be 6.8MHz, 13.5MHz or 27MHz. After adding framing and CRC error correction bits to the serial data, this carrier is BPSK modulated and applied to the RF coil by the RF Driver.

In stimulate mode, stimulation parameters, such as pulse width and amplitude, are loaded into the ASIC. Stimulation currents are applied between two sets of electrodes, where the switching network is programmed to determine which groups of electrodes are anodic, and which are cathodic. Any electrodes may also be left unconnected to the stimulator. When a "stimulate" command is received, the ASIC produces one stimulation pulse.

III. Amplifier Results

The 16-channel device uses a new fully differential AC coupled amplifier design. To reduce design risk, an 8-channel device was fabricated using the proven EMG amplifier used in the IMES2 device[5][6]. Both amplifiers were physically larger than the amplifier design used in the 64-channel ASIC, and the 8-channel device only had room for 8 instead of 16 amplifiers because the existing IMES2 amplifier is physically larger than the new differential design (refer again to Figure 2, where the amplifiers can be seen at the top of the ASIC die). The wire bonding patterns of the 8- and 16-channel devices are both compatible with the polyimide electrode substrate under development.

Noise performance is an important parameter when collecting microvolt-level neural signals. The comparative noise performance is shown below in Table 1.

16 Channel	Full Scale	F.S.	
Gain Setting	Range	Noise (Vp-p)	SNR(dB)
200	10.4 mV	36.5 µV	49
800	2.5 mV	28.9 µV	38.7
5000	0.4 mV	64 µV	16
50,000	37.3 µV	17.6 µV	6.5
8 Channel	Full Scale		F.S.
Gain Setting	Range	Noise (Vp-p)	SNR(dB)
80	26.2 mV	133 µV	45.8
1800	1.1 mV	11 µV	40

Table 1. Comparative noise performance of the 8 and 16 channel amplifiers.

A 9-bit ADC can achieve an SNR of 54 dB, so it can be seen that the noise performance of the system is limited by the noise of the EMG amplifiers and not the resolution of the ADC.

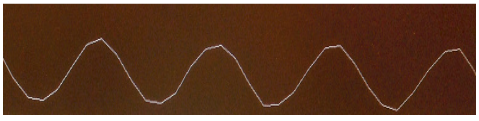

Figure 4. Screen shot of the data collection system showing a 30Hz, 400uVp-p sinusoid applied to the input of the 8 channel ASIC.

IV. 8 Channel Stimulator Operation

A. Stimulator Architecture

Aside from the amplifiers, the 8- and 16-channel devices are identical in every respect.

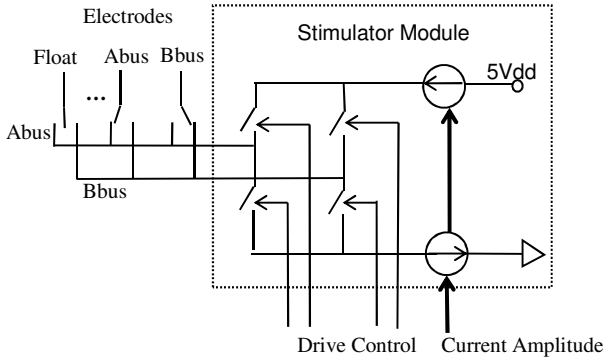

Figure 5. The stimulator module in the 8 and 16 channel ASICS. Each electrode has a switch than connects to either nothing, Abus or Bbus. Electrode stimulation is applied between Abus and Bbus.

For this reason, only the 8 channel stimulator results are shown. Figure 5 shows the architecture of the stimulator system in the ASICs (see also Figure 3).

B. *Stimulator Sequence*

To stimulate, a biphasic current is applied between one group of electrodes and another. The chip is set up (via forward telemetry) to assign each electrode to Abus, Bbus, or be left floating. The Stimulator Module applies current between Abus and Bbus. The Drive Control controls the pulse width and stimulation current sequence while the Current Amplitude control controls the magnitude of the stimulation current.

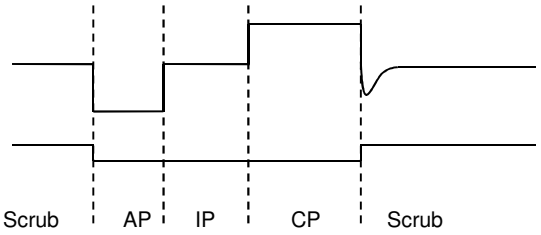

Figure 6. The stimulation waveform sequence consists of 4 phases; scrub, anodic phase (AP), interphase interval (IP), cathodic phase (CP) and returning to scrub.

In stimulate mode (as opposed to record mode), the stimulator idles in the Scrub phase before a stimulation pulse starts. Scrub insures all electrodes start the pulse at the same potential, connecting Abus to Bbus so as to short all stimulating electrodes together. There is also an optional setting called ScrubToGround, where Scrub connects Abus to Bbus to the chip supstrate.

In the anodic phase, current is pulled from all electrodes connected to Abus, and this current returns through the electrodes connected to Bbus. The Current Amplitude and duration of this phase is programmable.

In the Interphase interval, Abus and Bbus float, so no current flows.

In the cathodic phase, current is pulled from all electrodes connected to Bbus, and this current returns through the electrodes connected to Abus. The Current Amplitude and duration of this phase is programmable.

The stimulator returns to the Scrub phase until the next stimulate pulse command is received via the forward telemetry link.

C. *Symmetric and Asymmetric Modes*

In Symmetric mode, a current sink/source is applied to Abus while a matching current source/sink is applied to Bbus, resulting in a current waveform which is nearly independent of electrode voltage. Note that the anodic and cathodic currents may be programmed differently in this mode if desired.

In the Asymmetric mode, current is pulled out of Abus and returned to Bbus in the anodic phase like in the Symmetric mode. In the cathodic phase however, the current will flow into the Abus electrodes only until the voltages on Abus and Bbus become equal. This means that the voltage difference from Abus to Bbus will always be negative.

D. *Stimulator Capabilities*

The Current Amplitude is a logarithmic control, and the amplitude is set with a number 0-255 which produces 0mA to 4.5mA. The cathodic and anodic current amplitudes are set independently, so non-symmetric pulses may be produced.

The durations of AP, IP, and CP are set independently, and can be varied from 0 to 521uS in 8.25uS increments.

V. Stimulator Waveforms

In the waveforms below, the top red trace is the voltage across a 1k load resistor between cathodic and anodic electrodes connected to Abus and Bbus respectively (except for Fig 10). The scale is therefore 1mA/V. The yellow and blue traces are the voltages with respect to chip substrate of the anodic(yellow) and cathodic(blue) electrodes.

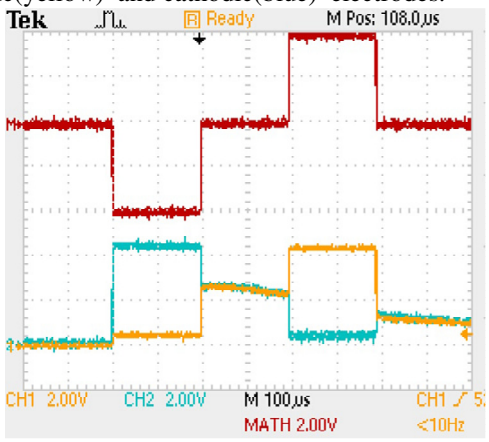

Figure 8. 4mA anodic and cathodic current, 100us AP,IP and CP, Scrub toGround=0 (Abus and Bbus connected but floating during scrub).

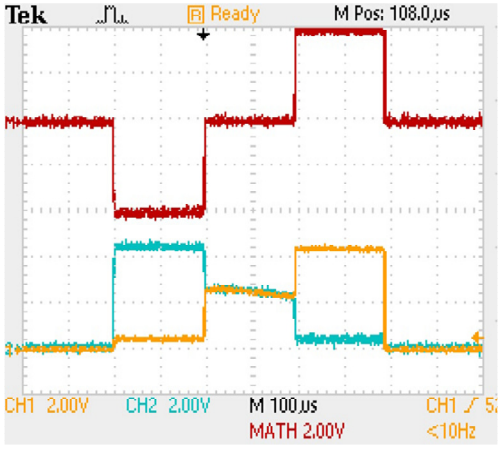

Figure 9. 4mA anodic and cathodic current, 100us AP,IP and CP, Scrub toGround=1 (Abus and Bbus connected and connected to Ground during scrub).

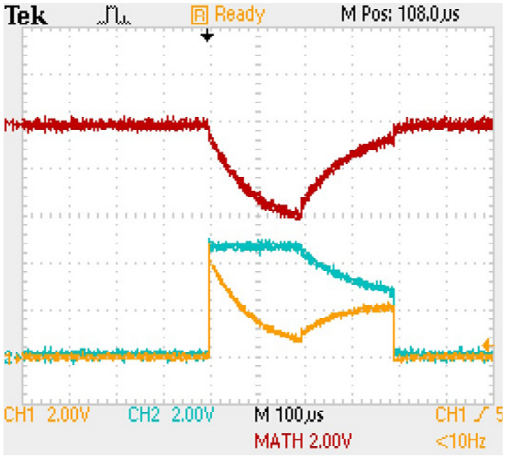

Figure 10. Electrode load is a 0.1uF capacitor in series with a 100 Ohm resistor to illustrate the Asymmetric mode. Red trace is voltage across the electrode load. 4mA anodic and cathodic current, 100us AP,IP and CP, Scrub toGround=0 (Abus and Bbus connected but floating during scrub).

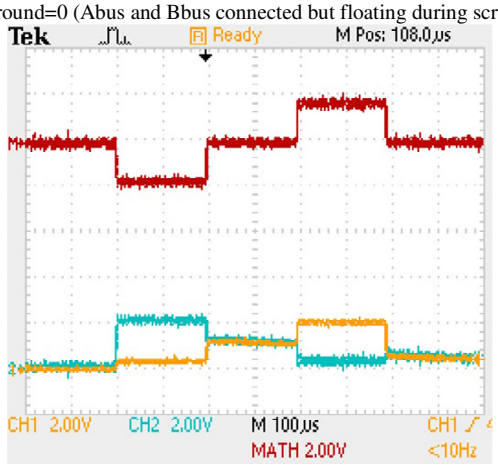

Figure 11. 1mA anodic and cathodic current, 100us AP,IP and CP, Scrub toGround=0 (Abus and Bbus connected but floating during scrub).

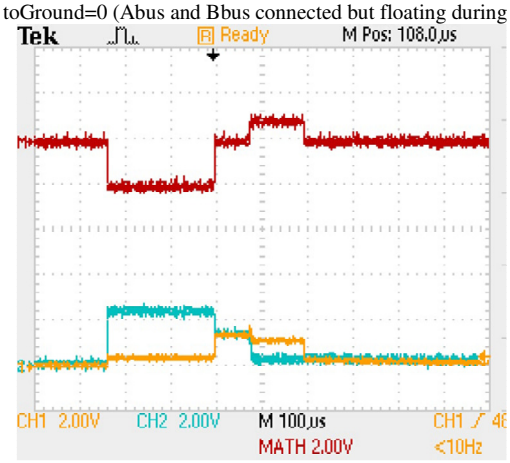

Figure 12. Illustrating independent control of anodic and cathodic currents and durations. 1mA anodic and 0.5mA cathodic current, 250us AP, 75uS IP, 130uSCP. Scrub toGround=0 (Abus and Bbus connected but floating during scrub).

VI. Stimulator Waveform Monitoring

An internal monitor circuit can sample the differential electrode voltage at a predetermined point in time after a stimulation pulse is started. By issuing multiple pulses while varying the sampling time, a reconstruction of the electrode voltage waveform may be telemetered to the external system controller to verify the integrity of the electrodes and their connections to the ASIC.

VII. Conclusions

Preliminary data presented here demonstrate that the two ECoG ASIC's work as designed and meet the anticipated needs of an ECoG array ASIC. The amplifier noise performance appears sufficiently good to perform the animal experiments, but reducing the noise to below the level of the ADC dynamic range would deliver better neural data. Amplifier noise must be reduced by about a factor of 4 in order to be below the dynamic range of a 9 bit ADC. Physically smaller amplifiers would reduce the size of arrays, making implantation easier. Since the logic core of these devices takes up more than half of the die area of the 16 channel ASIC, moving the design from a 0.8u to a 0.35u feature size process would cut the logic size by a factor of 5, either allowing for a die size reduction, an increase in the number of channels, or an increase in available amplifier area to reduce their noise.

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