A Multichannel Current Stimulator Chip for Spatiotemporal Pattern Stimulation of Neural Tissues

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***Abstract*— We developed a prototype very-large-scale integration chip of a multichannel current stimulator for stimulating neural tissues by utilizing 0.25 μm high-voltage complementary metal-oxide-semiconductor technology. Our designed chip has 20 output channels that are driven by five current buffers arranged in parallel; each buffer controls four output channels in time-sharing mode. The amplitude of a stimulation pulse can be controlled within a range of approximately $\pm$100 μA/phase in each output channel. The stimulus parameters, e.g., amplitude and duration, are controlled separately for each channel by digital codes stored in built-in registers. Combinations of anode and cathode electrodes to pass the current can be changed online. We integrated our stimulator chip with a multielectrode array and studied the neuronal responses to multichannel current stimulations with various temporal patterns in mouse brain slices.**

I. Introduction

To quantitatively analyze neural circuit dynamics through the relationship between the input and output, physiological neural responses must be measured while effectively changing multichannel and multivariate input parameters. Multichannel electrical stimulation is especially useful for measuring tissue slices surgically removed from experimental animals or incubated neural circuits because of the lack of signal input from sense organs. Currently, commercial stationary current stimulators are used extensively for these physiological experiments[1], [2]. However, these stationary stimulators occupy a comparatively large space because they consist of discrete circuits. A physiological experimental system that includes a stationary stimulator becomes complex as the number of stimulation channels increases. Therefore, setting up an experimental system in limited spaces such as a microscope stage or in an incubator is difficult.

In the research field of neural prosthesis, a multichannel stimulator chip has been developed with very-large-scale integration (VLSI) technology for applications such as cochlear implants[3], [4], artificial vision[5], [6], [7], [8], vestibular prostheses[9], and deep brain stimulation[10], [11], [12]. Note that these chips are not suited for the above physiological experiments because they were designed for specific use and thus have limited functions. Previous studies have verified that the stimulator chip met the required specifications. However, their results are insufficient for evaluating the applicability of these stimulator chips to neural tissues.

The development of versatile experimental system will require the application of a wide variety of electrodes. For example, in an experiment using a tissue culture or co-culture with neuron and glial cells or in the case wherein a needle-type multielectrode is inserted into tissue, the impedance of the electrode-tissue interface will be more than 100 kΩ because of the glial cells around the electrode[13], [14], [15]. Since the voltage drop at the output stage of the stimulator chips increases with the impedance of the electrode-tissue interface, the stimulator chips are required to have high-voltage compliance exceeding several volts. Recently, stimulator chips with high-voltage compliance have been fabricated, mostly for implant application[6], [9], [8], [16], [17], [18], [19].

In the present study, we designed and developed a prototype VLSI chip of a multichannel current stimulator for versatile use, such as in a physiological experiment, by utilizing 0.25 μm high-voltage complementary metal-oxide-semiconductor (CMOS) technology. The stimulator chip can control a spatiotemporal stimulation pattern with the aid of embedded current buffers and registers. In experiments, we used the stimulator chip to induce neuronal responses through multichannel stimulation of a cerebral tissue in vitro.

II. Multichannel current-mode stimulator chip

Fig. 1 shows a block diagram of our designed multichannel current stimulator chip. The chip has 20 output channels to connect to a multielectrode array. In order to generate various stimulation patterns, each electrode should be independently controllable. However, the number of electrodes that can be controlled independently in a single chip is restricted because a relatively large floor area is needed to implement a current stimulation buffer that generates current pulses. Therefore, one current stimulation buffer was designed to control four output channels, and these were arranged to be five lines in parallel. In standard physiological experiments, a biphasic current pulse stimulation is used to avoid charge accumulation in tissues. To realize a biphasic current pulse, monopolar and bipolar configurations are commonly used for the current stimulator[20]. The bipolar configuration has about twice the voltage compliance of the monopolar configuration for architectural reasons[20]. However, the stimulation approach of the bipolar configuration is limited because a pair of electrodes is required to generate the biphasic current pulse, and the stimulator can only apply the current to tissue between these two electrodes. For the

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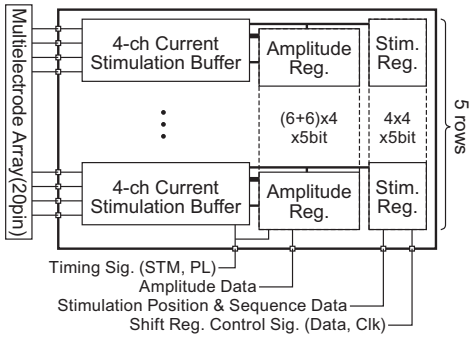

Fig. 1. Design block diagram of our multichannel current stimulator chip.

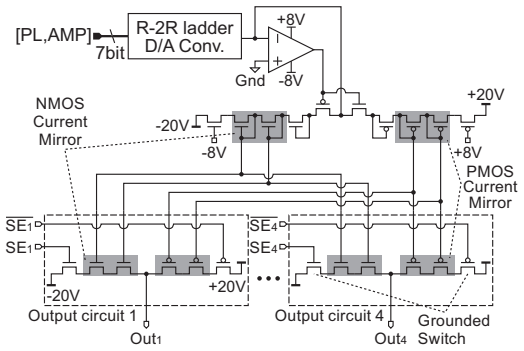

Fig. 2. CMOS circuit diagram of the 4-ch current buffer.

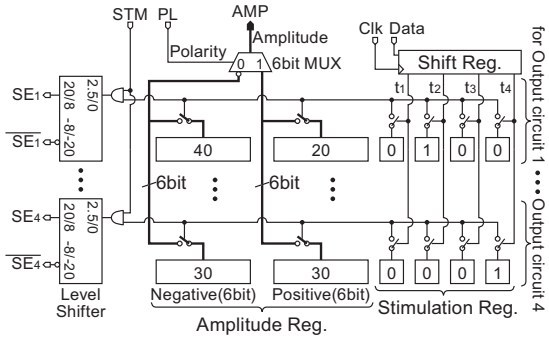

Fig. 3. Digital block diagram of the amplitude and stimulation registers per one current buffer.

monopolar configuration, the stimulator applies the biphasic current pulse from a single electrode through tissue to a common ground and can realize stimulation using a pair of electrodes, such as in the bipolar configuration. Therefore, we selected the monopolar configuration so that we could apply various stimulation approaches.

Fig. 2 shows a circuit diagram of the four-channel current stimulation buffer. This buffer consists of an R-2R ladder-type current-mode D/A converter (DAC), a differential amplifier, and P-type metal-oxide-semiconductor (PMOS) and N-type metal-oxide-semiconductor (NMOS) current mirrors[21]. The DAC produces a positive or negative analog current according to the polarity signal from “PL” and the 6-bit amplitude signal from “AMP”. The current from the DAC flows in the input stage of the PMOS or NMOS current mirror, and at the same time, the input stage of another current mirror is turned off by the output of the differential amplifier. The input stage of either the PMOS or NMOS current mirror is coupled with the four output stages of the current mirrors in the output circuits, and those are connected with each other in parallel. The current mirror ratio was designed to be 1:1. When one set of the switch transistors (i.e., grounded switches) arranged at the source sides of the output circuit is turned on, the output stage of the corresponding PMOS or NMOS current mirror generates the same current of the input stage. The output stage of the other current mirror is electrically isolated from the output channel by the high impedance. Therefore, the output channel produces the outflowing or inflowing current defined by the PL and AMP inputs of the DAC. If high-voltage CMOS technology is not used, multichannel switching is realized where the output of the current stimulation buffer, which includes the output stage of the current mirror, is connected with one of the channels by a demultiplexor consisting of CMOS switches[21]. However, when high-voltage CMOS technology is used to achieve high-voltage compliance because the gate-source voltage is restricted to 12 V, the CMOS switch requires inputs of $\pm$20 V, which is not available. Therefore, as presented above, in our stimulation buffer, each output circuit has the current mirror's output stages controlled by a set of grounded switches. To flip a grounded switch within the limits of the gate-source voltage, a level shifter must be in front of the grounded switch.

To adjust the stimulus parameters, each stimulation buffer has two registers for the current amplitude and stimulation timing, as shown in Fig. 3. The impedance of the electrode-tissue interface and charge threshold to evoke cortical activity differ with each electrode position. Therefore, the amplitude register consists of two 6-bit registers to memorize positive and negative pulse amplitudes independently in each output circuit. The stimulation timing is divided into four periods corresponding to the number of channels of each stimulation buffer. If a stimulation sequence of the four channels is fixed, artificial responses may be evoked depending on the stimulation sequence. Therefore, to stimulate an arbitrary sequence from the four channels, each output circuit has a 4-bit stimulation register consisting of four flip-flops corresponding to the four periods. A shift register selects the four flip-flops in series according to the four periods $\mathrm{t}_1 - \mathrm{t}_4$. If one of the four flip-flops memorizes “1”, the output circuit is chosen; the flip-flop is selected by the shift register, and its corresponding output of the amplitude register is connected to the DAC. Note that only one output circuit is chosen in each period. Basically, the amplitude register is set once when used. The stimulation register is rewritten in synchronicity with the frame rate of the imaging device and inter-pulse interval. Therefore, the setting data can be written in each register independently.

Fig. 4 shows an example timing diagram of the control signals for generating biphasic current pulses. When the registers are set to the values in Fig. 3, output circuits 1 and 4 are chosen during periods t_2 and t_4, respectively. One of the

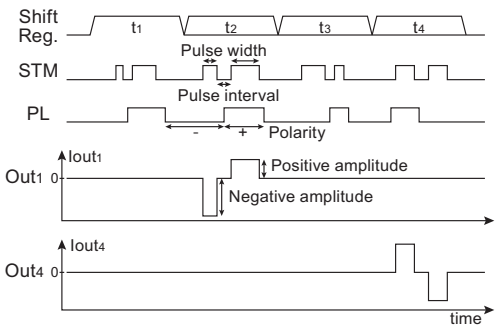

Fig. 4. An example of the timing diagram of control signals and the corresponding current outputs.

two amplitude registers is selected by the polarity signal of the stimulation PL and is connected to the DAC. During the initial part of t_2, since the PL is low, an inverted output of the negative amplitude register and PL are connected to the DAC as a 7-bit command signal (i.e., PL and AMP). Under this condition, when the stimulation timing signal STM becomes high, output circuit 1 becomes active and produces a negative current pulse according to the negative amplitude 40. During the latter part of t_2, since the PL is high, the output of the positive amplitude register and PL are connected to the DAC. Output circuit 1 produces a positive current pulse according to the positive amplitude 20 while the STM is high. As a result, output circuit 1 produces a cathodic-first biphasic current pulse during the t_2 period. The phase duration and inter-phase interval can be controlled by the STM timing. In addition, the anodic-first pulse can be realized by the PL timing, as shown in Fig. 4 for t_4. The output current amplitude increases as some output channels are shunted and stimulated simultaneously because the output circuit of the stimulation buffer consists of current source circuits.

We fabricated a current-pulse stimulator chip using 0.25 μm high-voltage CMOS technology capable of a maximum voltage supply of $\pm$20 V. Fig. 5A shows the layout design of the chip. The die size was $3.5\mathrm{mm} \times 3.5\mathrm{mm}$. The current buffer was designed to be able to generate a maximum current pulse of $\pm$100 μA with 7-bit accuracy. The power consumption was designed to be 21.8 mW without current stimulation. The time accuracy of the phase duration was sufficiently high because the rise and fall times were less than 1 μs, which is much less than the several hundred microseconds of a typical phase duration. The processing cycle, which includes the write time of the stimulation register and the four periods of pulse generation, was easily set to within 5 ms because the write time to the stimulation register was 80 μs at a transmission rate of 1 Mbps. In other words, a pulse train was easily produced at 200 Hz from all 20 channels.

III. Measurement results

To evaluate the performance of our chip, we first measured the stimulus current output in the circuit shown in Fig. 6 A. Parallel RC circuits (530 kΩ with 0.47 nF and 53.4 kΩ with 4.8nF) with impedances of 285 and 28.2 kΩ at 1 kHz

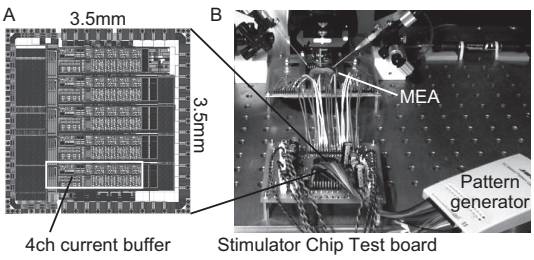

Fig. 5. The developed stimulator chip. A. Layout design. B. Overview of the experimental system for VSD imaging.

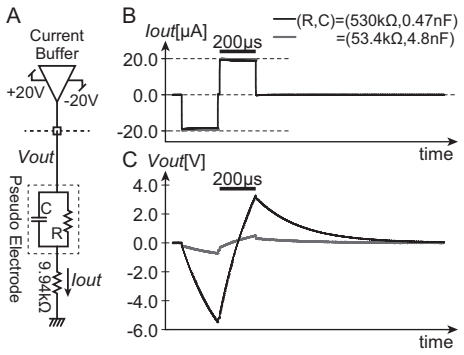

Fig. 6. Measurements of the current pulse outputs from the current buffer and the resulting voltage drops across the RC-electrode model circuits. A. Connection diagram. B. Current pulse outputs. C. Resulting voltage drops.

were connected to one of the output channels instead of a stimulating electrode. Fig. 6 B shows the biphasic current pulse I_{out} passing though the RC model electrode and the resistance, which was much smaller than the resistance of the RC circuit and placed to measure the current. Fig. 6 C shows the output voltage response V_{out}. In this measurement, the 7-bit input signals to the DAC (PL, AMP) were set to generate an amplitude of approximately $\pm$20.0 μA. As shown in Fig. 6 B, the current buffer generated a biphasic current pulse with almost the same amplitude as the preset value regardless of the voltage drop at the RC circuits, as shown in Fig. 6 C.

Fig. 7 A plots the measured amplitudes of the stimulus current I_{out} of every channel against the 7-bit amplitude command. As shown in the plot, the linearity of the stimulus current amplitude was sufficiently high with positive and negative maximum average values of 94.4 and -89.9 μA, respectively, and standard deviations of 1.49 and 8.49 μA, respectively. These were close to the design values. Our chip was not affected by variations in the current amplitude because of the amplitude register for each output channel. Fig. 7 B plots the measured amplitudes of the current pulse multiplication due to shunting of all output channels. The maximum current amplitude was approximately $\pm$2 mA, which was 20 times the amplitude of a single channel.

Table I compares a commercial stationary current stimulator (STG1008, Multichannel systems[1]), the results of previous studies, and our chip. In our circuit design, the overdrive voltage to drive transistors in the output circuit was a few hundreds of millivolts, which was negligible compared

TABLE I

COMPARISON WITH PREVIOUS STUDIES.

	STG1008[1]	Ghovanloo'07[19]	Jiang'11[9]	Ethier'11[16]	Ortmanns'07[8]	This work
Process	–	1.5μm	0.6μm	0.18μm, 0.8μm	0.35μm	0.25μm
Die size [mm^2]	–	4.6×4.6	2.27	1.0×1.0, 2.9×2.9	4.4×4.9	3.5×3.5
Number of channels	8	64	8	4	232	20
Configuration	–	Bipolar	Bipolar	Monopolar	Monopolar	Monopolar
Voltage compliance[V]	150	4.75 + 4.85	–	14.5*	–	–
Supply voltage[V]	100(AC)	5	18	3.3	22.5-35	40
Max stimulation current [A]	$\pm$0.8m	$\pm250\mu$	$\pm$1m	$\pm167\mu$	$\pm124\mu$, $\pm248\mu$, $\pm496\mu$, $\pm992\mu$	$\pm100\mu$@20ch $\pm$2m@1ch
Resolution[A]	0.2μ (13bit)	8.43μ (6bit)	4μ (9bit)	– (7bit)	4μ, 8μ, 16μ, 32μ (6bit)	1.6μ(7bit@20ch) 6.3μ(9.3bit@1ch)

*Two fully integrated charge pumps generates a high supply voltage from 3.3V supply.

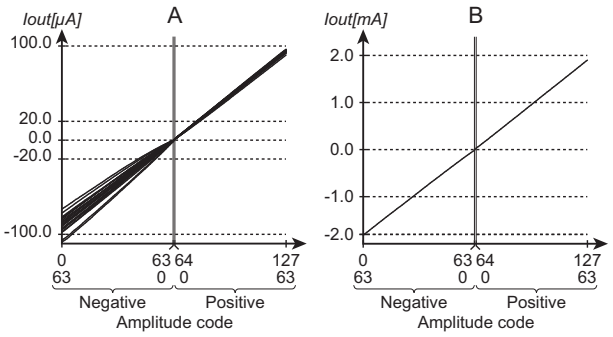

Fig. 7. Measured amplitude of the current pulses plotted against the 7-bit amplitude code. A. Results of every 64 channels. B. Result by shunting all output channels.

to the supply voltage of 40 V. Therefore, the compliance voltages in the monopolar and bipolar configurations were almost the same and twice the supply voltage, respectively. The higher compliance voltage of our chip, compared with the others, should be advantageous to a delicate electrophysiological experiment. For example, in order to realize a spatially localized stimulus, one may prefer the geometrically small electrode-tissue interface while reducing the current amplitude yet with an enough charge density for exciting neurons. In previous studies with such demands, glass microelectrodes with the open tip diameter of a few microns have been widely used. The impedance of those electrodes is often as high as 1 MΩ, which requires the voltage of a few tens of V to generate the stimulus current of a few tens of μA. Our chip had a somewhat lower limit of the maximum current amplitude per channel but a higher current resolution than the previous chips (Table I). The latter is thought to be critical to control the charge balance of stimulus current, and in turn, to avoid metal elution from the electrodes, electrolysis of water, and/or pH change in the tissue during the stimulation. Thus, our chip had a higher reliability of reducing such negative influences as compared with the previous chips. By shunting some electrodes, the maximum current output of our chip could be comparable to, or even larger than, those of the others (up to 2 mA, Table I). Our chip can be applied to various physiological experiments because of the above-mentioned specifications that meet actual experimental demands. Of course, the commercial stimulator (STG1008) had fairly high voltage compliance and current resolution setting but was relatively large; STG1008 had dimensions of $275\mathrm{mm} \times 330\mathrm{mm} \times 115\mathrm{mm}$[1]. In contrast, our stimulation chip system can be built on a substrate the size of a cash card.

We tested whether our stimulator chip can be used for the multichannel stimulation of a cerebral tissue in vitro. All animal care and experimental procedures in the present experiments were approved by the committee for animal research of Osaka University and performed in accordance with the guidelines from the Physiological Society of Japan. In order to visualize the spatial correspondence between the stimulation site and the responding region in the tissue, we combined a glass-bottom multielectrode array (MEA[1]) for the stimulation and the voltage-sensitive dye (VSD) imaging technique to record the neural responses. Fig. 5 B shows an overview of the experimental system. Fig. 8 A shows a near-infrared transmission image of a coronal slice of a mouse ' s (C57BL/6) cerebrum hemisphere placed on an MEA dish. The slice was pre-stained with the absorption VSD NK3630 (Nippon Kanko Shikiso Kenkyusho), and VSD imaging[22] was performed for the observation area shown in Fig. 8 B. The chip outputs of the four stimulation buffers were separately connected to the four electrodes (channels 1-4 in Fig. 8 B) of the MEA, which were located at layer IV of the primary visual cortex. The reference of the stimulation buffers was connected to a common return electrode of the MEA. The electrical impedance measured between each of the four electrodes and a non-current passing reference electrode (Ag/AgCl pellet placed in MEA dish) was 280-350 kΩ at 1 kHz. Fig. 8 C shows time-lapse pseudo-color images of the VSD signal recorded from the slice in response to a single biphasic pulse (200 μs/phase, 20 μA/phase), which was the same as that shown in Fig. 6, delivered from each stimulating electrode. In both recordings, the

depolarizing response was initiated around the stimulation site and propagated to layers II/III and V in a columnar fashion (second to third frames of Fig. 8 C). The depolarizing region expanded laterally in layers II/III (fourth frame) and then faded gradually. Such a spatiotemporal response pattern was similar to those obtained with a commercially available stimulator (STG4008, multichannel systems[1]) (not shown). The four stimulation buffers in parallel enabled the spatiotemporal pattern stimulations. For example, Fig. 8 D shows a neural response of the same slice in response to the single biphasic pulses delivered sequentially from channel 1 to channel 4 at intervals of 40 ms. As the stimulation site shifted in each step, the depolarizing region in layers II/III became prominent and expanded over the entire observation area. This was probably due to a spatiotemporal summation of the excitatory post-synaptic potentials.

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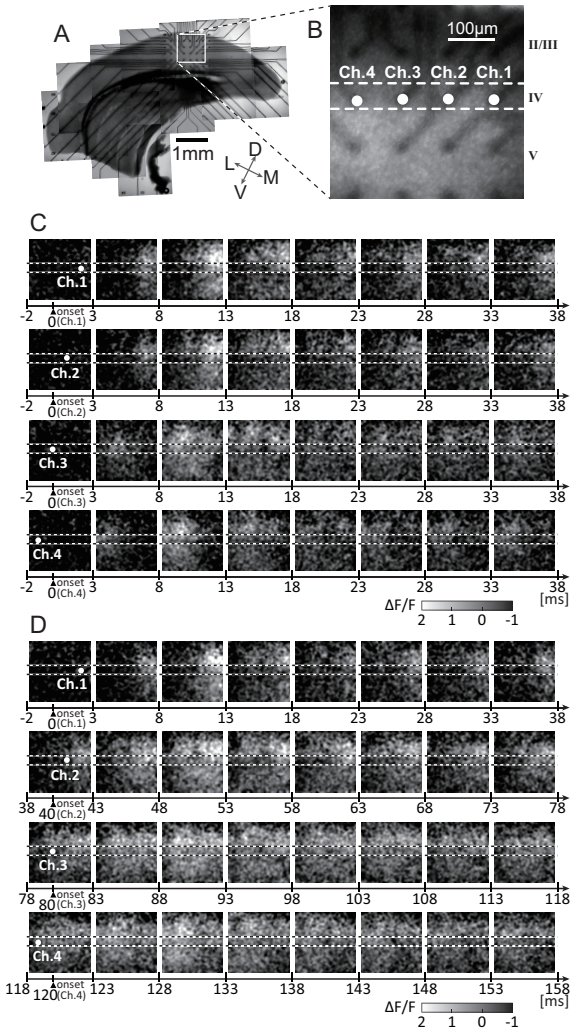

Fig. 8. Spatiotemporal pattern of in-vitro visual cortical tissue slice activities evoked by spatiotemporal stimulus current pulses delivered from the four electrodes connected to our chip. A. A microscope photograph of the cortical tissue slice on a multielectrode array, L: lateral, M: medial, V: ventral, D: dorsal, B. extended figure, which is an imaging area. Filled circles indicate stimulation electrode sites. C. Time lapse images of VSD signals (ΔF/F) (average of 4 trials) in the slice in response to the single current pulse from each channel. D. Time lapse images in responses to the single current pulses in order from Ch.1 to Ch.4 at intervals of 40 ms.

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