Toward a Reduced-Wire Readout System for Ultrasound Imaging

Jaemyung Lim, Evren F. Arkan, F. Levent Degertekin, and Maysam Ghovanloo

Abstract— **We present a system-on-a-chip (SoC) for use in high-frequency capacitive micromachined ultrasonic transducer (CMUT) imaging systems. This SoC consists of trans-impedance amplifiers (TIA), delay locked loop (DLL) based clock multiplier, quadrature sampler, and pulse width modulator (PWM). The SoC down converts RF echo signal to baseband by quadrature sampling which facilitates modulation. To send data through a 1.6 m wire in the catheter which has limited bandwidth and is vulnerable to noise, the SoC creates a pseudo-digital PWM signal which can be used for back telemetry or wireless readout of the RF data. In this implementation, using a 0.35-µm std. CMOS process, the TIA and single-to-differential (STD) converter had 45 MHz bandwidth, the quadrature sampler had 10.1 dB conversion gain, and the PWM had 5-bit ENoB. Preliminary results verified front-end functionality, and the power consumption of a TIA, STD, quadrature sampler, PWM, and clock multiplier was 26 mW from a 3 V supply.**

I. Introduction

More than 17.3 million people die each year by cardiovascular diseases worldwide, and arterial diseases have the highest proportion [1]. Therefore, there is a high demand for real time imaging technologies for arteries. Researchers have developed invasive and non-invasive methods of imaging. Among them, ultrasound imaging has proven to be a relatively inexpensive and effective tool, and intravascular ultrasound (IVUS) has become one of the most promising methods for diagnosis of coronary artery diseases and guiding cardiovascular interventions over the last decade [2].

One of the significant challenges of IVUS is the higher frequencies required for high resolution images. While conventional medical ultrasound systems utilized in cardiac or abdominal imaging generally use frequencies ranging from 2 MHz to 10 MHz, IVUS is performed in the 20 ~ 60 MHz range. Capacitive micromachined Ultrasonic Transducers (CMUTs) fabricated on CMOS electronics have been shown to be an effective way to miniaturize IVUS systems. In these systems, electronics for analog beamforming and time multiplexed readout have been implemented to miniaturize the system and reduce the cable count [3], [4]. However, to reduce the size of the IVUS imaging system down to 0.4 mm diameter so that it can be integrated on a typical guidewire, the number and size of the electrical wires should be further minimized. The length (~1.6 m) and the size of these wires may impose bandwidth limitations as well [5]. In addition, a long wire is vulnerable to noise and interference. To overcome these challenges, digitization or modulation of the raw data through the long wire is desired. Increasing the sampling rate for high-frequency IVUS results in more power consumption and require high speed clock if the signal is digitized at the front-end. On the other hand, lowering the frequency of the raw signal and eliminating the ADC and its associated digital circuits can reduce the power consumption. For the IVUS system operating around 40 MHz a 10 MHz bandwidth would be adequate. Based on this fact, a few sampling techniques have been proposed that reduce the required bandwidth [6], [7]. The quadrature sampling technique in [7] is one of the most common techniques, which can detect the envelope of the RF signal that contains the image data, while allowing for a lower sampling rate.

In this paper, we present a proof-of-concept capacitive micromachined ultrasonic transducer (CMUT) receiver system-on-a-chip (SoC) with quadrature sampling. We implemented two double-balanced passive mixers as the quadrature sampler. The delay locked loop (DLL) based clock multiplier provides local oscillator signals which have 90° phase difference between them. The pulse width modulator (PWM) converts analog signal to time signal in terms of pulse width data and send it to an external signal processor through long (1.6 m) and thin (100 µm dia) wires, which are driven by a digital wireline driver. We give an overview of the 1-D CMUT array in section II and the system design in section III. We verify the preliminary system functionality with the results presented in section IV, followed by the concluding remarks in section V.

II. 1-D CMUT Array for IVUS

While piezoelectric transducers have been commonly in use, CMUTs are viable alternatives with several advantages. CMUTs are fabricated based on micromachining and lithographic principles which provide both flexibility in shape and size, particularly with features well below 20 µm. They can also be compatible with standard CMOS process, allowing for further integration [3]. In addition, CMUTs can be designed to have lower mechanical impedance than the acoustic impedance of water, which ensures an over-damped system, leading to wide bandwidth and effective energy transfer to water, that constitute more than 90% of the tissue mass [8].

The lateral resolution of the ultrasound image is linearly proportional to the frequency of the generated ultrasound wave, whereas, the axial resolution depends on the bandwidth. Thus, the ultrasound system with high frequency and high bandwidth is highly desired. Given the acceptable performance limitations for IVUS, we designed a CMUT array operating around 40 MHz with more than 10 MHz bandwidth.

The 1-D CMUT array in Fig. 1a is designed with help of our custom simulation code implemented in the MATLAB environment [10]. Although in the actual implementation

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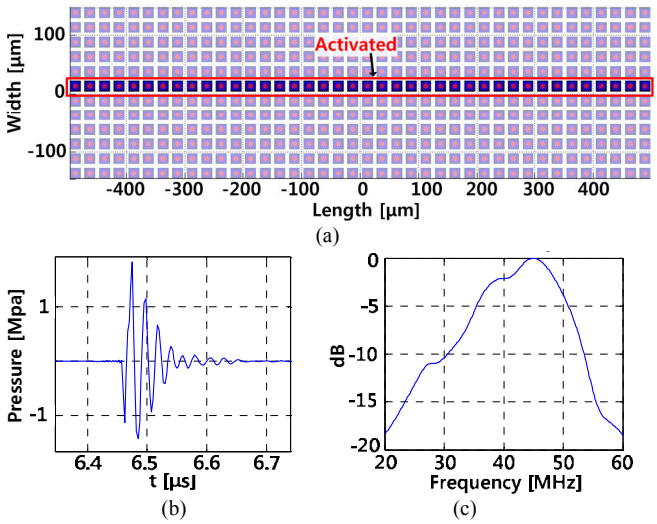

Fig. 1. (a) Layout of the simulated 1-D CMUT array, (b) simulated pressure output, (c) frequency component of the pressure output.

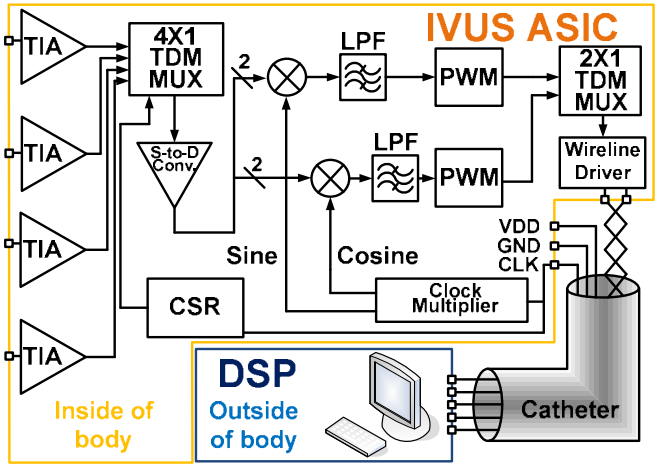

Fig. 2. Overall block diagram of ultrasound imaging system.

each element will be approximately 1mm long, in the simulations we used shorter elements considering the computation time. In the simulations, each element consists of 8 membranes that are 20 × 20 µm^2 in size with a 15 × 15 electrode and a Silicon nitride membrane thickness of 2.2 µm. The gap is 50 nm and the spacing between membranes is 5 µm. In simulation, the element in the middle is actuated with a 12.5 ns pulse of 50 V in amplitude. The simulated pressure output on the array surface, shown in Fig. 1b, has 2.8 MPa peak-to-peak amplitude. In Fig. 1c, the frequency response of the signal has a center frequency around 40 MHz and -3 dB bandwidth within 34 MHz ~ 48 MHz.

III. System Architecture

The overall block diagram of the proposed ultrasound imaging system is shown in Fig. 2. Since the more challenging aspect of the system design is the receiver side and data readout, we focused on the receiver (Rx) electronics. The capacitive membrane in the Rx CMUTs convert the acoustic vibrations echoed back towards the transducer array to current. The trans-impedance amplifiers (TIAs) on the front-end of the ultrasound imaging SoC, which are connected to the Rx CMUTs, convert the echo signals to

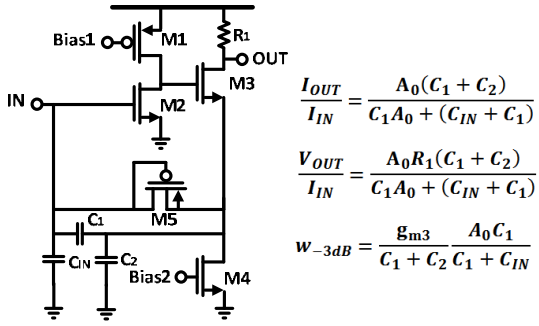

Fig. 3. Schematic of the capacitive-feedback transimpedance amplifier

voltage. Therefore, TIAs can operate at low voltage and there is no need to implement high voltage protection switches. In addition, because our target is synthetic aperture ultrasound imaging [11], only one CMUT is used at a given time. A 2-bit counter is used as a channel selector, and it chooses which of the 4 TIAs is connected to the rest of the system. To reduce self-mixing and the noise, we implemented a double balanced passive mixer, which down converts the received 40 MHz centered echo signal to baseband. For quadrature sampling with direct down conversion, we need 40 MHz in-phase and quadrature signals. To create them from a 10 MHz sinusoidal input, we utilized a clock multiplier. Down-converted input data is further converted from amplitude to time domain using a PWM circuit. The I and Q PWM pulses are time multiplexed and transmitted through a wireline driver and pair of twisted wires to be recovered and converted to digital data by the external time-to-digital converter (TDC) [12].

A. Trans-Impedance Amplifier

We implemented the capacitive feedback TIA in [3] with 45 MHz bandwidth and 100 kΩ trans-impedance, shown in Fig. 3. On-chip capacitors C_1 and C_2 are 100 fF and 400 fF, respectively. C_{IN} is 3.6 pF including CMUT capacitance of 1.6 pF and 2 pF for pad capacitances of ASIC and CMUT. Pseudo-resistor M5 is used as a DC bias because pseudo resistor exhibits more than 10 MΩ with small area (3 × 2 µm^2). Since C_{IN} is about 40 times larger than the one in [3], the TIA trans-impedance is lower (100 kΩ).

B. Clock Multiplier

A clock multiplier receives 10 MHz sinusoidal signal as an input. Because the wire is very thin (100 µm dia) and long (1.6 m), the wire itself has bandwidth limitation. With frequencies higher than 15 MHz signal, we cannot neglect the reflection caused by the wire. Thus, we choose 10 MHz as the external clock frequency. Since the passive mixer switches in quadrature sampler need high amplitude LO signal to reduce their resistance, we used rail-to-rail square wave to drive the mixer switches. In this system, a dual-loop DLL is used as part of the clock multiplier (Fig. 4a). Compared to a phase locked loop (PLL), DLL has lower power consumption, better stability, fast locking time, and less jitter. Delay cells consist of current starved inverters, which current is controlled by a charge pump (CP).

To make 50% duty cycle, this clock multiplier has two identical feedback loops which contain the charge pump and phase frequency detector (PFD). One loop is for locking rising-edge and the other loop is for falling-edge. When both

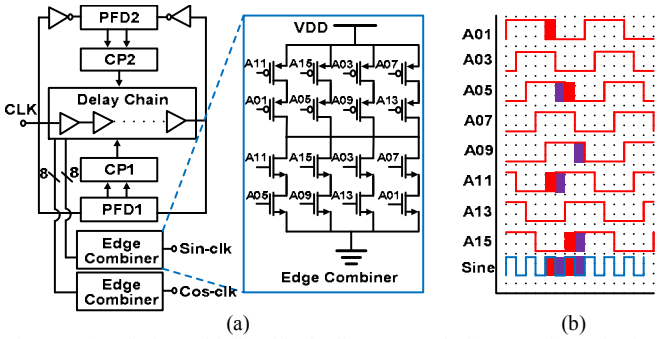

Fig. 4. (a) Clock Multiplier block diagram, and (b) operation of edge combiner.

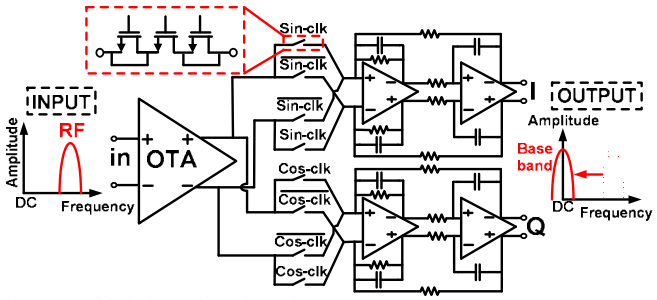

Fig. 5. Double balanced passive mixer.

loops are locked, every delay stage has 50% duty cycle. Because a quadrature demodulator needs two local oscillator signals which have 90˚ phase difference, we implemented two edge combiners and 16 delay cells. Odd-numbered delay cells make 'sine' square wave, and even-numbered delay cells make 'cosine' square wave. Each edge combiner has 4 branches of discharging and charging nodes. Thus, during one clock cycle, 4 rising edges and 4 falling edges are generated by combining specific delay cell rising and falling Edges, as shown in Fig. 4b.

C. Quadrature Sampler

In Fig. 5, a quadrature sampler with the double balanced passive mixer is shown. We choose the passive mixer for high linearity and low noise, while adopting the double balanced topology to reduce LO signal feedthrough, which causes self-mixing. Quadrature sampling needs two mixers with different LO signals. In this mixer, switches and low pass TIA are driven by an operational transimpedance amplifier (OTA). Because two mixers use same input signal, the OTA stage does not need to be separated. Since two mixers share one OTA, this quadrature sampler requires only one OTA, two switches, and two biquad TIAs. We implemented two half-sized dummy switches on both sides of the main switch to reduce the switching noise due to charge injection and clock feedthrough. The OTA converts input voltage to current, which flows through switch array and converted again to voltage by the low pass biquad TIA. High side injection signal (LO + RF) should be suppressed because the mixer is intended for down-conversion. A 2nd order biquad filter was sufficient because the baseband signal is around DC, while the high side injection is around 80 MHz.

D. Dual-Slope Pulse Width Modulator

The dual slope pulse width modulation (PWM), shown in Fig. 6a, was adopted for amplitude-to-time conversion (ATC)

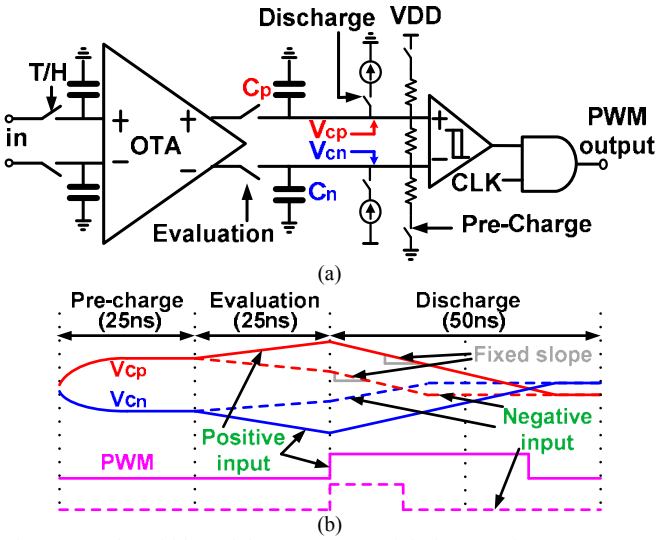

Fig. 6. (a) Pulse width modulator (PWM), and (b) its operation.

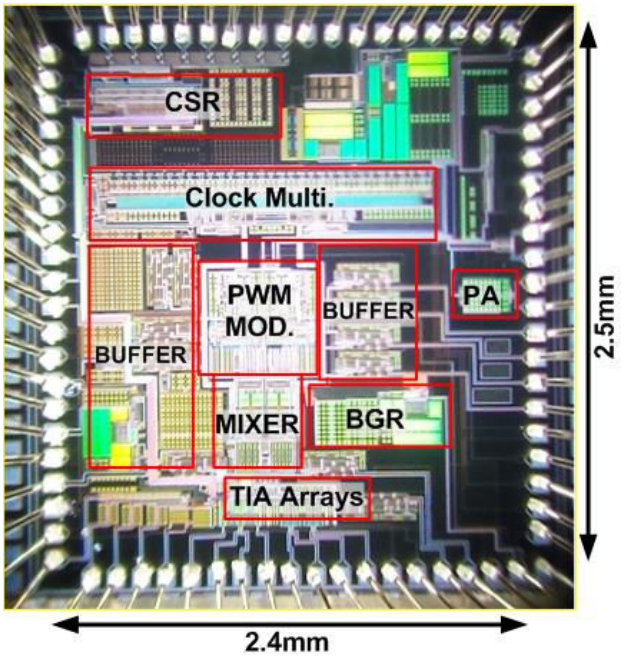

Fig. 7. Micrograph of the first ultrasound imaging ASIC prototype implemented in TSMC 0.35-µm std. CMOS process.

to maintain simplicity, while improving the signal robustness against noise and interference. A PWM circuit occupies less space and needs lower frequency clock compared to an ADC [12]. To reduce the number of wires in the future, communication between ASIC and handle needs to be wireless and PWM can be easily combined with wireless communication techniques as in [13].

The PWM block has 3 stages. At pre-charge stage, C_p and C_n are charged and discharged, respectively, to designated voltages through a resistive voltage divider. During this time, track and hold (T/H) switches at the input are opened to hold the sampled input voltages and settle the OTA output current for faster response during the evaluation stage. During the evaluation stage, C_p is charged and C_n is discharged by the OTA when input voltage is positive, and vice versa when input voltage is negative (Fig. 6b). The charging and discharging slopes are determined by the product of the OTA

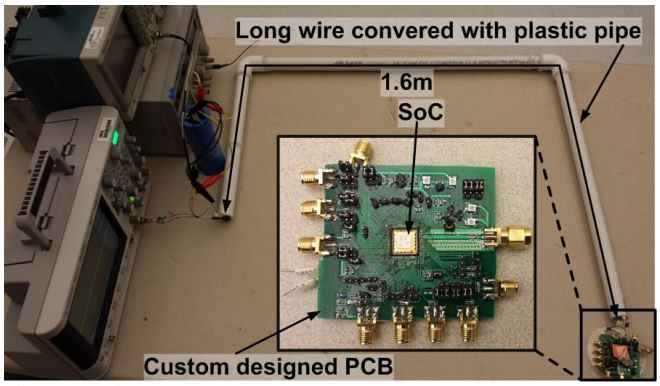

Fig. 8. Experiment setup.

transconductance (G_m) and differential input voltage.

During discharge stage, constant current sources charge C_n and discharge C_p with fixed slope. In this stage, the PWM pulse is raised and a comparator is turned on to compare V_{cp} and V_{cn}, which cross point indicate the PWM pulse falling-edge. We implemented two PWMs. One is for the in-phasesignal and the other is for quadrature signal. Because only half of a sampling cycle is used for the discharging stage in which the PWM pulse is generated, the two PWM sources can be time division multiplexed to share one output.

IV. Results

The first ultrasound imaging ASIC prototype, occupying 2.5 × 2.4 mm^2, was fabricated in 0.35-µm standard CMOS, as shown in Fig. 7. Twisted wires, 1.6 m in length and 100 µm in diameter (MWS wire industries, Westlake village, CA), were used in a PVC pipe to emulate the catheter, as shown in Fig. 8.

A. Transimpedance Amplifier and STD Converter

In simulation results, the input referred noise was 3 pA/√Hz at 40 MHz. The single-to-differential converter, which is placed after the TIA, has -3 dB bandwidth at 100 MHz and 0 dB gain in simulation. Measured -3 dB bandwidth of TIA is 45 MHz with 110 kΩ impedance gain and power consumption of it is 3 mW. We designed TIA with -3 dB bandwidth at 80 MHz, 50 kΩ trans-impedance and 7 mW power consumption. Because of process variation, R_1 in Fig. 3 increased, and we had to decrease the bias point of the TIA to decrease voltage drop across R_1. Thus, the gain was increased by two, while the bandwidth shrunk by half. The 4-ch TIAs are connected to the STD via TDM MUX.

B. Clock Multiplier and Quadrature Sampler

In Fig. 9a, the 10 MHz sinusoidal input signal and 40 MHz square wave multiplier clock output are depicted. In Fig. 9b, Clock $jitter_{rms}$ is 443 ps and $jitter_{peak\text{-}to\text{-}peak}$ is 1.8 ns, which are 3.5% and 14.5% of the clock period, respectively. It consumes 700 µW. The double balanced passive mixer had a conversion gain of 10.1 dB, -3 dB bandwidth of 2 MHz, and power consumption of 6 mW. The design target for the low pass biquad TIA cut off frequency was 5 MHz. However, process variations resulted in the TIA bandwidth to be 2 MHz in measurements. Total harmonic distortion

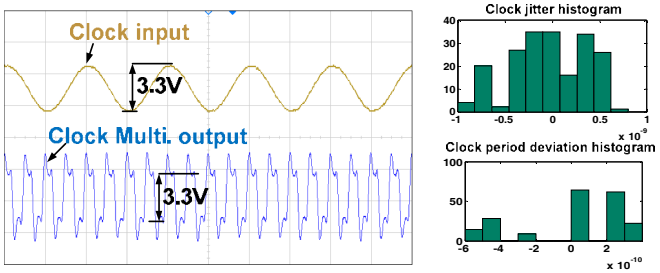

Fig. 9. (a) Clock multiplier measured results, and (b) Clock jitter.

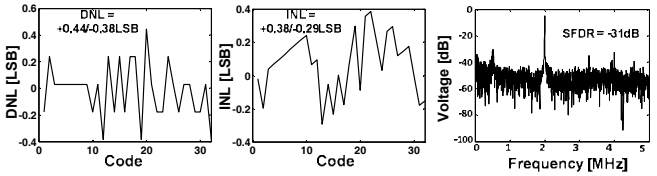

Fig. 10. PWM measured (a) DNL, (b) INL, and (c) single tone measurement.

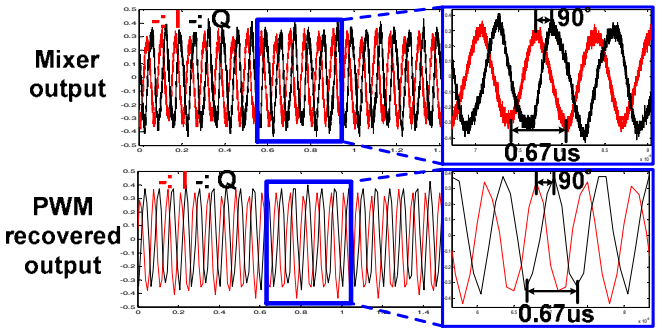

Fig. 11. System measurement with single frequency input.

(THD) is 0.98% with ideal square wave LO signals. In simulation, periodic input referred noise was 200 µV at a bandwidth with 5 MHz.

C. Dual Slope Pulse Width Modulator

Fig. 10 shows the INL (+0.38 / -0.29 LSB) and DNL (+0.44 / -0.38 LSB) of the dual slope PWM when operating at 10 MS/s with 5-bit resolution. The total number of samples through the twisted wireline driver, considering the TDM of the two PWM blocks was 20 MS/s. In Fig 9c, we show the single tone measurement at 2 MHz. Measured suprious-free dynamic range (SFDR) is -31 dB.

E. System Operation

In Fig. 11, a single tone test was conducted to see the overall system functionality. A 41.5 MHz current signal was applied as an input. The red and black traces indicate quadrature sampling in-phase (I) and quadrature (Q) signals, respectively. Because of clock multiplier's non-idealities, the mixer had gain variation and its output was distorted. Thus, THD is increased 2.5% from 0.93% when LO signals are ideal square waves. The input signal was 41.5 MHz, which resulted in a 1.5 MHz output after mixing with the 40 MHz LO signal. In Fig. 11a, I and Q signals clearly show 90° phase difference. In the recovered signal from the PWM pulses, shown in Fig. 10b, because of the limited PWM sampling rate, high frequency noise in the mixer outputs has

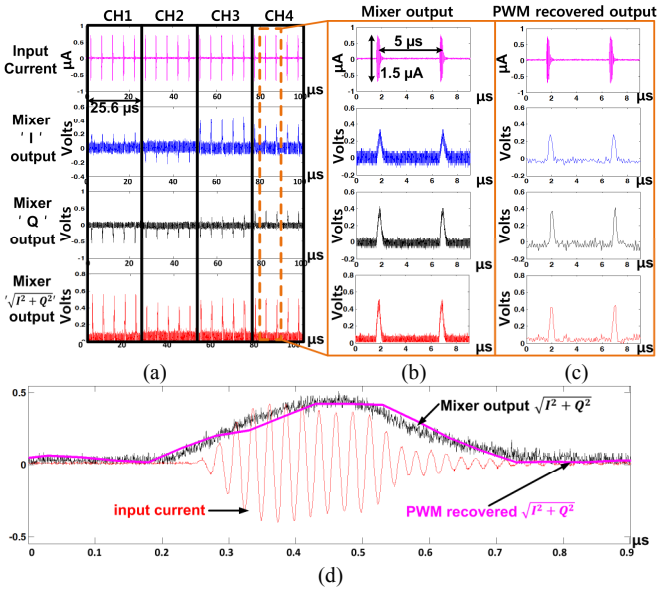

Fig. 12. System-level measurements with an emulated 38MHz~42MHz input signal, (a) four channel outputs, (b) one channel zoomed-in output, (c) one channel output recovered from PWM pulses, and (d) comparison between input, mixer output, and PWM recovered output.

been discarded.

Fig. 12 shows an experiment with an input current signal resembling that of Fig. 1b with a bandwidth within 38 MHz ~ 42 MHz range. The input signal was generated by passing multiple successive pulses with 12.5 ns and 25 ns pulse width through a 3rd order bandpass filter with 40 MHz center frequency.

Fig. 12a shows the quadrature sampler output from four channels. To let the CMUT have enough time to receive the echo signal, we set channel to channel multiplexing time to be 25.6 µs. Each channel has a different delay and phase shift. Therefore, channels show different I and Q signals. However, $\sqrt{(I^2+Q^2)}$, which indicates the envelope of the signal, shows similar waveforms in all channels. Fig. 12d, shows the input current signal, quadrature sampled signal, and the signal recovered from PWM pulses together to show partial system functionality. Table I summarized the specification of the current prototype system.

TABLE I
SPECIFICATIONS

	Design Target	Measurements
Technology	TSMC 0.35-µm CMOS	TSMC 0.35-µm CMOS
TIA Bandwidth	80 MHz	45 MHz
TIA impedance gain	50 kΩ	100 kΩ
PWM Sampling rate	2 x 10 MS/s	2 x 10 MS/s
ENOB	8-bit	5-bit
Power consumption	45 mW	26 mW
Mixer bandwidth	5 MHz	2 MHz

V. CONCLUSION

The functionality of a proof-of-concept prototype ultrasound imaging system with on-chip quadrature sampling and pulse width modulation was evaluated using emulated current input signals. The output was delivered through a pair of long and thin twisted wires (1.6 m in length and 100 µm in diameter). The large feature size process (0.35-µm) has resulted in a large silicon area in this early prototype. The target SoC dimensions are 400 × 1000 µm^2, which should be achievable by radically reducing the circuit complexity and migrating to a deep sub-micron process. Furthermore, we have plans to include wireless communication in this system to further reduce the number of wires in the catheter.

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