A Low-power Current-Reuse Dual-Band Analog Front-End for Multi-Channel Neural Signal Recording

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***Abstract*— Thoroughly studying the brain activity of freely moving subjects requires miniature data acquisition systems to measure and wirelessly transmit neural signals in real time. In this application, it is mandatory to simultaneously record the bioelectrical activity of a large number of neurons to gain a better knowledge of brain functions. However, due to limitations in transferring the entire raw data to a remote base station, employing dedicated data reduction techniques to extract the relevant part of neural signals is critical to decrease the amount of data to transfer. In this work, we present a new dual-band neural amplifier to separate the neuronal spike signals (SPK) and the local field potential (LFP) simultaneously in the analog domain, immediately after the pre-amplification stage. By separating these two bands right after the pre-amplification stage, it is possible to process LFP and SPK separately. As a result, the required dynamic range of the entire channel, which is determined by the signal-to-noise ratio of the SPK signal of larger bandwidth, can be relaxed. In this design, a new current-reuse low-power low-noise amplifier and a new dual-band filter that separates SPK and LFP while saving capacitors and pseudo resistors. A four-channel dual-band (SPK, LFP) analog front-end capable of simultaneously separating SPK and LFP is implemented in a TSMC 0.18 µm technology. Simulation results present a total power consumption per channel of 3.1 µw for an input referred noise of 3.28 µV and a NEF for 2.07. The cutoff frequency of the LFP band is f_c=280 Hz, and f_L=725 Hz and f_L=11.2 KHz for SPK, with 36 dB gain for LFP band 46 dB gain for SPK band.**

I. Introduction

Neural recording microsystems presenting large number of data acquisition channels are enabling neuroscientists to study the brain activities of the freely moving subjects [1]. This complex information contribute to gain a better understanding of brain functions and will eventually benefit patients suffering from spinal cord injuries, Parkinson's disease and other neurological diseases with new treatments [2]. Neural recording microsystems consist of two main parts: an implantable bioelectronics interface and a wireless power/data receiver/transmitter for harvesting power from a wireless transmitter and for transmitting/receiving the recorded data and commands. Transferring raw neural recorded signals from a large number of recording channels to an external base station require large bit rates, which leads to significant and sometimes prohibitive power consumption in the implanted part. For example, a microsystem featuring five hundred electrodes sampled at 20 ksps with 8-bit precision, would generate a continuous bit rate of 80 Mbps towards an external station. Consequently, data reduction is often performed on the raw recorded data before the transmitter. The spike signals (SPK) are extracellular biopotentials that can be recorded in the vicinity of a neuron. The frequency range of these signals spans from 100 Hz to 10 kHz, and their amplitude, which depends on the distance between the recorded cell and the recording electrodes is typically in the range of 500µV [1]. On the other hand, local field potentials (LFP) results from a local averaging of the combined electrical activities of several neurons around a low-impedance recording electrode. LFP occupy frequency band ranging from a few mHz up to around 300 Hz. LFP have higher amplitudes than SPK and can be as large as 5 mV [4]. Most data reduction schemes aim to detect and extract occurrences of SPK which correspond to a fraction of the raw data [3]. SPK can also be classified and sorted on-chip to achieve very high data reduction ratios by only transmitting time stamps [4]. Applying a data reduction scheme requires to separate the recorded broadband neural signals into a SPK band and a LFP band prior to signal detection and extraction. Then, extracted biopotentials can be transmitted to save the data link bandwidth power.

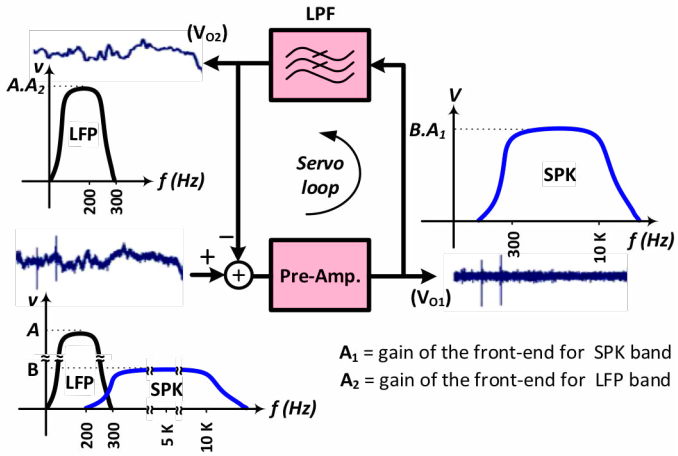

Figure 1: Conceptual block diagram of the proposed structure.

In this work, the proposed analog front-end separates the neuronal spiking signal band and the local field potential band in the analog domain, immediately after the first pre-amplification stage. Separating LFP and SPK bands in the analog domain increases SNR and allows using different gain values, which in turns relaxes requirements on dynamic range. The proposed dual-band analog front-end is described

This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and by the Microsystems Strategic Alliance of Quebec (ReSMiQ).

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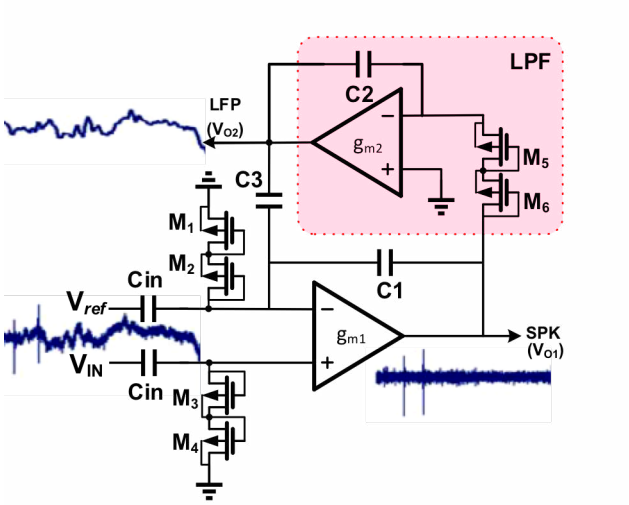

Figure 2: Single ended implementation of the proposed structure.

in Section II. Simulation results to verify the desired behavior of the proposed system are presented in Section III. Finally, conclusions are drawn in Section VI.

II. Overview of the Analog Front-End

A. LPF and SKP bands separation

Neural amplifiers to separate LPF and SPK have been reported in previous works for use in multi-channel neural recording systems. While some approaches consist in separating these bands using digital signal processing prior to digitization of the recorded signals, other separate both bands immediately into the analog domain for increasing SNR and relaxing requirements on dynamic range [12]. Fig. 1 shows the schematic of a single-ended implementation of the proposed dual-band LNA scheme. As shown, the LNA takes a broadband neural signal and generates two separated output signals lying into two different frequency bands. The low-frequency output V_{O1+}, V_{O1-} contain LFP and has a bandwidth of 0-300 Hz. The high-frequency output V_{O2+}, V_{O2-} which ranges from 300 Hz to 10 kHz, contains spike signals. In the proposed LNA, the output of the first low-pass LNA is amplified and filtered again into a second low-pass filter that act as a servo loop by subtracting the amplified LFP from the broadband recorded signal in order to generate the SPK. A single ended implementation of the proposed LNA scheme is shown in Fig. 2 while the fully differential version is shown in Fig. 3. A fully differential implementation is much more robust against noise. The high-frequency output of the recorded signals (100 Hz – 10 kHz) at V_{O1+}, V_{O1-} has a gain of A_1, while the low-frequency output at V_{O2+}, V_{O2-} has a gain of A_2. An AC coupling networks (including C_{in} and M_1, M_2, M_3, M_4) is used for implementing a high-pass filter with a high-pass cutoff frequency located within the mHz range for removing the large input DC offset from electrodes and avoiding saturation into the amplifiers. The transfer function of the SPK band is given by:

$$A_1 = \frac{V_{O1+}-V_{O1-}}{V_{in}-V_{ref}} = \frac{C_{in}}{C_2} \times \frac{PR_1 C_{eq}(S)}{1+PR_1 C_{eq}(S)} \times \frac{PR_2 C_{in}(S)}{1+PR_2 C_{in}(S)} \quad (1)$$

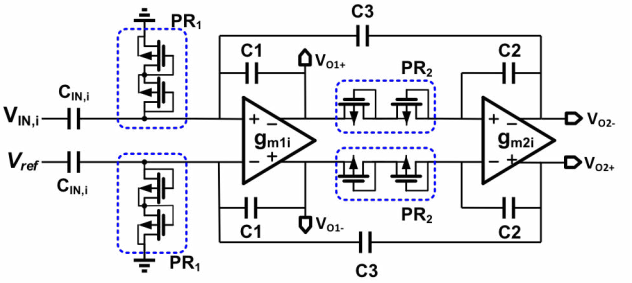

Figure 3: Fully differential implementation of the proposed dual-band neural amplifier.

$$C_{eq} = C_3 \times \frac{C_2}{C_4} \quad (2)$$

whereas, the transfer function of the LFP band is given by

$$A_2 = \frac{V_{O2+}-V_{O2-}}{V_{in}-V_{ref}} = A_1 \times \frac{-1}{PR_1 C_3(S)}, \quad (3)$$

where PR_1 and PR_2 are the equivalent resistances of the pseudo-resistors implemented with MOSFETs M1 to M_6. In addition to working under low-power budget, the proposed dual-band analog front-end presents several interesting advantages over other neural amplifiers such as:

- Uses the same AC coupled circuit to remove the large input offset (M_1-M_4 and capacitors C_{in}) for both the SPK and the LFP extraction circuits which decreases silicon die area since input capacitors (C_{in}) are usually on the order of several pF [9], [12].
- Achieves improved linearity by removing the pseudo-resistors from the feedback path of a closed-loop opamp.
- Presents gains for both of the SPK and LFP bands are that depend on ratios of integrated capacitors which prompt for high linearity.

B. Design of Current-Reuse OTA

Several efforts have been previously devoted to improving the size, the precision and the noise efficiency factor (NEF) of LNAs in neural recording applications. Among them are the component sharing arrays [12], the self-biased fully differential structure [8], and the signal folding topologies, which is using signal reconstruction algorithms in the digital domain [10]. In addition, several efforts towards optimization of the tradeoff between power consumption and input noise [6], [10] have been reported. Specific circuit techniques have been proposed, such as folded cascode with low-current folds [12], reference sharing [8], $g_m$boosting via current-splitting [11], and input circuits using complementary device inputs [12] or back-gate driven devices. Recently, an orthogonal current-reuse structure has been presented in [13]. Such an orthogonal current-reuse structure is very attractive in this application since the required voltage headroom in a differential pair can be minimized by operating an input differential pair in sub-threshold regime, amplifiers using stacked, sub-threshold inputs are able to yield ultra-low-power and operate properly under low-voltage supplies, without affecting the noise performance. The implemented current-reuse circuit topology presents several stacked inputs, the trans-conductance of which increase proportionally to the number of stacked input pairs in the amplifier [13]. A

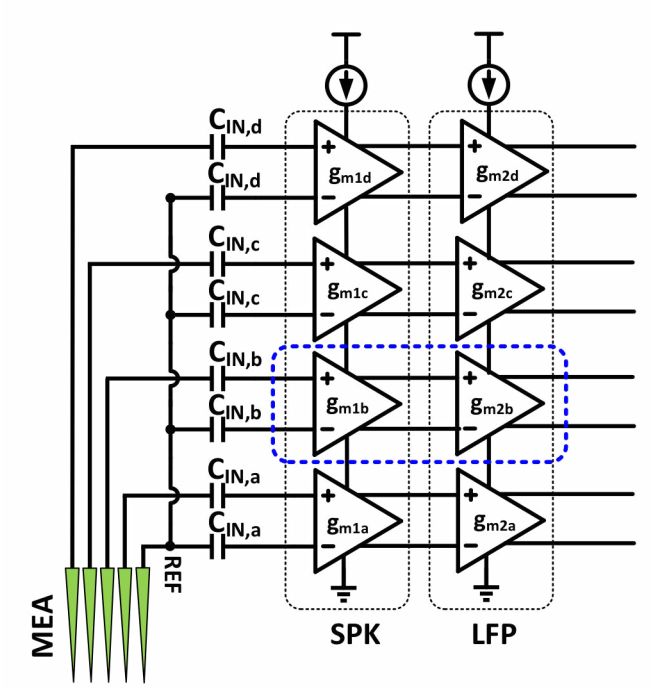

Figure 4: Current-reuse structure for a 4-channel analog front-end.

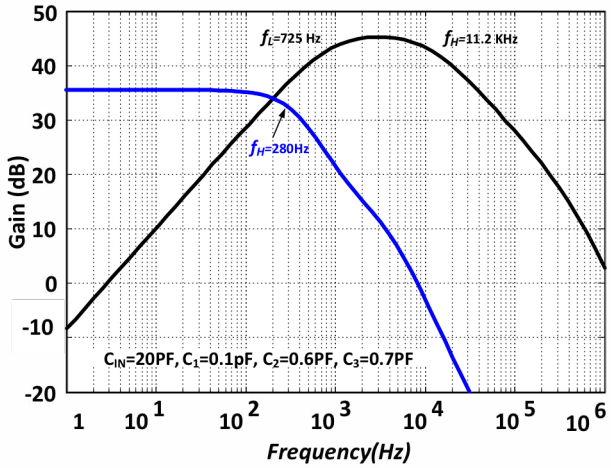

Figure 5: Frequency response of the proposed structure for SPK and LFP.

current-reuse structure increases the tran-conductance at the cost of voltage headroom. Each stacked differential pair needs one V_{DS} to work properly [13]. Therefore, one current source is employed to bias each stack of several differential input stages, which tail currents are coming from previous stage (Fig. 4). The schematic of a two input stacked current-reuse amplifier is presented in Fig. 6. The second stage (Stage 2 in Fig. 6.) is divided into two differential pairs, the input transistors of which are half the size of the input transistors of the first stage [13]. Both stacked input-stages (Stage 1 and Stage 2 in Fig. 6.) have sameg_m. As the total current that flows in second stage is same as the current that flows in the first stage (I_{bias}), the overall $g_m$in the second stage is equal to the g_m in the first stage. Each output current (small signal currents i_1, i_2, i_3, i_4) is an independent and linear combination of several output currents derived from the corresponding input voltages. The input pairs in the second stacked stage are parallel because they have same inputs (V_{in2+}, V_{in2-}), but they are independent since their tail currents ($I_{bias}/2$) are independent. For example, to generate V_{Out1}, V_{Out1+} and V_{Out1}, the corresponding output currents are re-constructed by summing currents i_1, i_2 and currents i_3, i_4 respectively. V_{Out2} is generated by summing i_1, i_3 currents to construct V_{Out2+}, and currents i_2, i_4 to construct V_{Out2-} (See the schematic of the Output stage in Fig. 6).

III. Simulation Results

In order to measure the performance of the proposed dual-band LNA to separate the SPK and LFP signal simultaneously, a four-channel analog front-end is designed and simulated in a TSMC 0.18-µm technology. Since the filter stage (g_{m1}) is dominant for determining the noise performance of the entire analog front-end, the power consumption of this stage cannot be decreased too much. However, power consumption can be reduced in the second filter stage since the input is already amplified by the low-frequency filter. In this design, the power consumption of the low-frequency filter stage is 2.325 μW per channel, and 775

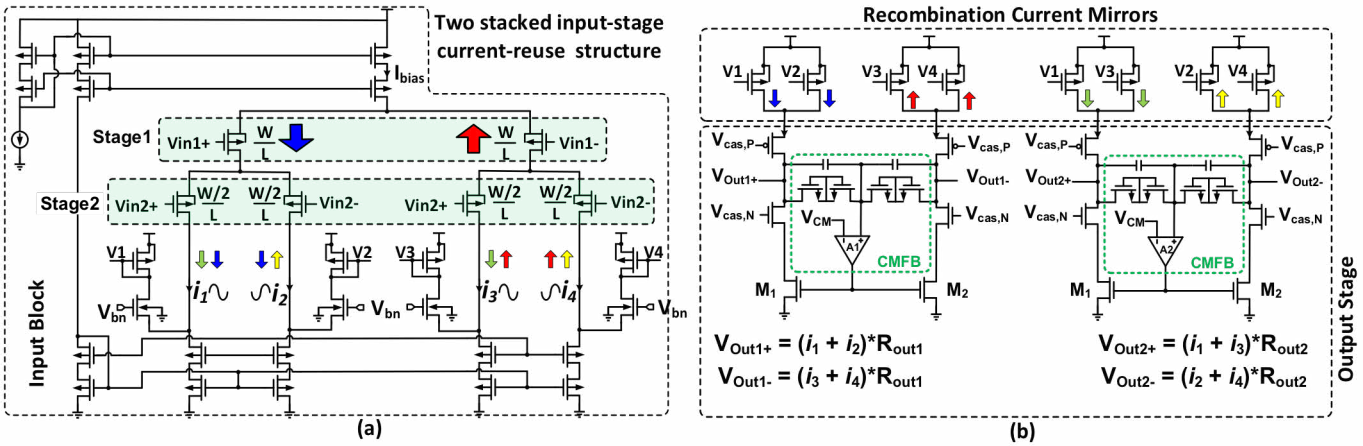

Fig. 6. (a) A two-stage current reused amplifier. Two input differential pairs are stacked, and share a same bias current source and a wide swing current mirror employed as an active load. These current mirrors copy the i_1, i_2, i_3 and i_4 to the output stage. (b) The employed common mode feedback circuit uses a low-power opamp and two pseudo resistors.

nW for the high-frequency filter.

Simulation results are presented in Fig. 5. In this design, capacitors values are C_{IN}=20 pF, C_1=0.1 pF, C_2=0.5 pF, C_3=0.6 pF, and the W/L ratios for the peso-resistors are 0.5/20 for PR_2 and PR_1. Figures. 7, 8, 9 presents the two output bands of the proposed LNA for a pre-recorded broadband neural signal. The LNA separates the SPK and LPF successfully. According to the employed capacitors ratio, gains of 46 dB and 36 dB are achieved for the SPK and the LPF respectively. Different gain values can be obtained for both bands by changing the capacitors value, for adjusting the swing of the output signal and use the full dynamic range. Moreover, different cutoff frequencies can be achieved by changing the capacitors values for changing the SPK and the LFP output frequency bands.

TABLE I. COMPARISION WITH OTHER WORKS

Parameter (LNA)	*[7]*	*[9]*	*[12]*	*[6]*	*This work*
Power (µW) per ch.	7.56	2.52	12	4.79	3.1
VDD (Volt)	2.8	1	1	0.5	1.8
Noise (µVrms)	3.06	3.83	2.2	4.9	3.28
NEF(SPK band)	2.67	3.03	2.9	5.99	2.07
NEF(LFP band)	-	5.27	-	-	4.37
BW (kHz)	4.9	5.7	10.5	10	10.5
Gain (dB)	40.8	54.2	40	36	36 and 46
PSRR (dB)	75	67	≥80	64	78
CMRR (dB)	66	65	80	75	72
Technology (nm)	500	180	130	65	180
Blocks included in comparision	LNA BPF	LNA	LNA	LNA, BPF,ADC	LNA

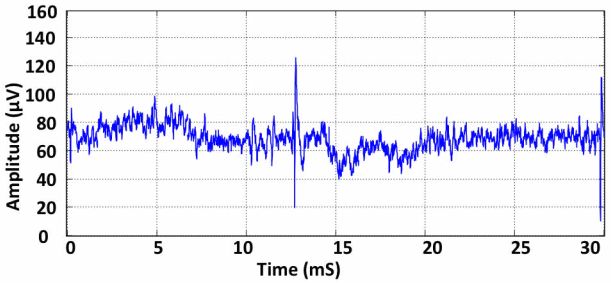

Figure 7: Pre-recorded broadband neural signal.

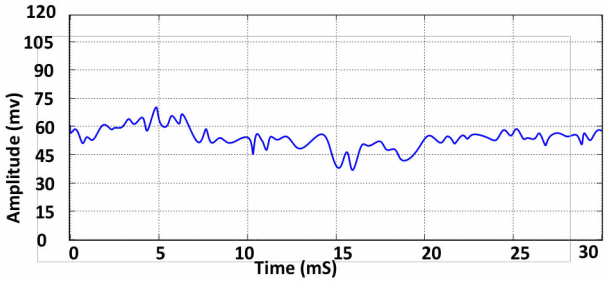

Figure 8: The separated local field potential band at the output of the proposed low-noise dual-band neural amplifier.

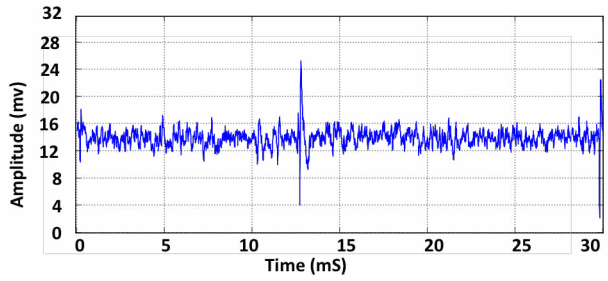

Figure 9: The separated spike signal band at the output of the proposed low-noise dual-band neural amplifier.

IV. CONCLUSION

A current-reuse dual-band analog front-end enabling to separate the SPK and LPF simultaneously has been presented. This system not only extracts the SPK and LPF at the same time, but also achieves excellent noise vs power vs area tradeoff, which are critical parameters in the design of practical multi-channel neural recording microsystems. These advantages make the proposed front-end a good prospect for enabling the next generation of multi-channel neural recording microsystems featuring thousands of recording sites.

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