A 700mV Low Power Low Noise Implantable Neural Recording System Design

Guanglei An, Chriswell Hutchens and Robert L. Rennaker II

Abstract— **a low power, low noise implantable neural recording interface for use in a Radio-Frequency Identification (RFID) is presented in this paper. A two stage neural amplifier and 8 bit Pipelined Analog to Digital Converter (ADC) are integrated in this system. The optimized number of amplifier stages demonstrates the minimum power and area consumption; The ADC utilizes a novel offset cancellation technique robust to device leakage to reduce the input offset voltage. The neural amplifier and ADC both utilize 700mV power supply. The midband gain of neural amplifier is 58.4dB with a 3dB bandwidth from 0.71 to 8.26 kHz. Measured input-referred noise and total power consumption are 20.7μVrms and 1.90 respectively. The ADC achieves 8 bit accuracy at 16Ksps with an input voltage of ±400mV. Combined simulation and measurement results demonstrate the neural recording interface's suitability for in situ neutral activity recording.**

Keywords— **Neural signal; low-power low-noise design; Neural amplifier; Pipelined ADC; subthreshold operation; smart RFID**

I. INTRODUCTION

In the past few decades, the low power, low noise integrated multiple neural signal recording systems have been developed for understanding and monitoring neural activities. Important performance parameters of these recent activities are summarized in TABLE I [1, 2, 3, 4]. These systems generally consist of low pass filters to amplify small biopotentials and reject the high frequency noise; ADC for digitizing the spike data and wireless telemetry circuit to transmit data from implant body. The amplitude of extracellular spike signal ranges from 50 - 500 uV and its frequency is on the order of 100Hz- 7 kHz. Hence, there is a major design challenge to develop small low-power acquisition circuits and at the same time achieve an acceptable input-referred noise [5].

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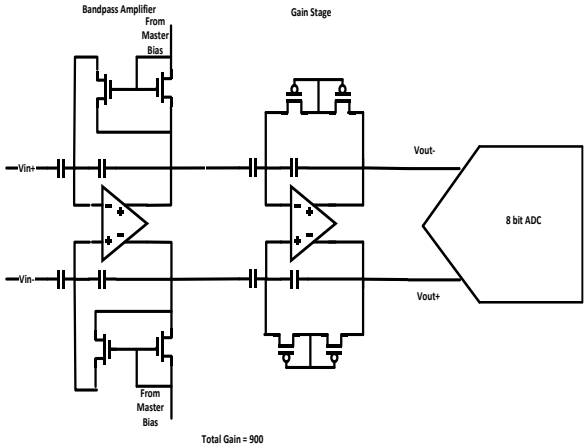

Figure.1 System Block Diagram

In this work, we present a two stage neural amplifier and 8 bit Pipelined ADC operating at 0.7V. A fully differential (FD) configuration is utilized to increase the common mode rejection, input common mode range, and reduce even order harmonic distortion. Section II introduces the optimized number of amplifier stages for minimum power and area; the 1.5 bit/stage multiplying digital to analog converter (MDAC) in Pipelined ADC with low Common Mode (CM) offset is discussed. The simulation and measurement results are shown in Section III and the conclusion is given in section IV.

TABLE I COMPARISONS OF NEURAL RECORDING SYSTEM

Author	Supply Voltage (V)	Midband Gain (dB)	Band Width (kHz)	Input Referred Noise (μVrms)	Total Power (μW)
Harrison[1]	3.55	60	5	5.1	135
Zhiming [2]	0.8	49	6.2	14	20
Walker [3]	1.2	40	10	2.2	43
Azin [4]	1.5	51.9-65.6	12	3.12	26.9
This work	0.7	58.4	8	20.7	5.47

II. SYSTEM DESIGN

A. Two stage neural amplifier

The schematic of the 1st stage Operational Transconductance Amplifier (OTA) including common mode feedback (CMFB) is shown in Figure. 3. The geometries of the transistors for the first OTA are presented in TABLE II. In this application, low power and low area consumption are both important. However, there is a tradeoff between the both. This makes optimizing the number of amplifier stages important. Assuming the OTA of each stage is a folded cascode structure with equal gains K, and gain bandwidth product. The total

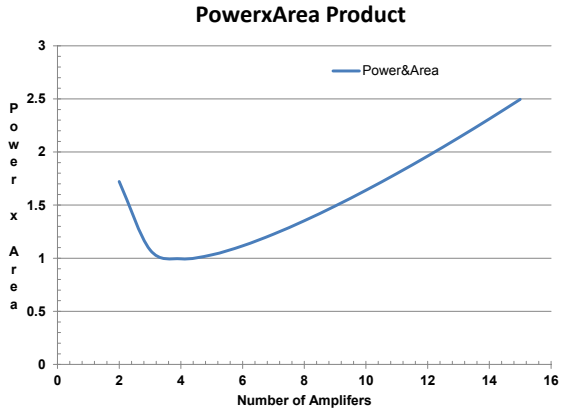

Figure 2. Plot of normalized power area product for different number of stages.

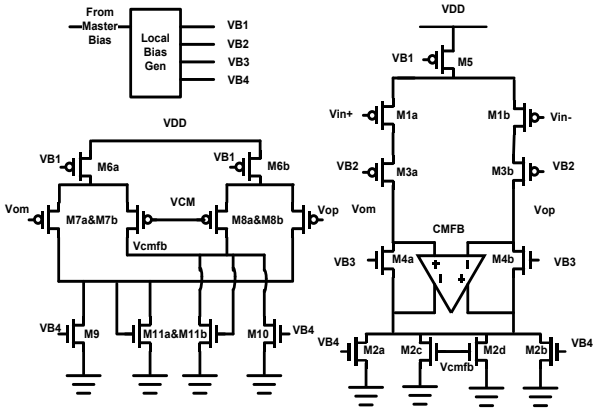

Figure 3. Schematic diagram of stage one OTA with its common mode feedback circuit.

power consumption and area product is given [6]:

$$P\,\&\,Area \propto \frac{2\pi n^2 * \sqrt[n]{G_T}\,(\sqrt[n]{G_T}+2)}{(\sqrt[n]{G_T}+1)} * \frac{0.833}{\sqrt{n}} \qquad (1)$$

G_T is the total gain of amplifier and n is the number of stages. Considering that each stage should have a gain greater than 10 to ensure noise contributions for following stages is negligible, and the total gain requirement G_T, is 900, a 2 stage amplifier with a gain of 30 per stage was selected. From post layout of two stage neural amplifier, the area of 1st stage is only 10% larger than that of 2nd stage, which is ensuing our previous assumption.

TABLE II GEOMETRIES OF FIRST STAGE OTA.

Devices	W/L(μm)
M1a&M1b	40/1.6
M2a&M2b	24/4.4
M2c&M2d	26.4/2.4
M3a&M3b	40/1.6
M4a&M4b	96/2.2
M5	238.08/1.6
M6a&M6b	39.68/1.6
M7a&M7b M8a&M8b	9.92/1.6
M9&M10	8/4.4
M11a&M11b	8.8/2.4

B. Pipelined ADC

The system block diagram of a pipelined ADC is shown in Figure. 4. The 8 bit 16 kSps pipelined ADC is comprised of a 2.5 bit front end followed by five 1.5 bit stage MDACs. A FD configuration with Correlated Double Sampling (CDS) techniques is utilized to alleviate the nonlinear distortion but with increased power consumption [7]. Of all the errors hindering ADC performance; noise, limited bandwidth, and DC gain, The voltage offset caused by mismatch is the more significant errors in the Pipeline ADC, followed by capacitor mismatch. Especially voltage offset from the first stage MDAC. As the offset voltage will propagate and be amplified by the gain of the following stages [8]:

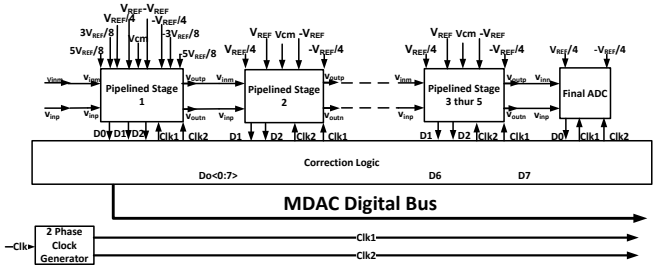

Figure 4. Block Diagram of Pipelined ADC.

$$V_{OS,Total} = \sqrt{(2^{n-1}V_{OS,MDAC1})^2 + (2^{n-2}V_{OS,MDAC2})^2 + \ldots + (V_{OS,MDAC8})^2} \qquad (2)$$

where $V_{OS,\ Total}$ is the total offset voltage of Pipeline ADC, $V_{OS,\ MDAC}$ is the offset voltage of MDAC, and n is the number of stages. The 1.5 bit MDAC architecture is shown in Figure 5. During PH1, the inputs of OTA are shorted to the outputs to CM voltage. During PH2, the SW 1 and 2 turn off but the leakage current through the two switches causes the sampled offset voltage at the inputs of OTA to drift, which further

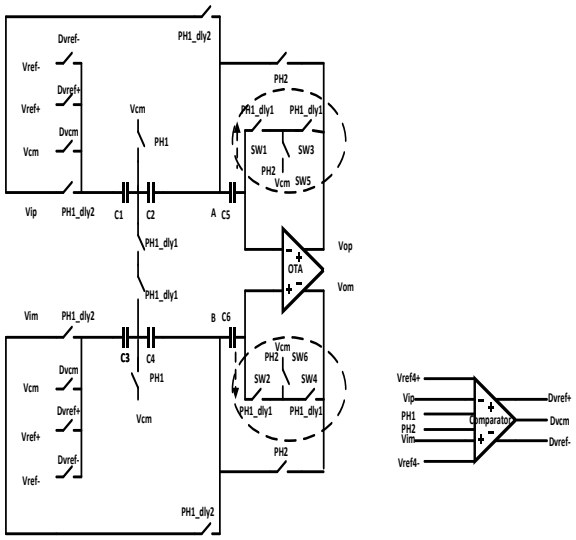

Figure 5. 1.5 bit MDAC Architecture

affects the offset voltage of CM nodes A and B. To reduce the leakage current through the switches, SW 5 and 6 are added to isolate the CDS capacitors from switch leakage present from output to input.

III. SIMULATION AND MEASUREMENT RESULTS

The neural amplifier and Pipeline ADC was fabricated in a 0.18-µm CMOS process and designed to operate on a 700mV supply. Figure 6 shows the combined neural amplifier frequency response. The midband gain is 58.4dB with a bandwidth of 710Hz to 8.26 kHz. The neural amplifier

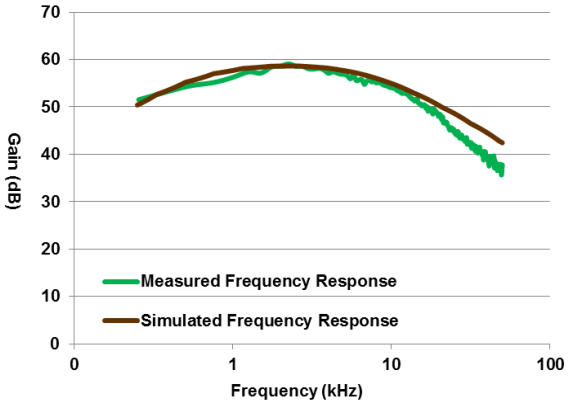

Figure 6. Simulated and Measured Frequency Response of neural Amplifier

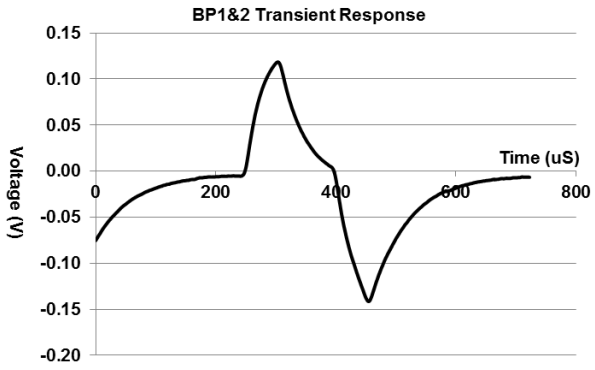

Figure 7. Neural Amplifier Transient Response

operates with 1.2V to 0.7V supplies consuming less than 1.90 µW at 700mV.

The transient response of neural amplifier is shown in Figure 7. Large signal behavior of neural amplifier in cascade is validated with an input 0.5mV pulse 1.5ms in duration. The resulting 114mV differentiated output with rise/fall equal 750us. Given

$$\frac{dV_{out}}{dt} = RC \times \frac{dV_{in}}{dt} \times K \tag{3}$$

$$RC = \frac{114mV}{0.5mV \times 0.8/750us} \times 900 \tag{4}$$

From (3) and (4) 1/RC equals 4.2*10^3, confirming the lower 3dB frequency.

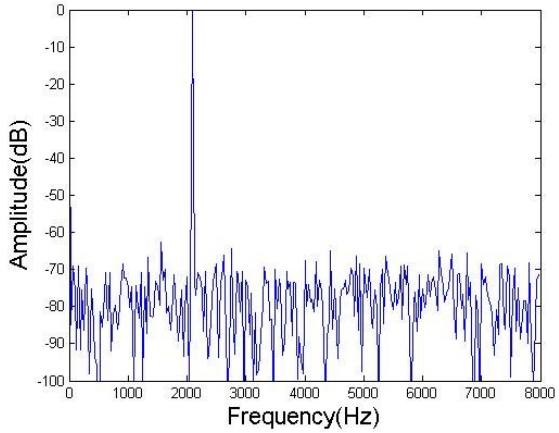

Figure 8. Simulated ADC Output FFT Spectrum Input@2.1kHz

TABLE III PERFORMANCE SUMMARY OF NEURAL AMPLIFIERS

	Midband Gain	f_low_3dB	f_high_3dB	Input referred noise	Output SNDR	Power Consumption	Power Supply
Stage 1	30dB	565Hz	11.8kHz	13.7uV	46.5dB	0.77uW	0.7V
Stage 2	30.2dB	202Hz	10.9kHz	62.6uV	45.2dB	0.77uW	0.7V
Two Stages Simulated	58.6dB	560Hz	8kHz	10uV	48.1dB	1.81uW	0.7V
Two Stages Measured	58.4dB	710Hz	8.26kHz	20.7uV	44.7dB	1.90uW	0.7V

The performance of previous neural amplifiers designs are summaried in TABLE III. The simulated ADC output FFT spectrums is shown in Figures 8. The resulting SNDR is 49.64dB with ENOB of 7.95bits. The total power consumption of the ADC including analog and digital part is 3.57uW with performance summarized in the TABLE IV as below.

TABLE IV ADC PERFORMANCE

Parameters	Simulation
Supply Voltage (V)	0.7
Input Range (V)	0.8Vpp
ENOB (bit)	8
Sampling Frequency (KHz)	16
Power Consumption (uW)	3.57
DNL&INL (LSB)	±0.5
FOM=Power/(2^{ENOB}*fs)	0.87pJ/step

IV. CONCLUSION

The low power, low noise two stage fabricated and tested neural amplifier and an 8 bit low power pipelined ADC were presented. Optimal stages for power, gain and area ensure both low power and area efficiency. A low CM and differential offset ADC suitable for multi-channel neural recording application was also presented. The functionality of the proposed neural recording system has been verified via extracted simulations and measurement results.

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